

Storage Concepts for SIMATIC S7-300 CPUs and for C7 Devices

1	Overview of Memory Area and Storage Concept.....	2
1.1	Version.....	2
1.2	Storage Concept.....	2
1.2.1	Load memory	2
1.2.2	RAM.....	2
1.2.3	System memory	3
1.3	Determining the memory IDs of a CPU	3
2	SIMATIC S7-300 CPUs and C7 Devices without Slot.....	4
2.1	Graphic display of the storage concept.	4
2.2	Load memory	5
2.3	Main memory	5
2.4	Application of the buffer battery	6
3	SIMATIC S7-300 CPUs and C7 Devices with Slot for an MC.....	7
3.1	Graphic display of the storage concept.	7
3.2	Load memory	8
3.3	Main memory	9
3.4	Application of the buffer battery	10
4	SIMATIC S7-300 CPUs and C7 Devices with Slot for an MMC.....	11
4.1	Graphic display of the storage concept.	11
4.2	Load memory	12
4.3	Main memory	13
4.4	Application of the buffer battery	13
5	The Storage Concept for SIMATIC S7-300 CPU Types and for C7 Device Types in Detail.....	14
5.1	The storage concept of individual SIMATIC S7-300 CPU types.....	14
5.2	The storage concept of the individual C7 device types	18

1 Overview of Memory Area and Storage Concept

1.1 Version

There are three main versions for S7-300 CPUs and C7 devices:

- [CPU without shaft](#)
- [CPU with shaft for a Memory Card \(MC\)](#)
- [CPU with shaft for a Micro Memory Card \(MMC\)](#)

The properties described in this chapter (1 Overview of Memory Area and Storage Concept) apply for three versions. In the following chapters type-specific properties are discussed.

1.2 Storage Concept

Storage concepts for SIMATIC S7-300 CPUs and C7 devices can be described by means of three storage areas:

1.2.1 Load memory

The load memory collects code and data blocks as well as system data (configuration, connections, module parameter, etc.). The blocks are transferred from the programming device (PG) into the load memory. Blocks not labeled as process relevant, are exclusively inserted into the load memory.

1.2.2 RAM

Process relevant code and data blocks as well as configuration data are stored in the main memory. The main memory is used for processing the code as well as preparing the data of the user program. Program processing is exclusively performed in the main memory and system memory areas.

Retentive main memory

The main memory is not retentive over the entire range for all CPUs. For some CPU types part of the main memory is retentive and the other part is non-retentive. The retentive part of the main memory can be used for retentive data blocks. The rest of the main memory can be used for code blocks, non-retentive DBs and SDBs.

Note For SIMATIC S7-300 CPUs there are the data block properties “Non-Retain” (Properties Datablock /General - Part2/Non-Retain).

In chapter [The Storage Concept for SIMATIC S7-300 CPU Types and for C7 Device Types in Detail](#) you see which CPU types and C7 devices support the data block properties.

1.2.3 System memory

The system memory of the SIMATIC S7-CPU is integrated in the CPU and cannot be expanded. It is divided into operand areas. Using the respective operations you address the data directly into the respective operand area in your program.

The system memory contains:

- the operand areas: memory bit (M), times (T) and counters (C)
- the process images of inputs (PII) and outputs (PIQ)
- the local data stack (temporary memory)
- the block stack,
- the interruption stack,
- the diagnostic buffer

1.3 Determining the memory IDs of a CPU

To determine the **memory IDs of your CPU** select a station in the SIMATIC Manager and go to PLC > Diagnostics/Settings> Module information.... There you select the "Memory" tab. (The connection to your CPU must be active (e.g. via MPI). The data are read from the connected CPU.)

In the Memory tab it is displayed how much load memory and main memory are currently free or assigned.

2 SIMATIC S7-300 CPUs and C7 Devices without Slot

2.1 Graphic display of the storage concept.

This figure shows the memory concept of the S7-300 CPUs and C7 devices without MC.

Figure 1: SIMATIC S7-300, without memory card



Integrated Load Memory (CPU 312 IFM and CPU 314 IFM)	
RAM	FEPROM
Code blocks Data blocks	Code blocks Data blocks



Work Memory	
Code	Data
Runtime relevant Code blocks	Runtime relevant Code blocks



System Memory
Process image of the inputs (PII) Process image of the inputs (PIQ)
Memory bit (M) Times (T) Counter (C)
Local stack Block stack Interruption stack
Diagnostics Buffer

2.2 Load memory

These CPUs and C7 devices have an integrated FEPRAM load memory on which the code and data blocks can be stored network and reset failsafe.

Location of load memory

The load memory is located internally within the CPU.

Setup of load memory and program buffer

The load memory consists of a RAM memory and FEPRAM memory. RAM and FEPRAM load memory have the same size.

The user program in the internal RAM load memory is buffered via the buffer battery.

Loading the program network failsafe load memory

The programming device (PG) writes the program to the integrated RAM load memory using the Load function. The "Copy RAM to ROM" returns the program to FEPRAM. If the program is located in FEPRAM, then it is battery independent and stored on the CPU network and reset failsafe.

Expansion options of the load memory

When requesting a larger load memory, either a respective CPU, or a CPU with slots for MC or MMC must be used.

2.3 Main memory

STEP 7 function "Load"

During the "Load" function, the selected code and data blocks are transferred to the internal RAM load memory, and from there, if process relevant, they are written to the main memory.

Retentivity of the data blocks

A battery buffer can keep all data blocks retentive. The CPU can keep a part of the data volume retentive without battery (HW Konfig -> CPU -> Properties -> Retentive Memory). A buffer battery needs only be used if you wish to keep an exceeding data volume retentive.

Note: A buffer battery cannot be used with the CPU 312-IFM.

Expanding the main memory

The main memory is integrated in the CPU and cannot be expanded. If a larger main memory is required, the user must use a different CPU with larger main memory.

Note If you wish to execute the STEP 7 function `Copy RAM to ROM ...`, the current values of the process relevant data blocks in the load memory are overwritten with the current values from the main memory. If the process relevant data blocks are then transferred back to the main memory (e.g. after memory reset), then the new current values from the load memory are adopted by the CPU as initial values. In SIMATIC STEP 7 these new initial values are displayed in the "Actual value" column.

2.4 Application of the buffer battery

For the CPUs, buffering is performed via a buffer battery, depending on CPU type.

The battery only buffers data and time. Therefore, when using a battery, the CPU behaves as in unbuffered mode.

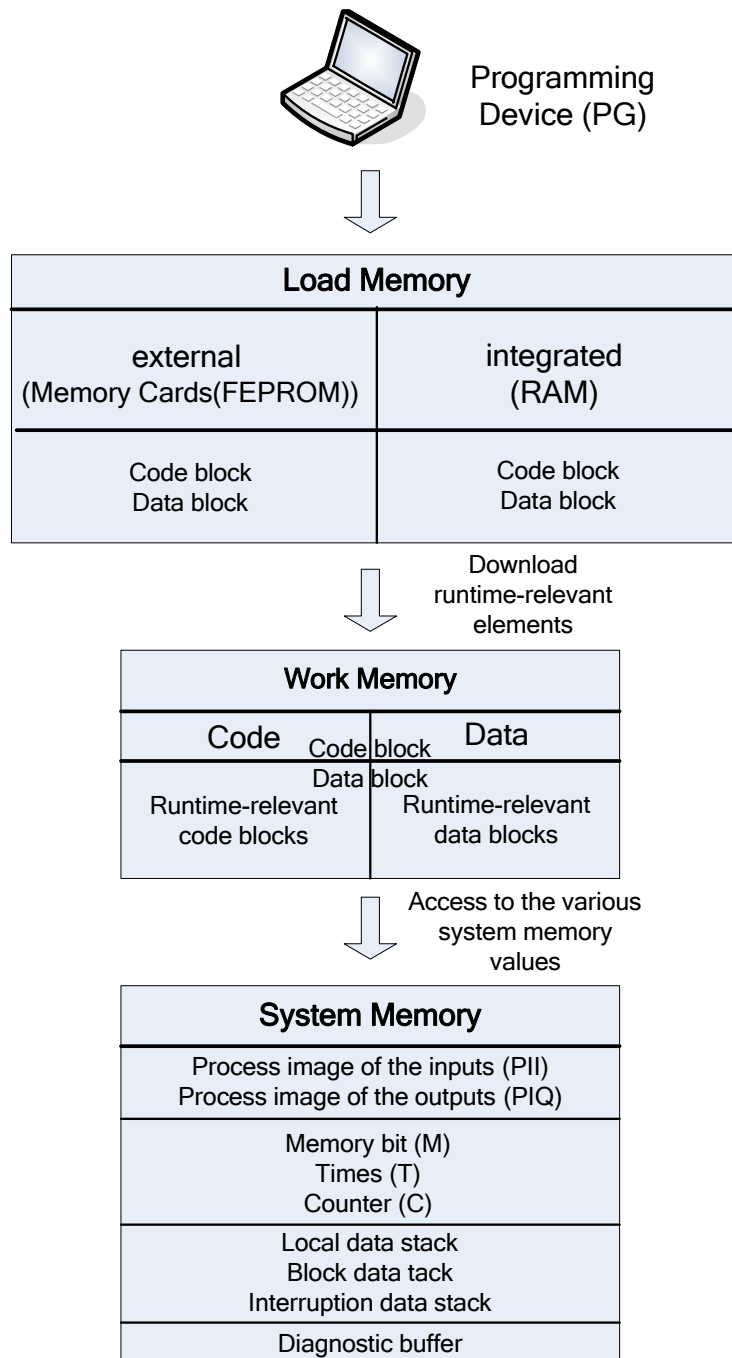
The CPUs can keep part of the data volume retentive independent of the battery. A buffer battery needs only be used if you wish to keep an exceeding data volume retentive. This also applies for CPUs (e.g. 312 IFM), for which no buffer battery can be used.

3 SIMATIC S7-300 CPUs and C7 Devices with Slot for an MC

3.1 Graphic display of the storage concept.

This figure shows the storage concept for S7-300 CPUs and C7 devices with MC.

Figure 2: SIMATIC S7-300, with memory card



3.2 Load memory

The operation of SIMATIC S7-300 CPUs and C7 devices with slot for a Memory Card is also possible without MC.

Location of load memory

The load memory is located internally within the CPU and externally on the MC.

Additional use of the load memory

Additionally, the complete configuration data of a project can be filed on the MC.

Setup of load memory and program buffer

The integrated load memory is a RAM memory. The external memory (MC) is a memory card with FEPRAM memory.

The user program in the internal RAM load memory is buffered via the buffer battery.

Loading the program network failsafe load memory

The program is transferred directly into the internal RAM using the programming device.

Copying the program to the MC is not possible with all CPUs. If necessary, a specific prommer (e.g. SIMATIC USB prommer 6ES7 792-0AA00-XA0) must be used. If the user program is stored on the MC, then it is retained during POWER OFF of the CPU, even without buffer battery.

Depending on the CPU operation from the memory card (MC or MMC)

Loading of user programs and operating the CPU is also possible without MC.

Expansion options of the load memory

If a larger load memory is required, then a larger MC must be used.

Exchanging the memory card during POWER OFF

If during POWER OFF (CPU buffered via buffer battery) an MC is pulled out and an MC with identical content plugged back in, then the CPU returns to the state it had before the POWER OFF, which is RUN or STOP. If during POWER OFF another MC with different content is plugged in, the CPU goes to STOP after POWER OFF and requests a memory reset. Keeping the mode switch pressed in "MRES" position executes the memory reset. After switching the CPU to RUN, the process relevant program parts are transferred from the memory card into the main memory for program initialization. If the MC contains a user program for a different CPU type, the CPU goes back to STOP.

Note Plugging the memory card in and out during RUN mode is not permitted.

3.3 Main memory

STEP 7 function "Load user program to Memory Card"

The function `Load user program to Memory Card` performs a memory reset, the user program is loaded to the MC, and then the process relevant code and data blocks are loaded from the MC into the main memory of the CPU.

STEP 7 function "Load"

During the Load function, the selected code and data blocks are transferred to the internal RAM load memory, and from there, if process relevant, they are written to the main memory.

Retentivity of the data blocks

A battery buffer can keep all data blocks retentive. The CPU can keep a part of the data volume retentive without battery (`Settings in HW Konfig -> CPU -> Properties -> Retentive Memory`). A buffer battery needs only be used if you wish to keep an exceeding data volume retentive.

Note: A buffer battery cannot be used with the CPU 312-IFM.

Expanding the main memory

The main memory is integrated in the CPU and cannot be expanded. If a larger main memory is required, the user must use a different CPU with larger main memory.

Note If you wish to execute the STEP 7 function `Copy RAM to ROM ..`, the current values of the process relevant data blocks in the load memory are overwritten with the current values from the main memory. If the process relevant data blocks are then transferred back to the main memory (e.g. after memory reset), then the new current values from the load memory are adopted by the CPU as initial values. In SIMATIC STEP 7 these new initial values are displayed in the "Actual value" column.

3.4 Application of the buffer battery

For the CPUs, buffering is performed via a buffer battery, depending on CPU type.

The battery only buffers data and time. Therefore, when using a battery, the CPU behaves as in unbuffered mode.

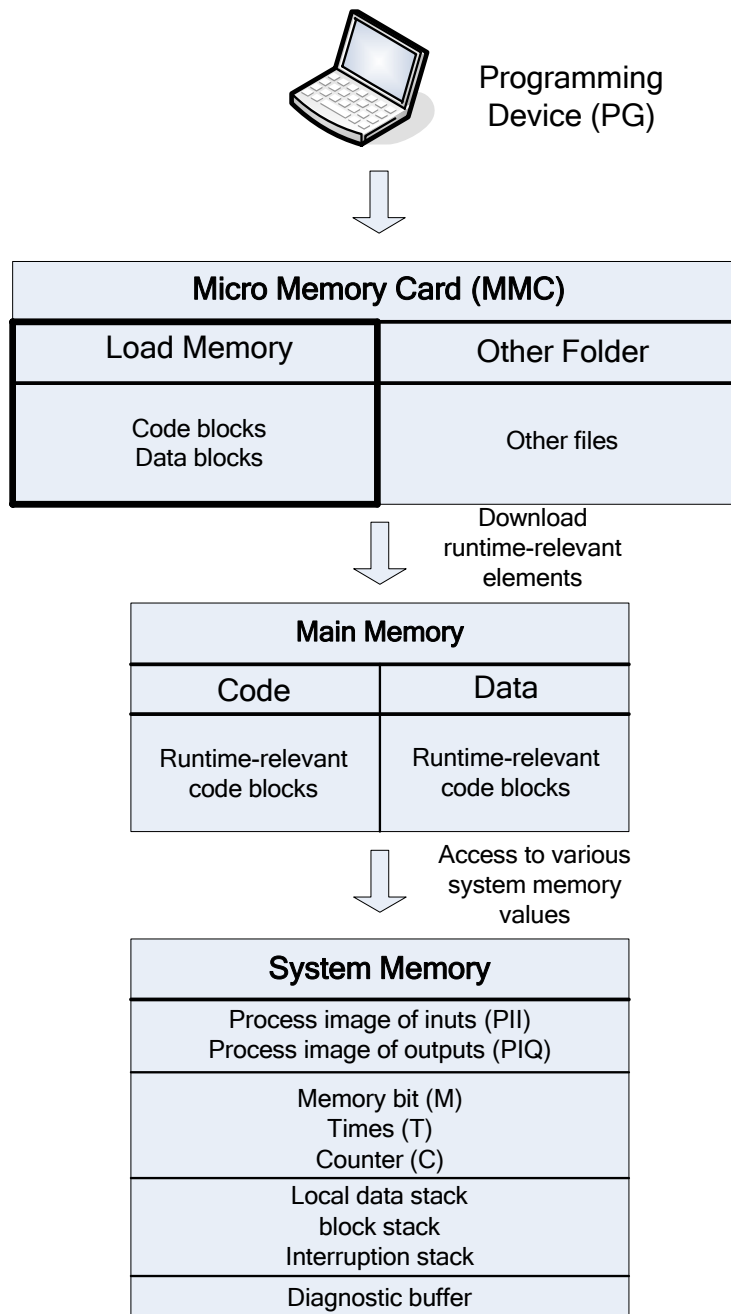
The CPUs can keep part of the data volume retentive independent of the battery. A buffer battery needs only be used if you wish to keep an exceeding data volume retentive.

4 SIMATIC S7-300 CPUs and C7 Devices with Slot for an MMC

4.1 Graphic display of the storage concept.

This figure shows the storage concept for S7-300 CPUs and C7 devices with MMC.

Figure 3: SIMATIC S7-300, with MMC memory card



4.2 Load memory

The operation of "SIMATIC S7-300 CPUs and C7 devices with slot for an MMC" is also possible without MMC.

Location of load memory

The load memory is located on the MMC and corresponds precisely to the size of the MMC.

Additional use of the load memory

Additionally, the complete configuration data of a project can be filed on the MMC.

Setup of load memory and program buffer

The MMC is an NFLASH. The program is therefore always retentive in the load memory: During loading, it is already stored network and reset failsafe on the MMC.

Loading the program network failsafe load memory

The program is written to the MMC using the programming device.

Depending on the CPU operation from the memory card (MC or MMC)

Loading of user programs, hence operation of the CPU, is only possible in conjunction with a SIMATIC Micro Memory Card (MMC).

Expansion options of the load memory

If a larger load memory is required, then a larger MMC must be used.

Exchanging the memory card during POWER OFF

If during POWER OFF an MMC is pulled out, and a different MMC plugged in, then (after NETWORK ON) the CPU performs a memory reset and goes to STOP mode. This behavior of the CPU is independent of the content (new or identical content) of the MMC.



Plugging in an MMC with a user program for a different CPU, might disconnect you from the CPU for as long as the MMC stays in the slot. In this case you must delete the user program from the MMC before using the MMC.



Unplugging the MMC during RUN mode is not permitted, as this may produce inconsistent data on the MMC!

4.3 Main memory

STEP 7 function "Load user program to Memory Card"

The function Load user program to Memory Card loads the entire user program to the MMC. Previous contents on the MMC are deleted. Then, process relevant code and data blocks are loaded from the MMC into the main memory.

STEP 7 function "Load"

The "Load" function transfers selected code and data blocks to the MMC (load memory). After loading a process relevant block, its contents are transferred to the main memory and activated. Non-process relevant blocks are only loaded to the load memory.

Retentivity of the data blocks

The main memory is not completely retentive for all CPUs. For some CPU types part of the main memory is retentive and the other part is **non**-retentive.

Only the retentive part of the main memory can be used for retentive data blocks.

Expanding the main memory

The main memory is integrated in the CPU and cannot be expanded. If a larger main memory is required, the user must use a different CPU with larger main memory.

Note If you wish to execute the STEP 7 function `Copy RAM to ROM ...`, the current values of the process relevant data blocks in the load memory are overwritten with the current values from the main memory. If the process relevant data blocks are then transferred back to the main memory (e.g. after memory reset), then the new current values from the load memory are adopted by the CPU as initial values. In SIMATIC STEP 7 these new initial values are displayed in the "Actual value" column.

4.4 Application of the buffer battery

The CPUs have a maintenance-free retentive memory. This means they do not require a buffer battery for operation. The content of a retentive memory remains after POWER OFF and restart (warm start).

5 The Storage Concept for SIMATIC S7-300 CPU Types and for C7 Device Types in Detail

In the following table you can see which storage concept exists for a specific CPU type or a C7 device type. The tables contain information on whether the CPU types and C7 devices support the “Non-Retain” data block property.

5.1 The storage concept of individual SIMATIC S7-300 CPU types

Table 1 and Table 2 gives you the SIMATIC S7-300 CPU types and the integrated storage concepts. For both CPU types in Table 1 the data block property “Non-Retain” is **not** supported.

Table 1: The data block property “Non-Retain” is **not** supported for these CPU types!

SIMATIC S7-300 CPU	Ordering number	Load memory	Non-Retain support
CPU 312IFM, 6kB, 0.7ms/kAW	6ES7312-5AC0x-0AB0	RAM and EEPROM integrated	no
CPU 312IFM, 6kB, 0.7ms/kAW	6ES7312-5AC8x-0AB0	RAM and EEPROM integrated	no
CPU 313, 12 kB, 0.7 ms/kAW	6ES7313-1AD0x-0AB0	Memory Card (MC)	no
CPU 314, 24 kB, 0.3ms/kAW	6ES7314-1AE0x-0AB0	Memory Card (MC)	no
CPU 314, 24 kB, 0.3 ms/kAW	6ES7314-1AE8x-0AB0	Memory Card (MC)	no
CPU 314 IFM for S7-300	6ES7318-2AJ00-0AB0	RAM and FEPR0M integrated	no
CPU 314 IFM with slot for MC	6ES7314-5AE10-0AB0	Memory Card	no
CPU 314 IFM, 32 KB, extended temperature range	6ES7314-5AE8x-0AB0	RAM and FEPR0M integrated	no
CPU 315, 48 kB, 0.3 ms/kAW	6ES7315-1AF0x-0AB0	Memory Card (MC)	no

Storage Concept for S7-300 CPUs and C7 Devices

Entry ID: 7302326

SIMATIC S7-300 CPU	Ordering number	Load memory	Non-Retain support
CPU 315-1, 48 kB, 1024 I/O	6ES7315-1AF03-0AB0	Memory Card (MC)	no
CPU 315-2 DP, 48 kB, 0.3 ms/kAW	6ES7315-2AF00-0AB0	Memory Card (MC)	no
CPU 315-2 DP, 48 kB, 0.3 ms/kAW	6ES7315-2AF01-0AB0	Memory Card (MC)	no
CPU 315-2 DP, 64 kB, 0.3 ms/kAW	6ES7315-2AF02-0AB0	Memory Card (MC)	no
CPU 315-2 DP, 64 kB, 0.3 ms/kAW	6ES7315-2AF03-0AB0	Memory Card (MC)	no
CPU 315-2 DP, 64 kB, 0.3 ms/kAW	6ES7315-2AF8x-0AB0	Memory Card (MC)	no
CPU 316, 128 kB, 0.3 ms/kAW	6ES7316-1AG00-0AB0	Memory Card (MC)	no
CPU 316-2DP, 128kB, 0.3 ms/kAW	6ES7316-2AG00-0AB0	Memory Card (MC)	no
CPU 315F, 128kB	6ES7315-6FF00-0AB0	Memory Card (MC)	no
Sector CPU 614, 128kB, 0.3ms	6ES7614-1AH0x-0AB3	Memory Card (MC)	no

Table 2: CPU types with Micro Memory Card (MMC) as load memory

SIMATIC S7-300 CPU	“Non-Retain” is not supported for the following order numbers	“Non-Retain” is not supported from following order numbers on	“Non-Retain” wird nicht unterstützt bei den Firmware-Versionen	“Non-Retain” wird unterstützt ab Firmware-Version
CPU 312C, 16 kB, 10DI / 6 DO onboard	6ES7312-5BD00-0AB0 up to 6ES7312-5BD01-0AB0		V1.0.0 up to V2.0.11	
CPU 312C, 32 kB, 10DI / 6 DO onboard		6ES7312-5BE03-0AB0		V2.0.12
CPU 313C, 32 kB, 24DI / 16DO, 4AI / 2AO onboard	6ES7313-5BE00-0AB0 up to 6ES7313-5BE01-0AB0		V1.0.0 up to V2.0.11	
CPU 313C, 64 kB, 24DI / 16DO, 4AI / 2AO onboardC		6ES7313-5BF03-0AB0		V2.0.12
CPU 313C-2 PtP, 32 kB, 16 DI / 16 DO; PtP-SS	6ES7313-6BE00-0AB0 up to 6ES7313-6BE01-0AB0		V1.0.0 up to V2.0.11	
CPU 313C-2 PtP, 64 kB, 16 DI / 16 DO; PtP-SS		6ES7313-6BF03-0AB0		V2.0.12
CPU313C-2 DP,32kB,16DI / 16DO;DP-SS M/S	6ES7313-6CE00-0AB0 up to 6ES7313-6CE01-0AB0		V1.0.0 up to V2.0.11	
CPU313C-2 DP,64 kB,16DI / 16DO;DP-SS M/S		6ES7313-6CF03-0AB0		V2.0.12
CPU314C-2 PtP,48kB, 24DI / 16DO / 4AI /2AO,PtP-SS	6ES7314-6BF00-0AB0 up to 6ES7314-6BF01-0AB0		V1.0.1 up to V2.0.11	
CPU314C-2 PtP,64kB, 24DI / 16DO / 4AI /2AO,PtP-SS	6ES7314-6BF02-0AB0		V2.0.10 up to V2.0.11	
CPU314C-2 PtP,96 kB, 24DI / 16DO / 4AI /2AO,PtP-SS		6ES7314-6BG03-0AB0		V2.0.12
CPU314C-2 DP,48kB,24DI / 16DO/ 4AI /	6ES7314-6CF00-0AB0 up to		V1.0.0 up to V2.0.11	

Storage Concept for S7-300 CPUs and C7 Devices

Entry ID: 7302326

SIMATIC S7-300 CPU	“Non-Retain” is not supported for the following order numbers	“Non-Retain” is not supported from following order numbers on	“Non-Retain” wird nicht unterstützt bei den Firmware-Versionen	“Non-Retain” wird unterstützt ab Firmware-Version
2AO,DP-SS M/S	6ES7314-6CF01-0AB0			
CPU314C-2 DP,64kB,24DI / 16DO/ 4AI / 2AO,DP-SS M/S	6ES7314-6CF02-0AB0		V2.0.10 up to V2.0.11	
CPU314C-2 DP,96kB,24DI / 16DO/ 4AI / 2AO,DP-SS M/S		6ES7314-6CG03-0AB0		V2.0.12
CPU 312, 16 kB, 0.2 ms/kAW	6ES7312-1AD10-0AB0		V2.0.0 up to V2.0.11	
CPU 312, 32 kB, 0.2 ms/kAW		6ES7312-1AE13-0AB0		V2.0.12
CPU 314, 48 kB, 0.1 ms/kAW	6ES7314-1AF10-0AB0		V2.0.0 up to V2.0.11	
CPU 314, 64 kB, 0.1 ms/kAW	6ES7314-1AF11-0AB0		V2.0.10 up to V2.0.11	
CPU 314, 96 kB, 0.1 ms/kAW		6ES7314-1AG13-0AB0		V2.0.12
CPU 315-2DP, 128 kB, 0.1 ms/kAW	6ES7315-2AG10-0AB0		V2.0.0 up to V2.0.11	V2.0.12
CPU 315-2 PN/DP, 128 kB, 0.1 ms/kAW		6ES7315-2EG10-0AB0		V2.3.1
CPU 315-2 PN/DP, 256 kB, 0.1 ms/kAW		6ES7315-2EH13-0AB0		V2.3.4
CPU 317-2DP, 512 kB, 0.05 ms/kAW		6ES7317-2AJ10-0AB0		V2.1.1
CPU 317-2 PN/DP, 512 kB, 0.05 ms/kAW		6ES7317-2EJ10-0AB0		V2.2.1
CPU 317-2 PN/DP, 1MB, 0.05 ms/kAW		6ES7317-2EK13-0AB0		V2.3.4
CPU 319-3PN/DP, 1400 kB		6ES7318-3EL00-0AB0		V2.4.0
CPU 315F-2 DP, 192 kB*	6ES7315-6FF01-0AB0		V2.0.0 up to V2.0.11	V2.0.12

SIMATIC S7-300 CPU	“Non-Retain” is not supported for the following order numbers	“Non-Retain” is not supported from following order numbers on	“Non-Retain” wird nicht unterstützt bei den Firmware-Versionen	“Non-Retain” wird unterstützt ab Firmware-Version
CPU 315F-2 PN/DP, 192 kB*		6ES7315-2FH10-0AB0		V2.3.3
CPU 317F-2 DP, 512 kB, 0.1 ms/kAW*		6ES7317-6FF00-0AB0		V2.1.1
CPU 317F-2 DP, 1024kB*		6ES7317-6FF03-0AB0		V2.1.10
CPU 317F-2 PN/DP, 512 kB*		6ES7317-2FJ10-0AB0		V2.3.3
CPU 317F-2 PN/DP, 1024kB*		6ES7317-2FK13-0AB0		V2.3.4
CPU 315T-2 DP, 128 kB, 0.1 ms/kAW		6ES7315-6TG10-0AB0		V2.3.1
CPU 317T-2 DP, 512 kB, 0.1 ms/kAW		6ES7317-6TJ10-0AB0		V2.1.1

*) The behavior of the CPUs for DBs and F-DBs are not equal.

5.2 The storage concept of the individual C7 device types

Table 3 and Table 4 gives you the C7 types and the integrated storage concepts. For both CPU devices in Table 3 the data block property “Non-Retain” is **not** supported.

Comment

For devices where the load memory is described as “integrated”, the load memory is integrated in the CPU and not expandable. The load memory then consists of a RAM part and a FEPRM part.

Table 3: The data block property “Non-Retain” is **not** supported for these CPU types!

C7 device	Ordering number	Load memory	Non-Retain support
SIMATIC C7-621, control system	6ES7621-1AD0x-0AE3	integrated	no
SIMATIC C7-621 ASi, control system	6ES7621-6BD0x-0AE3	integrated	no
SIMATIC C7-623, control system	6ES7623-1AE0x-0AE3	integrated	no
SIMATIC C7-623/A, control system	6ES7623-1CE0x-0AE3	integrated	no
SIMATIC C7-623/P, control system	6ES7623-1DE01-0AE3	integrated	no
SIMATIC C7-624, control system	6ES7624-1AE0x-0AE3	integrated	no
SIMATIC C7-624/P, control system	6ES7624-1DE01-0AE3	integrated	no
SIMATIC C7-626, control system	6ES7626-1AG0x-0AE3	integrated	no
SIMATIC C7-626/A, control system	6ES7626-1CG0x-0AE3	integrated	no
SIMATIC C7-626/P, control system	6ES7626-1DG0x-0AE3	integrated	no
SIMATIC C7-626 DP control system	6ES7626-2AG0x-0AE3	integrated	no
SIMATIC C7-626/A DP, control system	6ES7626-2CG0x-0AE3	integrated	no
SIMATIC C7-626/P DP, control system	6ES7626-2DG0x-0AE3	integrated	no
SIMATIC C7-633/P, control system	6ES7633-1DF0x-0AE3	Memory Card (MC)	no
SIMATIC C7-633 DP, control system	6ES7633-2BF0x-0AE3	Memory Card (MC)	no
SIMATIC C7-633/P DP, control system	6ES7633-2DF00-0AE3	Memory Card (MC)	no
SIMATIC C7-634/P, control system	6ES7634-1DF0x-0AE3	Memory Card (MC)	no
SIMATIC C7-634 DP, control system	6ES7634-2BF0x-0AE3	Memory Card (MC)	no
SIMATIC C7-634/P DP, control system	6ES7634-2DF00-0AE3	Memory Card (MC)	no

Table 4: CPU devices with Micro Memory Card (MMC) as load memory

C7 devices	“Non-Retain” is not supported for the following order numbers	“Non-Retain” is not supported from following order numbers on	“Non-Retain” is not supported for the firmware versions	“Non-Retain” is not supported from the following firmware versions on
C7-613	6ES7613-1CA00-0AE3 up to 6ES7613-1CA01-0AE3		V1.0.4 up to V2.0.11	
		6ES7613-1CA02-0AE3		V2.0.12
C7-635 Touch	6ES7635-2EB00-0AE3 up to 6ES7635-2EB01-0AE3		V1.0.1 up to V2.0.11	
		6ES7635-2EB02-0AE3		V2.0.12
C7-635 Key	6ES7635-2EC00-0AE3 up to 6ES7635-2EC01-0AE3		V1.0.3 up to V2.0.11	
		6ES7635-2EC02-0AE3		V2.0.12
C7-636 Touch	6ES7636-2EB00-0AE3*		V2.0.8 up to V2.0.11	V2.0.12
C7-636 Key	6ES7636-2EC00-0AE3*		V2.0.7 up to V2.0.11	V2.0.12

* Whether the data block property “Non-Retain” is supported, depends on the firmware version. The order number was not changed during the improvement of the firmware.