SIMATIC S7-200
Quick Reference Card

Interrupts			
Event Number	**Interrupt Description**	**Priority Group**	**Priority in Group**
8	Port 0: Receive character	Communications (highest)	0
9	Port 0: Transmit complete		0
23	Port 0: Receive message complete		0
24	Port 1: Receive message complete		1
25	Port 1: Receive character		1
26	Port 1: Transmit complete		1
19	PT0 0 complete interrupt	Discrete (middle)	0
20	PT0 1 complete interrupt		1
0	Rising edge, I0.0		2
2	Rising edge, I0.1		3
4	Rising edge, I0.2		4
6	Rising edge, I0.3		5
1	Falling edge, I0.0		6
3	Falling edge, I0.1		7
5	Falling edge, I0.2		8
7	Falling edge, I0.3		9
12	HSC0 CV=PV (current value = preset value)		10
27	HSC0 direction changed		11
28	HSC0 external reset		12
13	HSC1 CV=PV (current value=preset value)		13
14	HSC1 direction input changed		14
15	HSC1 external reset		15
16	HSC2 CV= PV		16
17	HSC2 direction changed		17
18	HSC2 external reset		18
32	HSC3 CV=PV (current value=preset value)		19
29	HSC4 CV=PV (current value=preset value)		20
30	HSC4 direction changed		21
31	HSC4 external reset		22
33	HSC5 CV=PV (current value = preset value)		23
10	Timed interrupt 0	Timed (lowest)	0
11	Timed interrupt 1		1
21	Timer T32 CT= PT interrupt		2
22	Timer T96 CT=PT interrupt		3

Special Memory Bits			
SM0.0	Always On	SM1.0	Result of operation = 0
SM0.1	First Scan	SM1.1	Overflow or illegal value
SM0.2	Retentive data lost	SM1.2	Negative result
SM0.3	Power up	SM1.3	Division by 0
SM0.4	30 s off / 30 s on	SM1.4	Table full
SM0.5	0.5 s off / 0.5 s on	SM1.5	Table empty
SM0.6	Off 1 scan / on 1 scan	SM1.6	BCD to binary conversion error
SM0.7	Switch in RUN position	SM1.7	ASCII to HEX conversion error

High-Speed Counter Modes								
Mode	**HSC0**			**HSC3**	**HSC4**			**HSC5**
	I0.0	**I0.1**	**I0.2**	**I0.1**	**I0.3**	**I0.4**	**I0.5**	**I0.4**
0	Clk			Clk	Clk			Clk
1	Clk		Reset		Clk		Reset	
3	Clk	Direction			Clk	Direction		
4	Clk	Direction	Reset		Clk	Direction	Reset	
6	Clk Up	Clk Dwn			Clk Up	Clk Dwn		
7	Clk Up	Clk Dwn	Reset		Clk Up	Clk Dwn	Reset	
9	Phase A	PhaseB			PhaseA	Phase B		
10	Phase A	PhaseB	Reset		PhaseA	Phase B	Reset	
Mode	**HSC1**				**HSC2**			
	I0.6	**I0.7**	**I1.0**	**I1.1**	**I1.2**	**I1.3**	**I4.4**	**I1.5**
0	Clk				Clk			
1	Clk		Reset		Clk		Reset	
2	Clk		Reset	Start	Clk		Reset	Start
3	Clk	Direction			Clk	Direction		
4	Clk	Direction	Reset		Clk	Direction	Reset	
5	Clk	Direction	Reset	Start	Clk	Direction	Reset	Start
6	Clk Up	Clk Dwn			Clk Up	Clk Dwn		
7	Clk Up	Clk Dwn	Reset		Clk Up	Clk Dwn	Reset	
8	Clk Up	Clk Dwn	Reset	Start	Clk Up	Clk Dwn	Reset	Start
9	Phase A	Phase B			Phase A	Phase B		
10	Phase A	Phase B	Reset		Phase A	Phase B	Reset	
11	Phase A	Phase B	Reset	Start	Phase A	Phase B	Reset	Start

Description	**Range Limit**				**Accessible as...**			
	CPU 221	**CPU 222**	**CPU 224**	**CPU 226**	**Bit**	**Byte**	**Word**	**DWord**
User program size	2 Kwords	2 Kwords	4 Kwords	4 Kwords				
User data size	1 Kwords	1 Kwords	2.5 Kwords	2.5 Kwords				
Process-image input register	I0.0 to I15.7	I0.0 to I15.7	I0.0 to I15.7	I0.0 to I15.7	Ix.y	IBx	IWx	IDx
Process-image output register	Q0.0 to Q15.7	Q0.0 to Q15.7	Q0.0 to Q15.7	Q0.0 to Q15.7	Qx.y	QBx	QWx	QDx
Analog inputs (read only)	—	AIW0 to AIW30	AIW0 to AIW62	AIW0 to AIW62			AIWx	
Analog outputs (write only)	—	AQW0 to AQW30	AQW0 to AQW62	AQW0 to AQW62			AQWx	
Variable memory (V)[1]	V0.0 to V2047.7	V0.0 to V2047.7	V0.0 to V5119.7	V0.0 to V5119.7	Vx.y	VBx	VWx	VDx
Local Memory (L)[2]	L0.0 to L63.7	L0.0 to L63.7	L0.0 to L63.7	L0.0 to L63.7	Lx.y	LBx	LWx	LDx
Bit Memory (M)	M0.0 to M31.7	M0.0 to M31.7	M0.0 to M31.7	M0.0 to M31.7	Mx.y	MBx	MWx	MDx
Special Memory (SM) Read only	SM0.0 to SM179.7 SM0.0 to SM29.7	SM0.0 to SM299.7 SM0.0 to SM29.7	SM0.0 to SM299.7 SM0.0 to SM29.7	SM0.0 to SM299.7 SM0.0 to SM29.7	SMx.y	SMBx	SMWx	SMDx
Timers Retentive on-delay 1 ms Retentive on-delay 10 ms Retentive on-delay 100 ms On/Off delay 1 ms On/Off delay 10 ms On/Off delay 100 ms	256 (T0 to T255) T0, T64 T1 to T4, T65 to T68 T5 to T31, T69 to T95 T32, T96 T33 to T36, T97 to T100 T37 to T63, T101 to T255	256 (T0 to T255) T0, T64 T1 to T4, T65 to T68 T5 to T31, T69 to T95 T32, T96 T33 to T36, T97 to T100 T37 to T63,T101 to T255	256 (T0 to T255) T0, T64 T1 to T4, T65 to T68 T5 to T31, T69 to T95 T32, T96 T33 to T36, T97 to T100 T37 to T63,T101 to T255	256 (T0 to T255) T0, T64 T1 to T4, T65 to T68 T5 to T31, T69 to T95 T32, T96 T33 to T36, T97 to T100 T37 to T63, T101 to T255	Tx		Tx	
Counters	C0 to C255	C0 to C255	C0 to C255	C0 to C255	Cx		Cx	
High-speed counter	HC0, HC3, HC4, HC5	HC0, HC3, HC4, HC5	HC0 to HC5	HC0 to HC5				HCx
Sequential control relays (S)	S0.0 to S31.7	S0.0 to S31.7	S0.0 to S31.7	S0.0 to S31.7	Sx.y	SBx	SWx	SDx
Accumulator registers	AC0 to AC3	AC0 to AC3	AC0 to AC3	AC0 to AC3		ACx	ACx	ACx
Jumps/Labels	0 to 255	0 to 255	0 to 255	0 to 255				
Calls/Subroutines	0 to 63	0 to 63	0 to 63	0 to 63				
Interrupt routines	0 to 127	0 to 127	0 to 127	0 to 127				
PID loops	0 to 7	0 to 7	0 to 7	0 to 7				
Port	Port 0	Port 0	Port 0	Port 0, Port 1				

[1] All V memory can be saved to permanent memory. [2] LB60 to LB63 are reserved by STEP 7–Micro/WIN 32, version 3.0 or later.

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Boolean Instructions			
LD	N	Load	9-2
LDI	N	Load Immediate	9-3
LDN	N	Load Not	9-2
LDNI	N	Load Not Immediate	9-3
A	N	AND	9-2
AI	N	AND Immediate	9-3
AN	N	AND Not	9-2
ANI	N	AND Not Immediate	9-3
O	N	OR	9-2
OI	N	OR Immediate	9-3
ON	N	OR Not	9-2
ONI	N	OR Not Immediate	9-3
LDBx	N1, N2	Load result of Byte Compare N1(x:<,<=,=,>,>=, or <>)	9-10
ABx	N1, N2	AND result of Byte Compare N1(x: <,<=,=,>,>=, or <>) N2	9-10
OBx	N1, N2	OR result of Byte Compare N1(x: <,<=,=,>,>=, or <>) N2	9-10
LDWx	N1, N2	Load result of Word Compare N1(x: <,<=,=,>,>=, or <>) N2	9-11
AWx	N1, N2	AND result of Word Compare N1 (x: <,<=,=,>,>=, or <>) N2	9-11
OWx	N1, N2	OR result of Word Compare N1 (x: <,<=,=,>,>=, or <>) N2	9-11
LDDx	N1, N2	Load result of DWord Compare N1 (x: <,<=,=,>,>=, or <>) N2	9-12
ADx	N1, N2	AND result of DWord Compare N1(x: <,<=,=,>,>=, or <>) N2	9-12
ODx	N1, N2	OR result of DWord Compare N1(x: <,<=,=,>,>=, or <>) N2	9-12
LDRx	N1, N2	Load result of Real Compare N1 (x: <,<=,=,>,>=, or <>) N2	9-13
ARx	N1, N2	AND result of Real Compare N1 (x: <,<=,=,>,>=, or <>) N2	9-13
ORx	N1, N2	OR result of Real Compare N1 (x: <,<=,=,>,>=, or <>) N2	9-13
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–D	IN1, OUT		9-74
–R	IN1, OUT	OUT–IN1=OUT	9-82
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*R	IN1, OUT		9-83
*D	IN1, OUT		9-76
*I	IN1, OUT	IN1 * OUT = OUT	9-75
DIV	IN1, OUT	Divide Integer or Real	9-77
/R	IN1, OUT	OUT / IN1 = OUT	9-83
/D	IN1, OUT		9-76
/I	IN1, OUT		9-75
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