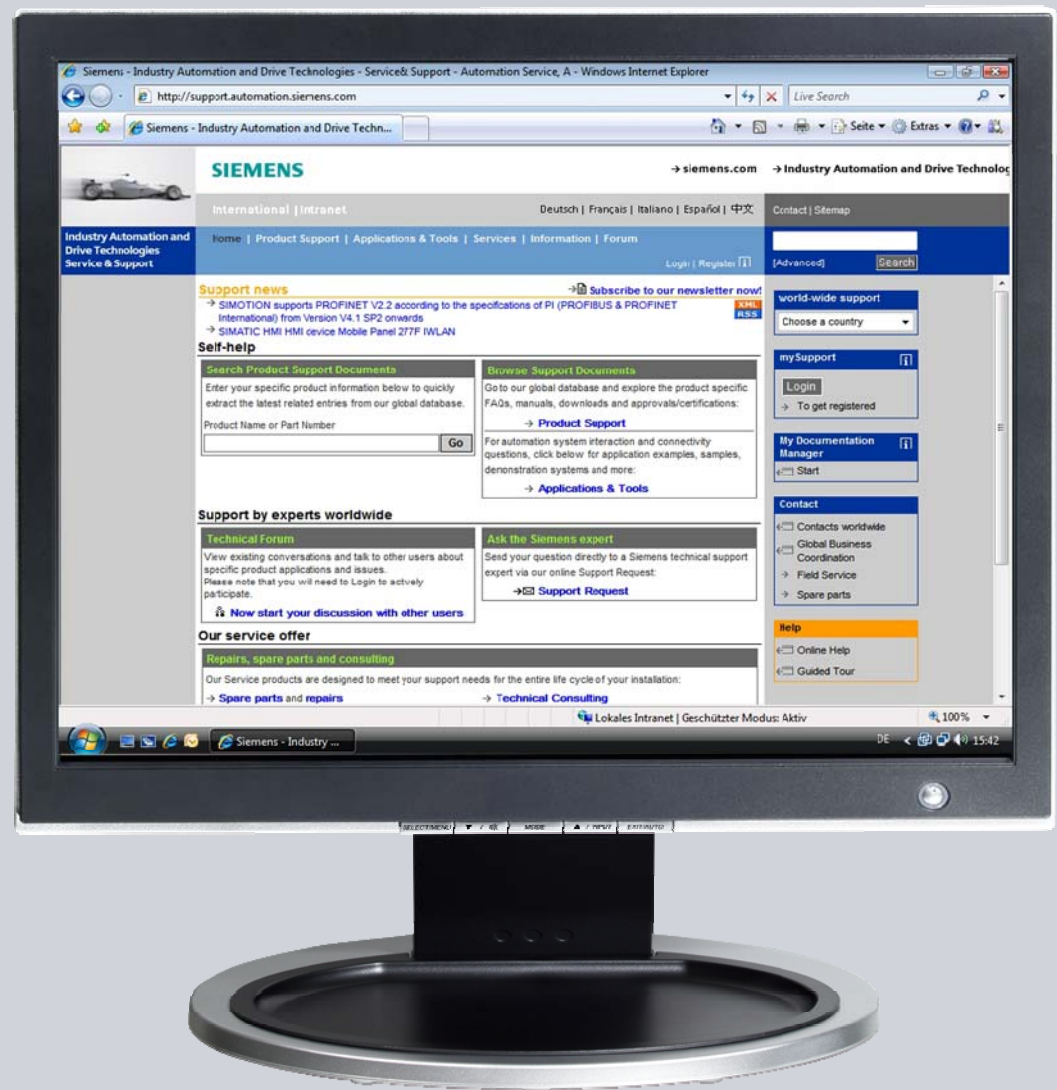


How many high-speed counters (HSCs) are provided by the SIMATIC S7-1200 PLC?

SIMATIC S7-1200

FAQ • March 2010



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Question

How many high-speed counters (HSCs) are provided by the SIMATIC S7-1200 PLC?

Answer

In chapter 1.1 you will get information about the dependency of S7-1200 high-speed counters.

In chapter 1.2 you will get an overview about how to select the right S7-1200 hardware to solve your high-speed counting task (with example).

Table of content

1	SIMATIC S7-1200 High-Speed Counter	4
1.1	Hardware	4
	Type of counting	4
1.1.1	Inputs	4
	Operating phase	5
1.1.2	Outputs	6
1.1.3	Frequency	7
1.2	Summary	8
1.2.1	Example	8

1 SIMATIC S7-1200 High-Speed Counter

1.1 Hardware

With the SIMATIC S7-1200 PLC you can use up to 6 high-speed counters.

The number of high-speed counters that you can use depends upon which CPU you use:

Table 1-1

CPU	Max. number of HSCs without signal boards
1211C	3 (HSC_1, HSC_2, HSC_3)
1212C	4 (HSC_1, HSC_2, HSC_3, HSC_4)
1214C	6 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5, HSC_6)

For any CPU you can install one signal board (SB).

Depending on the combination of CPU with SB you can use the following HSCs:

Table 1-2

CPU	SB 1223 2DI/2DO	SB 1223 2DI/2DO 200kHz	SB 1221 4DI 200kHz	SB 1222 4DO 200kHz
1211C	4 (HSC_1, HSC_2, HSC_3, HSC_5)	4 (HSC_1, HSC_2, HSC_3, HSC_5)	5 (HSC_1, HSC_2, HSC_3, HSC_5, HSC_6)	3 (HSC_1, HSC_2, HSC_3)
1212C	5 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5)	5 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5)	6 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5, HSC_6)	4 (HSC_1, HSC_2, HSC_3, HSC_4)
1214C	6 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5, HSC_6)	6 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5, HSC_6)	6 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5, HSC_6)	6 (HSC_1, HSC_2, HSC_3, HSC_4, HSC_5, HSC_6)

Type of counting

You can choose between three types of counting:

- Counting (claims inputs and enables an external reset input)
- Frequency (claims inputs and disables an external reset input)
- Axis of motion (claims outputs for pulse train output (PTO) and claims HSC to count the pulses)

1.1.1 Inputs

For every HSC, at least one and up to three inputs will be claimed.

The maximum number of the claimed inputs depends on the type of counting

(“Counting” or “Frequency”) and the operating phase (SP = single phase or MP = multi-phase (two phase and AB Quadrature)).

Operating phase

Table 1-3

In-put	SP	MP		
	Single phase	Two phase	AB Quadrature 1X	AB Quadrature 4X
1.	CLK	CLK UP	CLK A	CLK A
2.	[DIR]	CLK DN	CLK B	CLK B
3.	[R]	[R]	[R]	[R]

NOTE

The 3rd input “[R]” is only available for the type of counting: “Counting”.

Legend

CLK = clock input
 [DIR] = optional external direction input
 [R] = optional external reset input
 CLK UP = clock up input
 CLK DN = clock down input
 CLK A = clock A input
 CLK B = clock B input

The HSCs claim the following CPU inputs (for type of counting: “Counting” or “Frequency”):

Table 1-4

	HSC_1	HSC_2	HSC_3	HSC_4	HSC_5	HSC_6
1.	I0.0	I0.2	I0.4	I0.6	I1.0	I1.3
2.	I0.1	I0.3	I0.5	I0.7	I1.1	I1.4
3.	I0.3	I0.1	I0.7	I0.5	I1.2	I1.5

NOTE

Claiming the 2nd and the 3rd input depends on Table 1-3.

The HSCs claim the following signal board inputs as selected (for type of counting: “Counting” or “Frequency”):

Table 1-5

	HSC_1	HSC_2	HSC_5	HSC_6
1.	I4.0	I4.2	I4.0	I4.0
2.	I4.1	I4.3	I4.1	I4.3
3.	I4.3	I4.1	I4.3	I4.1

NOTE

Claiming the 2nd and the 3rd input depends on Table 1-3.

Table 1-5 shows the maximum high-speed counter reservation for signal boards (SB 1221 DC 200 kHz 4xDI).

This signal board allows the use of two HSCs in groups (HSC_1/HSC_2, or HSC_5/HSC_6).

As you can see by the colored fields in Table 1-4 or Table 1-5, the first input (CLK, CLK UP, or CLK A) is unique, but the second input can overlap with the neighboring "Input 3. [R]". This also depends on the type of counting, the operating phase, and if you need the optional external direction/reset inputs.

1.1.2 Outputs

The S7-1200 CPUs have two pulse generators, which can be used as Pulse-width modulation (PWM) or pulse train output (PTO). To count the pulses in mode PTO (type of counting: Axis of motion) the pulse generators claim specific HSCs and digital outputs as shown in the following table:

Table 1-6

PTO (HSC)	Default output assignment		
	CPU or SB	Pulse	Direction
PTO 1 (HSC_1)	Onboard CPU	Q0.0	Q0.1
	Signal board	Q4.0	Q4.1
PTO 2 (HSC_2)	Onboard CPU	Q0.2	Q0.3
	Signal board	Q4.2	Q4.3

NOTE

If you configure high-speed counter HSC1 or HSC2 for other counting tasks, these cannot be used by pulse generator PTO1 or PTO2, respectively.

The S7-1200 CPUs with relay outputs are not recommended for PTO.

You can use these CPUs with one of the following signal boards with digital outputs:

- SB 1222 4 DO 200kHz
- SB 1223 2DI/2DO
- SB 1223 2DI/2DO 200kHz

1.1.3 Frequency

The maximum count and PTO frequency for the high-speed counters is shown in the following table:

Table 1-7

Max. frequency [kHz]		CPU	Signal boards			
High-speed counter	Operating phase	DI/DO	2DI/2DO	200 kHz		
				2DI/2DO	4DI	4DO
HSC_1	SP	100/100	30/20-	200/100	200	100
	MP	80/-	20/-	160/-	160	
HSC_2	SP	100/100			200	100
	MP	80/-			160	
HSC_3	SP	100/-				
	MP	80/-				
HSC_4	SP	30/-				
	MP	20/-				
HSC_5	SP	30/-	30/-	200/-	200	
	MP	20/-	20/-	160/-	160	
HSC_6	SP	30/-			200	
	MP	20/-			160	

Legend

SP = operating phase "single phase"

MP = "multi-phase" (operating phase "two phase" or "AB Quadrature")

frequency "x/y" = maximum input count frequency/ maximum PTO frequency (both in kHz)

Summary

1.2 Summary

In Figure 1-1 you will find an overview of the SIMATIC S7-1200 high-speed counters.

To show you how to handle the overview please have a look at the following example:

1.2.1 Example

Automation task

How many PLCs/Signal Boards are required to use

- 9 HSCs
- with A/B Quadrature and reset input
- (maximum frequency: 80kHz,
- logic 1 level: 24 VDC)?

CPU selection

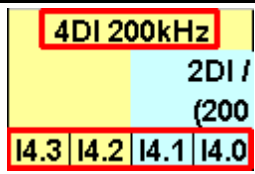
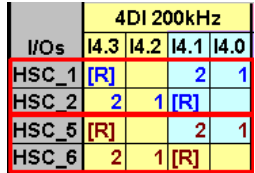
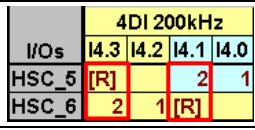
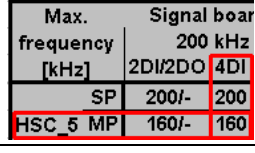
Table 1-8

CPU	Description	Picture	Selection																				
1.	The S7-1200 CPUs identify digital input voltage from 15 to 26 V as logic signal "1" (-> S7-1200 System Manual).		CPU 1211C, CPU 1212C, CPU 1214C																				
2.	3 HSCs are able to count up to 80 kHz in multi-phase mode (without signal boards).	<table border="1"> <thead> <tr> <th>Max. frequency [kHz]</th> <th>CPU DI/DO</th> </tr> </thead> <tbody> <tr> <td>SP</td> <td>100/100</td> </tr> <tr> <td>HSC_1 MP</td> <td>80/-</td> </tr> <tr> <td>SP</td> <td>100/100</td> </tr> <tr> <td>HSC_2 MP</td> <td>80/-</td> </tr> <tr> <td>SP</td> <td>100/-</td> </tr> <tr> <td>HSC_3 MP</td> <td>80/-</td> </tr> </tbody> </table>	Max. frequency [kHz]	CPU DI/DO	SP	100/100	HSC_1 MP	80/-	SP	100/100	HSC_2 MP	80/-	SP	100/-	HSC_3 MP	80/-	HSC_1, HSC_2, HSC_3						
Max. frequency [kHz]	CPU DI/DO																						
SP	100/100																						
HSC_1 MP	80/-																						
SP	100/100																						
HSC_2 MP	80/-																						
SP	100/-																						
HSC_3 MP	80/-																						
3.	To count A/B Quadrature, you need three inputs (CLK A, CLK B, and R) per HSC. For HSC_1, the inputs overlap with HSC_2, therefore you can use only one of the two high-speed counters. -> We choose HSC_1.	<table border="1"> <thead> <tr> <th>I/Os</th> <th>I0.0</th> <th>I0.1</th> <th>I0.2</th> <th>I0.3</th> </tr> </thead> <tbody> <tr> <td>HSC_1</td> <td>1</td> <td>2</td> <td>[R]</td> <td></td> </tr> <tr> <td>HSC_2</td> <td></td> <td>[R]</td> <td>1</td> <td>2</td> </tr> </tbody> </table>	I/Os	I0.0	I0.1	I0.2	I0.3	HSC_1	1	2	[R]		HSC_2		[R]	1	2	HSC_1, HSC_3					
I/Os	I0.0	I0.1	I0.2	I0.3																			
HSC_1	1	2	[R]																				
HSC_2		[R]	1	2																			
4.	The onboard reset input for HSC_3 is only available with CPU 1212C or CPU 1214C. -> We choose CPU 1212C.	<table border="1"> <thead> <tr> <th>I/Os</th> <th colspan="4">CPU 1212C</th> </tr> <tr> <th></th> <th>U 1211C</th> <th></th> <th></th> <th></th> </tr> <tr> <th>I/Os</th> <th>I0.4</th> <th>I0.5</th> <th>I0.6</th> <th>I0.7</th> </tr> </thead> <tbody> <tr> <td>HSC_3</td> <td>1</td> <td>2</td> <td>[R]</td> <td></td> </tr> </tbody> </table>	I/Os	CPU 1212C					U 1211C				I/Os	I0.4	I0.5	I0.6	I0.7	HSC_3	1	2	[R]		CPU 1212C
I/Os	CPU 1212C																						
	U 1211C																						
I/Os	I0.4	I0.5	I0.6	I0.7																			
HSC_3	1	2	[R]																				

We choose CPU 1212C with HSC_1 and HSC_3.

SB selection

Table 1-9

SB	Description	Picture	Selection
1.	To count A/B Quadrature with external reset you need three inputs (CLK A, CLK B and R) per HSC. So you have to use a signal board with at least 3 inputs.		SB 1221 DC 200kHz 4xDI
2.	SB 1221 DC 200 kHz 4xDI can be used in groups (HSC_1 and HSC_2, or HSC_5 and HSC_6). -> We choose HSC_5 and HSC_6.		HSC_5, HSC_6
3.	For HSC_5 the SB inputs overlap with HSC_6; therefore you can use only one of them. -> We choose HSC_5.		HSC_5
4.	With the SB 1221 DC 200 kHz 4xDI, you can count up to 160 kHz in multi-phase mode.		
5.	The SB 1221 DC 200 kHz 4xDI is available with 5V or 24V signal input. -> We choose SB 1221, 4DI, 24VDC 200 kHz.		SB 1221, 4DI, 24VDC 200kHz

We choose SB 1221, 4DI, 24VDC 200 kHz with HSC_5.

Result

You can choose CPU 1212C or CPU1214C with an SB 1221, 4DI, 24VDC 200 kHz to use 3 HSCs to count 3 A/B Quadratures with reset input (maximum frequency: 80 kHz, logic 1 level: 24 VDC).

Thus, you need 3 CPUs with an SB1221 each to solve the automation task.

