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Preface

1.1 Preface

Purpose of this manual

This manual represents a useful reference and contains information on operator inputs, descriptions of functions, and technical specifications of the S7-400H CPUs.

For information on installing and wiring these and other modules in order to set up an S7-400H system, refer to the S7-400 Automation System, Installation manual.

Changes compared to the previous version

The following changes have been made in relation to the previous version of this manual, SIMATIC High Availability Systems, Edition 11/2011 (A5E00267693-09):

- The firmware of the CPUs 41x-5H PN/DP has version 6.0
- The CPUs 41x-5H PN/DP feature a PROFINET interface
- CPU 416-5H has been added.
- Know-How protection through access-protected blocks (S7 Block Privacy)
- New protection mechanism "signed firmware update" as of STEP7 V5.5 SP2 HF1
- Increase of communication performance
- Reduction of processing times
- Adaptation of work memory and additional quantity frameworks to the CPUs 41x-3 PN/DP V6.0
- You can implement a programmed master-reserve switchover using SFC 90 "H_CTRL".

Differences in system behavior between versions 4.5 and 6.0

- A user program that uses SFC 87 to read out the current connection status and that was written for a H-CPU V4.x does not return any data on an H-CPU V6.0. The reason is that the quantity Framework expanded to 120 connections also requires a larger target range in the program. You must adapt the program accordingly.
- A reserve CPU can take over the role of master at startup, see chapter STARTUP mode (Page 125).
- In large configurations with many CPs and/or external DP masters it may take up to 30 seconds until a requested restart is performed in the buffered POWER ON mode of the H-CPU V 6.0, see chapter STARTUP mode (Page 125).
- In contrast to OB 84, the reason for the call is not entered in the start information of OB 82, see chapter Synchronization modules for S7-400H (Page 323).
Preface

1.1 Preface

- Extended cycle time in case of long synchronization lines, see chapter Synchronization modules for S7-400H (Page 323).
- If you use long synchronization lines, you have to extend the monitoring time of the connection at an H-CPU V6.0, see chapter Communication via fault-tolerant S7 connections (Page 232).
- The startup time of the CPU at power on, the loading time of blocks, as well as the startup after a plant modification at runtime can be significantly prolonged by encrypted blocks; see chapter Access-protected blocks (Page 73).
- The following applies to PROFINET in the fault-tolerant system: The job must be repeated if it is rejected with return value W#16#80BA when using SFB 52/53/54.

Basic knowledge required

This manual requires general knowledge of automation engineering. Moreover, it is assumed that the readership has sufficient knowledge of computers or equipment similar to a PC, such as programming devices, running under the Windows XP, Windows Vista or Windows 7 operating system. An S7-400H is configured using the STEP 7 basic software, and you should thus be familiar in the handling of this basic software. This knowledge is provided in the Programming with STEP 7 manual.

In particular when operating an S7-400H system in potentially explosive atmospheres, you should always observe the information on the safety of electronic control systems provided in the appendix of the S7-400 Automation System, Installation manual.

Scope of the manual

The manual is relevant to the following components:
- CPU 412–5H; 6ES7 412–5HK06–0AB0 as of firmware V6.0
- CPU 414–5H; 6ES7 414–5HM06–0AB0 as of firmware V6.0
- CPU 416–5H; 6ES7 416–5HS06–0AB0 as of firmware V6.0
- CPU 417–5H; 6ES7 417–5HT06–0AB0 as of firmware V6.0

Approvals

For details on certifications and standards, refer to the S7-400 Automation System, Module Data manual, chapter 1.1, Standards and Certifications.
Further information

For more information on the topics covered in this manual, refer to the following manuals:


Online help

In addition to the manual, you will find detailed support on how to use the software in the integrated online help system of the software.

The help system can be accessed using various interfaces:

- The Help menu contains several commands: Table of contents opens the Help index. You will find help on H systems in Configuring H-Systems.
- Using Help provides detailed instructions on using the online help system.
- The context-sensitive help system provides information on the current context, for example, on an open dialog or active window. You can call this help by clicking "Help" or using the F1 key.
- The status bar provides a further form of context-sensitive help. It shows a short description of each menu command when you position the mouse pointer over a command.
- A short info text is also shown for the toolbar buttons when you hold the mouse pointer briefly over a button.

If you prefer to read the information of the online help in printed form, you can print individual topics, books or the entire help system.

Recycling and disposal

The S7-400H system contains environmentally compatible materials and can be recycled. For ecologically compatible recycling and disposal of your old device, contact a certificated disposal service for electronic scrap.
Additional support

If you have any questions relating to the products described in this manual, and do not find the answers in this documentation, please contact your Siemens partner at our local offices.

You will find information on who to contact at:

Contact partners [http://www.siemens.com/automation/partner]

A guide to the technical documents for the various SIMATIC products and systems is available at:


You can find the online catalog and order system under:

Catalog [http://mall.automation.siemens.com/]

Functional Safety Services

Siemens Functional Safety Services is a comprehensive performance package that supports you in risk assessment and verification all the way to plant commissioning and modernization. We also offer consulting services for the application of fail-safe and fault-tolerant SIMATIC S7 automation systems.

Additional information is available at:


Submit your requests to:

Mail Functional Safety Services [mailto:safety-services.industry@siemens.com]

Training center

We offer a range of relevant courses to help you to get started with the SIMATIC S7 automation system. Please contact your local training center or the central training center.

Training [http://www.sitrain.com/index_en.html]

Technical Support

For technical support of all Industry Automation products, fill in and submit the online Support Request:

Support Request [http://www.siemens.de/automation/support-request]

Service & Support on the Internet

In addition to our documentation, we offer a comprehensive online knowledge base on the Internet at:

Service & Support [http://www.siemens.com/automation/service&support]

There you will find:
• The newsletter containing the latest information on your products.
• The latest documents via our search function in Service & Support.
• A forum for global information exchange by users and specialists.
• Your local Automation representative.
• Information on field service, repairs and spare parts. Much more can be found under "Services".

See also

Technical Support [http://support.automation.siemens.com]
Security information

Siemens offers IT security mechanisms for its automation and drive product portfolio in order to support the safe operation of the plant/machine. We recommend that you inform yourself regularly on the IT security developments regarding your products. You can find information on this under: http://support.automation.siemens.com

You can register for a product-specific newsletter here.

For the safe operation of a plant/machine, however, it is also necessary to integrate the automation components into an overall IT security concept for the entire plant/machine, which corresponds to the state-of-the-art IT technology. You can find information on this at: http://www.siemens.com/industrialsecurity.

Products used from other manufacturers should also be taken into account here.
Fault-tolerant automation systems

2.1 Redundant SIMATIC automation systems

Operating objectives of redundant automation systems

Redundant automation systems are used in practice with the aim of achieving a higher degree of availability or fault tolerance.

![Redundant automation systems, e.g.]

<table>
<thead>
<tr>
<th>Fault-tolerant 1-out-of-2 systems</th>
<th>Fail-safe 1-out-of-2 systems</th>
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<td>Objective: Reduced risk of produc-</td>
<td>Objective: Protect life, the</td>
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<tr>
<td>tion loss by means of parallel</td>
<td>environment and investments</td>
</tr>
<tr>
<td>operation of two systems</td>
<td>by safely disconnecting to a secure</td>
</tr>
<tr>
<td></td>
<td>“off” position</td>
</tr>
</tbody>
</table>

Figure 2-1 Operating objectives of redundant automation systems

Note the difference between fault-tolerant and fail-safe systems. The S7–400H is a fault-tolerant automation system. You may only use it to control safety-related processes if you have programmed and configured it in accordance with the rules for F systems. You can find details in the following manual: SIMATIC Industrial Software S7 F/FH Systems [http://support.automation.siemens.com/WW/view/en/2201072]

Why fault-tolerant automation systems?

The purpose of using fault-tolerant automation systems is to reduce production downtimes, regardless of whether the failures are caused by an error/fault or are due to maintenance work.

The higher the costs of production stops, the greater the need to use a fault-tolerant system. The generally higher investment costs of fault-tolerant systems are soon recovered since production stops are avoided.
Fault-tolerant automation systems

2.2 Increasing the availability of plants

Redundant I/O

Input/output modules are termed redundant when they exist twice and they are configured and operated as redundant pairs. The use of redundant I/O provides the highest degree of availability, because the system tolerates the failure of a CPU or of a signal module. If you require a redundant I/O, you use the blocks of the "Functional I/O Redundancy" function block library, see section Connecting redundant I/O to the PROFIBUS DP interface (Page 171).

2.2 Increasing the availability of plants

The S7-400H automation system satisfies the high demands on availability, intelligence, and decentralization placed on modern automation systems. It also provides all functions required for the acquisition and preparation of process data, including functions for the open-loop control, closed-loop control, and monitoring of assemblies and plants.

System-wide integration

The S7-400H automation system and all other SIMATIC components such as the SIMATIC PCS7 control system are matched to one another. The system-wide integration, ranging from the control room to the sensors and actuators, is implemented as a matter of course and ensures maximum system performance.

Figure 2-2: Integrated automation solutions with SIMATIC
**Graduated availability by duplicating components**

The redundant structure of the S7-400H ensures requirements to reliability at all times. This means: all essential components are duplicated.

This redundant structure includes the CPU, the power supply, and the hardware for linking the two CPUs.

You yourself decide on any other components you want to duplicate to increase availability depending on the specific process you are automating.

**Redundancy nodes**

Redundant nodes represent the fail safety of systems with redundant components. A redundant node can be considered as independent when the failure of a component within the node does not result in reliability constraints in other nodes or in the overall system.

The availability of the overall system can be illustrated simply in a block diagram. With a 1-out-of-2 system, one component of the redundant node may fail without impairing the operability of the overall system. The weakest link in the chain of redundant nodes determines the availability of the overall system.

**No error/fault**

![Redundancy node with 1oo2 redundancy](image)

Figure 2-3 Example of redundancy in a network without error
With error/fault

The following figure shows how a component may fail without impairing the functionality of the overall system.

![Diagram of 1-out-of-2 redundancy system with error](image1)

**Figure 2-4** Example of redundancy in a 1-out-of-2 system with error

**Failure of a redundancy node (total failure)**

The following figure shows that the overall system is no longer operable, because both subunits have failed in a 1-out-of-2 redundancy node (total failure).

![Diagram of 1-out-of-2 redundancy system with total failure](image2)

**Figure 2-5** Example of redundancy in a 1-out-of-2 system with total failure
S7-400H setup options

3.1 S7-400H setup options

The first part of the description deals with the basic setup of the fault-tolerant S7-400H automation system, and with the components of an S7-400H basic system. We then describe the hardware components with which you can expand this basic system.

The second part deals with the software tools required for configuring and programming the S7-400H. Also included is a description of the extensions and functional expansions available for the S7-400 standard system which you need to create your user program to utilize all properties of your S7-400H in order to increase availability.

Important information on configuration

<table>
<thead>
<tr>
<th>WARNING</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Open equipment</strong></td>
</tr>
<tr>
<td>S7–400 modules are classified as open equipment, meaning you must install the S7-400 in an enclosure, cabinet, or switch room which can only be accessed by means of a key or tool. Such enclosures, cabinets, or switch rooms may only be accessed by instructed or authorized personnel.</td>
</tr>
</tbody>
</table>

The following figure shows an example of an S7-400H configuration with shared distributed I/O and connection to a redundant plant bus. The next pages deal with the hardware and software components required for the installation and operation of the S7-400H.
The components of the S7-400 standard system are also used in the fault-tolerant S7–400H automation system. For a detailed description of all hardware components for S7–400, refer to the Reference Manual *S7-400 Automation System; Module Specifications*.

The rules governing the design of the user program and the use of function blocks laid down for the S7-400 standard system also apply to the fault-tolerant S7-400H automation system. Refer to the descriptions in the *Programming with STEP 7* manual, and to the *System Software for S7-300/400; Standard and System Functions* Reference Manual.
3.2 Rules for the assembly of fault-tolerant stations

The following rules have to be complied with for a fault-tolerant station, in addition to the rules that generally apply to the arrangement of modules in the S7-400:

- The CPUs have to be inserted in the same slots.
- Redundantly used external DP master interfaces or communication modules must be inserted in the same slots in each case.
- External DP master interfaces for redundant DP master systems must only be inserted in central units rather than in expansion devices.
- Redundantly used CPUs must be identical, i.e. they must have the same article number, product version and firmware version. It is not the marking on the front side that is decisive for the product version, but the revision of the "Hardware" component ("Module status" dialog mask) to be read using Step 7.
- Redundantly used other modules must be identical, i.e. they must have the same article number, product version and - if available - firmware version.

3.3 The S7–400H basic system

Hardware of the basic system

The basic system consists of the hardware components required for a fault-tolerant controller. The following figure shows the components in the configuration.

The basic system can be expanded with S7–400 standard modules. Restrictions only apply to the function and communication modules; see Appendix Function modules and communication processors supported by the S7-400H (Page 429).
Central processing units

The two CPUs are the heart of the S7-400H. Use the switch on the rear of the CPU to set the rack numbers. In the following sections, we will refer to the CPU in rack 0 as CPU 0, and to the CPU in rack 1 as CPU 1.

Rack for S7–400H

The UR2-H rack supports the installation of two separate subsystems with nine slots each, and is suitable for installation in 19" cabinets.

You can also set up the S7-400H in two separate racks. The racks UR1 and UR2 are available for this purpose.

Power supply

You require one power supply module from the standard range of the S7-400 for each H-CPU, or to be more precise, for each of the two subsystems of the S7-400H.

To increase availability of the power supply, you can also use two redundant power supplies in each subsystem. Use the power supply modules PS 405 R / PS 407 R for this purpose. They can also be used together in redundant configurations (PS 405 R with PS 407 R).

Synchronization modules

The synchronization modules are used to link the two CPUs. They are installed in the CPUs and interconnected by means of fiber-optic cables.

There are two types of synchronization modules: one for distances up to 10 meters, and one for distances up to 10 km between the CPUs.

A fault-tolerant system requires 4 synchronization modules of the same type. For more information on synchronization modules, refer to section Synchronization modules for S7-400H (Page 323).

Fiber-optic cable

The fiber-optic cables are used to interconnect the synchronization modules for the redundant link between the two CPUs. They interconnect the upper and lower synchronization modules in pairs.

You will find the specifications of fiber-optic cables suitable for use in an S7-400H in section Selecting fiber-optic cables (Page 330).
3.4 I/O modules for S7–400H

I/O modules of the SIMATIC S7 series can be used for the S7-400H. The I/O modules can be used in the following devices:

- Central units
- Expansion units
- Distributed via PROFIBUS DP
- Distributed via PROFINET

You will find the function modules (FMs) and communications modules (CPs) suitable for use in the S7-400H in Appendix Function modules and communication processors supported by the S7-400H (Page 429).

I/O design versions

The following I/O module design versions are available:

- Single-channel, one-sided configuration with standard availability
  
  With the single-channel, one-sided design, single input/output modules are available. The I/O modules are located in only one subsystem, and are only addressed by this subsystem.

  However, in redundant mode, both CPUs are interconnected via the redundant link and thus execute the user program identically.

- Single-channel, switched configuration with enhanced availability
  
  Switched single-channel distributed configurations contain only single I/O modules, but they can be addressed by both subsystems.

- Redundant dual-channel configuration with maximum availability
  
  A redundant dual-channel configuration contains two sets of the I/O modules which can be addressed by both subsystems.

Additional information

For detailed information on using the I/O, refer to section Using I/Os in S7–400H (Page 163).
3.5 Communication

The S7-400H supports the following communication methods and mechanisms:

- Plant buses with Industrial Ethernet
- Point-to-point connection

This equally applies to the central and distributed components. Suitable communication modules are listed in Appendix Function modules and communication processors supported by the S7-400H (Page 429).

Communication availability

You can vary the availability of communication with the S7-400H. The S7-400H supports various solutions to meet your communication requirements. These range from a simple linear network structure to a redundant optical two-fiber loop.

Fault-tolerant communication via PROFIBUS or Industrial Ethernet is supported only by the S7 communication functions.

Programming and configuring

Apart from the use of additional hardware components, there are basically no differences with regard to configuration and programming compared to standard systems. Fault-tolerant connections only have to be configured; specific programming is not necessary.

All communication functions required for fault-tolerant communication are integrated in the operating system of the fault-tolerant CPU. These functions run automatically in the background, for example, to monitor the communication connection, or to automatically change over to a redundant connection in the event of error.

Additional information

For detailed information on communication with the S7-400H, refer to section Communication (Page 205).
3.6 Tools for configuration and programming

Like the S7-400, the S7-400H is also configured and programmed using STEP 7.

You only need to make allowances for slight restrictions when you write the user program. However, there are some additional details specific to the fault-tolerant configuration. The operating system automatically monitors the redundant components and switches over to the standby components when an error occurs. You have already configured the relevant information and communicated it to the system in your STEP 7 program.

Detailed information can be found in the online help, section Configuring with STEP 7 (Page 247), and Appendix Differences between fault-tolerant systems and standard systems (Page 425).

Optional software

All standard tools, engineering tools and runtime software used in the S7-400 system are also supported by the S7-400H system. Any restrictions in the functional scope are described in the respective Online Help.
3.7 The user program

The rules of developing and programming the user program for the standard S7-400 system also apply to the S7-400H.

In terms of user program execution, the S7-400H behaves in exactly the same manner as a standard system. The integral synchronization functions of the operating system are executed automatically in the background. You do not need to consider these functions in your user program.

In redundant operation, the user programs are stored identically on both CPUs and are executed in event-synchronous mode.

However, we offer you several specific blocks for optimizing your user program, e.g. in order to improve its response to the extension of cycle times due to updates.

Specific blocks for S7–400H

In addition to the blocks supported both in the S7-400 and S7-400H systems, the S7-400H software provides further blocks which you can use to influence the redundancy functions.

You can react to redundancy errors of the S7-400H using the following organization blocks:

- OB 70, I/O redundancy errors
- OB 72, CPU redundancy errors

SFC 90 "H_CTRL" can be used to influence fault-tolerant systems as follows:

- You can disable interfacing in the master CPU.
- You can disable updating in the master CPU.
- You can remove, resume or immediately start a test component of the cyclic self-test.
- You can execute a programmed master to standby changeover. The following changeovers are possible:
  - The current standby CPU becomes a master CPU.
  - The CPU in rack 0 becomes a master CPU.
  - The CPU in rack 1 becomes a master CPU.

Note

Required OBs

Always download these error OBs to the S7-400H CPU: OB 80, OB 82, OB 83, OB 85, OB 86, OB 88, OB 121 and OB 122. If you do not download these OBs, the fault-tolerant system goes into STOP when an error occurs.

Additional information

For detailed information on programming the blocks described above, refer to the STEP 7 Online Help.
### 3.8 Documentation

The figure below provides an overview of the descriptions of the various components and options in the S7-400H automation system.

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<th>Documentation</th>
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</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Figure 3-3 User documentation for fault-tolerant systems</td>
<td></td>
</tr>
</tbody>
</table>
S7-400H setup options

3.8 Documentation
4.1 Getting Started

Based on a specific example, these instructions guide you through the steps to implement commission all the way to a functional application. You will learn how an S7-400H automation system operates and become familiar with its response to a fault.

It takes about 1 to 2 hours to work through this example, depending on your previous experience.

4.2 Requirements

The following requirements must be met:

A correctly installed and valid version of the STEP 7 basic software on your programming device; see section Configuring with STEP 7 (Page 247). Any necessary hardware updates are installed.

The modules required for the hardware setup available:

- An S7-400H automation system consisting of:
  - 1 UR2–H rack
  - 2 PS 407 10 A power supply units
  - 2 H–CPUs
  - 4 synchronization modules
  - 2 fiber-optic cables

- An ET 200M distributed I/O device with active backplane bus with
  - 2 IM 153–2
  - 1 digital input module, SM321 DI 16 x DC24V
  - 1 digital output module, SM322 DO 16 x DC24V

- All necessary accessories such as PROFIBUS cables, etc.
4.3 Hardware assembly and commissioning of the S7–400H

Assembly of the hardware

Follow the steps below to assemble the S7-400H as shown in the following figure:

1. Assemble both modules of the S7-400H automation system as described in the S7-400 Automation Systems, Installation and Module Specifications manuals.

2. Set the rack numbers using the switch on the rear of the CPUs.
   An incorrectly set rack number prevents online access and the CPU might not start up.

3. Install the synchronization modules in the CPU. See chapter Synchronization modules (Page 323).

4. Connect the fiber-optic cables.
   Always interconnect the two upper and two lower synchronization modules of the CPUs. Route your fiber-optic cables so that they are reliably protected against any damage.
   You should also always make sure that the two fiber-optic cables are routed separately. This increases availability and protects the fiber-optic cables from potential double errors caused, for example, by interrupting both cables at the same time.
   Furthermore, always connect at least one fiber-optic cable to both CPUs before you switch on the power supply or the system. Otherwise both CPUs may execute the user program as master CPU.

5. Configure the distributed I/O as described in the ET 200M Distributed I/O Device manual.

6. Connect the programming device to the first fault-tolerant CPU (CPU0). This CPU will be the master of your S7-400H.

7. A high-quality RAM test (self-test) is executed after POWER ON. The self-test takes at least 10 minutes.
   The CPU cannot be accessed and the STOP LED flashes for the duration of this test. If you use a backup battery, this test is no longer performed when you power up in future.
Commissioning the S7–400H

Follow the steps outlined below to commission the S7–400H:

1. In SIMATIC Manager, open the sample project "HProject". The configuration corresponds to the hardware configuration described in "Requirements".

2. Open the hardware configuration of the project by selecting the "Hardware" object, then by right-clicking and selecting the shortcut menu command "Object -> Open". If your configuration matches, continue with step 6.

3. If your hardware configuration does not match the project, e.g. there are different module types, MPI addresses or DP addresses, edit and save the project accordingly. For additional information, refer to the basic help of SIMATIC Manager.

4. Open the user program in the "S7 program" folder.

   In the offline view, this "S7 program" folder is only assigned to CPU0. The user program is executable with the described hardware configuration. It activates the LEDs on the digital output module (running light).

5. Edit the user program as necessary to adapt it to your hardware configuration, and then save it.

6. Select "PLC -> Download" to download the user program to CPU0.

7. Start up the S7-400H automation system by setting the mode switch of CPU0 to RUN and then the switch on CPU1. The CPU performs a restart and calls OB 100.

   Result: CPU0 starts up as the master CPU and CPU1 as the reserve CPU. After the reserve CPU is linked and updated, the S7-400H assumes redundant mode and executes the user program. It activates the LEDs on the digital output module (running light).

---

**Note**

You can also start and stop the S7-400H automation system using STEP 7.

For additional information, refer to the online help.

You can only initiate a cold restart using the programming device command "Cold restart". For this purpose, the CPU must be in STOP mode and the mode switch must be set to RUN. OB 102 is called in the cold restart routine.
4.4 Examples of the response of the fault-tolerant system to faults

Example 1: Failure of a CPU or power supply module
Initial situation: The S7-400H is in redundant system mode.
1. Simulate a CPU0 failure by turning off the power supply.
   Result: The LEDs REDF, IFM1F and IFM2F light up on CPU1. CPU1 goes into single mode and continues to process the user program.
2. Turn the power supply back on.
   Result:
   – CPU0 performs an automatic LINK-UP and UPDATE.
   – CPU0 changes to RUN, and now operates as reserve CPU.
   – The S7-400H is now in redundant system mode.

Example 2: Failure of a fiber-optic cable
Initial situation: The S7-400H is in redundant system mode. The mode selector switch of each CPU is set to RUN.
1. Disconnect one of the fiber-optic cables.
   Result: The LEDs REDF and IFM1F or IFM2F (depending on which fiber-optic cable was disconnected) now light up on both CPUs. The reserve CPU changes to ERROR-SEARCH mode. The other CPU remains master and continues operation in single mode.
2. Reconnect the fiber-optic cable.
   Result: The reserve CPU performs starts a LINK-UP and UPDATE. The S7–400H resumes redundant system mode.
4.5 Special layout features of SIMATIC Manager

In order to do justice to the special features of a fault-tolerant system, the way in which the system is visualized and edited in SIMATIC Manager differs from that of a S7-400 standard station as follows:

- In the offline view, the S7 program appears only under CPU0. No S7 program is visible under CPU1.
- In the online view, the S7 program appears under both CPUs and can be selected in both locations.
- In the online view, the CPUs are represented by symbols that reflect the respective operating states of the CPUs.
- For programming device (PG) functions that set up online connections, one of the two CPUs has to be selected (even if the function affects the entire fault-tolerant system by means of the redundant link).

**Note**

You should preferably process CPU0, because information that is only available offline will be missing otherwise (e.g. comments or parameter names).
4.5 Special layout features of SIMATIC Manager
Assembly of a CPU 41x–H

5.1 Operator controls and display elements of the CPUs

Controls and display elements of CPU 41x-5H PN/DP

Figure 5-1 Arrangement of the control and display elements on CPU 41x-5H PN/DP

LED displays

The following table shows an overview of the LED displays on the individual CPUs.

Sections Monitoring functions of the CPU (Page 49) and Status and error displays (Page 52) describe the states and errors/faults indicated by these LEDs.
### Table 5-1  LED displays on the CPUs

<table>
<thead>
<tr>
<th>LED</th>
<th>Color</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTF</td>
<td>red</td>
<td>Internal error</td>
</tr>
<tr>
<td>EXTF</td>
<td>red</td>
<td>External error</td>
</tr>
<tr>
<td>BUS1F</td>
<td>red</td>
<td>Bus fault on MPI/PROFIBUS DP interface 1</td>
</tr>
<tr>
<td>IFM1F</td>
<td>red</td>
<td>Error in synchronization module 1</td>
</tr>
<tr>
<td>IFM2F</td>
<td>red</td>
<td>Error in synchronization module 2</td>
</tr>
<tr>
<td>FRCE</td>
<td>yellow</td>
<td>Active force request</td>
</tr>
<tr>
<td>MAINT</td>
<td>yellow</td>
<td>Maintenance request pending</td>
</tr>
<tr>
<td>RUN</td>
<td>green</td>
<td>RUN mode</td>
</tr>
<tr>
<td>STOP</td>
<td>yellow</td>
<td>STOP mode</td>
</tr>
<tr>
<td>REDF</td>
<td>red</td>
<td>Loss of redundancy/Redundancy fault</td>
</tr>
<tr>
<td>BUS2F</td>
<td>red</td>
<td>Bus error at the PROFIBUS interface</td>
</tr>
<tr>
<td>BUS5F</td>
<td>red</td>
<td>Bus error at the PROFINET interface</td>
</tr>
<tr>
<td>MSTR</td>
<td>yellow</td>
<td>CPU controls the process</td>
</tr>
<tr>
<td>RACK0</td>
<td>yellow</td>
<td>CPU in rack 0</td>
</tr>
<tr>
<td>RACK1</td>
<td>yellow</td>
<td>CPU in rack 1</td>
</tr>
<tr>
<td>LINK 1 OK</td>
<td>green</td>
<td>Connection via synchronization module 1 is active and OK</td>
</tr>
<tr>
<td>LINK 2 OK</td>
<td>green</td>
<td>Connection via synchronization module 2 is active and OK</td>
</tr>
<tr>
<td>LINK</td>
<td>green</td>
<td>Connection at the PROFINET interface is active</td>
</tr>
<tr>
<td>RX/TX</td>
<td>orange</td>
<td>Receiving or sending data at the PROFINET interface.</td>
</tr>
</tbody>
</table>

## Mode switch

You can use the mode switch to set the current operating mode of the CPU. The mode switch is a toggle switch with three switching positions.

Section *Function of the mode switch (Page 55)* describes the functions of the mode switch.

## Memory card slot

You can insert a memory card into this slot.

There are two types of memory card:

- **RAM cards**
  
  You can expand the CPU load memory with a RAM card.

- **FLASH cards**
  
  A FLASH card can be used for fail-safe backup of the user program and data without a backup battery. You can program the FLASH card either on the programming device or in the CPU. The FLASH card also expands the load memory of the CPU.

  For detailed information on memory cards, refer to section *Design and function of the memory cards (Page 60)*.
Slot for synchronization modules

You can insert one synchronization module into this slot. See chapter Synchronization modules (Page 323).

MPI/DP interface

You can, for example, connect the following devices to the MPI of the CPU:

- Programming devices
- Operator control and monitoring devices
- For further S7-400 or S7-300 controllers, see section Multi Point Interface MPI/DP (X1) (Page 65).

Use bus connectors with angled cable outlet, see the S7–400 Automation System, Installation manual.

The MPI can also be configured for operation as DP master and therefore as a PROFIBUS DP interface with up to 32 DP slaves.

PROFIBUS DP interface

The PROFIBUS DP interface supports the connection of distributed I/O, programming devices and OPs.

PROFINET interface

You can connect PROFINET IO devices to the PROFINET interface. The PROFINET interface features two switched ports with external connectors (RJ 45). The PROFINET interface provides the interconnection with Industrial Ethernet.

CAUTION

This interface only allows connection to an Ethernet LAN. You cannot connect it to the public telecommunication network, for example.

You may only connect PROFINET-compliant network components to this interface.

Setting the rack number

Use the switch on the rear panel of the CPU to set the rack number. The switch has two positions: 1 (up) and 0 (down). One CPU is allocated rack number 0, and the partner CPU is assigned rack number 1. The default setting of all CPUs is rack number 0.
Connecting an external backup voltage to the "EXT. BATT." socket

The S7–400H power supply modules support the use of two backup batteries. This allows you to implement the following:

● Back up the user program stored in RAM.
● Retain bit memories, timers, counters, system data and data in variable data blocks.
● Back up the internal clock.

You can achieve the same backup by connecting a DC voltage between 5 V DC and 15 V DC to the "EXT. BATT." socket of the CPU.

Properties of the "EXT. BATT." input:

● Reverse polarity protection
● Short-circuit current limiting to 20 mA

For incoming supply at the "EXT. BATT" socket, you require a connecting cable with a 2.5 mm Ø jack connector as shown in the figure below. Observe the polarity of the jack connector.

![Figure 5-2 Jack connector](image)

You can order an assembled jack connector and cable with the order number A5E00728552A.

**Note**

If you replace a power supply module and want to backup the user program and the data (as described above) in an RAM while doing so, you must connect an auxiliary power supply to the "EXT. BATT." socket.

Do not interconnect the cables of different CPUs. Interconnecting the cables of different CPUs may lead to problems with regard to EMC conditions and different voltage potentials.
### 5.2 Monitoring functions of the CPU

#### Monitoring functions and error messages

The hardware of the CPU and operating system provide monitoring functions to ensure proper operation and defined reactions to errors. Various errors may also trigger a reaction in the user program.

The table below provides an overview of possible errors and their causes, and the corresponding responses of the CPU.

Additional test and information functions are available in each CPU; they can be initiated in STEP 7.

<table>
<thead>
<tr>
<th>Type of error</th>
<th>Cause of error</th>
<th>Response of the operating system</th>
<th>Error LED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access error</td>
<td>Module failure (SM, FM, CP)</td>
<td>LED &quot;EXTF&quot; remains lit until the error is eliminated.</td>
<td>EXTF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In SMs:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Call of OB 122 with direct access, call of OB 85 in the event of a process image update</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Entry in the diagnostic buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In the case of input modules: Entry of &quot;null&quot; as date in the accumulator or the process image</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In the case of other modules:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Call of OB 122 with direct access, call of OB 85 in the event of a process image update</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time error</td>
<td>LED &quot;INTF&quot; remains lit until the error is eliminated.</td>
<td>INTF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Call of OB 80.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>If the OB is not loaded: CPU changes to STOP mode.</td>
<td>INTF</td>
</tr>
<tr>
<td></td>
<td>Power supply module(s) fault (not power failure)</td>
<td>Call of OB 81</td>
<td>EXTF</td>
</tr>
<tr>
<td></td>
<td>In the central or expansion rack:</td>
<td>If the OB is not loaded: The CPU remains in RUN.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• at least one backup battery in the power supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>module is flat.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• the backup voltage is missing.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• the 24 V supply to the power supply module has</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>failed.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## 5.2 Monitoring functions of the CPU

<table>
<thead>
<tr>
<th>Type of error</th>
<th>Cause of error</th>
<th>Response of the operating system</th>
<th>Error LED</th>
</tr>
</thead>
</table>
| Diagnostic interrupt | An I/O module with interrupt capability reports a diagnostic interrupt  
In a configuration as of V6.0: The synchronization module reports a diagnostics interrupt; see chapter Synchronization modules for S7–400H (Page 323) | Call of OB 82  
If the OB is not loaded: CPU changes to STOP mode. | EXTF |
| Swapping interrupt | Removal or insertion of an SM, and insertion of a wrong module type.  
Removing a synchronization module. | Call of OB 83  
If the OB is not loaded: CPU changes to STOP mode. | EXTF |
| Redundancy error interrupt | • Loss of redundancy on the CPUs  
• Standby master changeover  
• Synchronization error  
• Error in a synchronization module  
• Cancellation of the update process  
• Comparison error (e.g. RAM, PAA) | Call of OB 72  
If the OB is not loaded: The CPU remains in RUN. | EXTF |
| CPU hardware fault | • A memory error was detected and eliminated  
• In a configuration older than V6.0: Data transmission error at the redundant link. | Call of OB 84  
If the OB is not loaded: The CPU remains in RUN. | INTF |
| Program execution error | • Priority class is called, but the corresponding OB is not available.  
• In the case of an SFB call: Missing or faulty instance DB  
• Process image update error | Call of OB 85  
If the OB is not loaded: CPU changes to STOP mode. | INTF |
| Failure of a rack/station | • Power failure in an expansion rack  
• Failure of a DP/PN segment  
• Failure of a coupling segment: Missing or defective IM, interrupted cable | Call of OB 86  
If the OB is not loaded: CPU changes to STOP mode. | EXTF |
| Communication error | Communication error:  
• Time synchronization  
• Access to DB when exchanging data via communications function blocks | Call of OB 87  
If the OB is not loaded: CPU does not change to STOP mode. | INTF |
<table>
<thead>
<tr>
<th>Type of error</th>
<th>Cause of error</th>
<th>Response of the operating system</th>
<th>Error LED</th>
</tr>
</thead>
</table>
| Execution canceled  | The execution of a program block was canceled. Possible reasons for the cancellation are:  
  • Nesting depth of nesting levels too great  
  • Nesting depth of master control relay too great  
  • Nesting depth of synchronization errors too great  
  • Nesting depth of block call commands (U stack) too great  
  • Nesting depth of block call commands (B stack) too great  
  • Error during allocation of local data | Call of OB 88  
  If the OB is not loaded: CPU changes to STOP mode. | INTF       |
| Programming error   | User program error:  
  • BCD conversion error  
  • Range length error  
  • Range error  
  • Alignment error  
  • Write error  
  • Timer number error  
  • Counter number error  
  • Block number error  
  • Block not loaded | Call of OB 121  
  If the OB is not loaded: CPU changes to STOP mode. | INTF       |
| MC7 code error      | Error in the compiled user program, for example, illegal OP code or a jump beyond block end | CPU changes to STOP mode.  
  Restart or memory reset required. | INTF       |
## 5.3 Status and error displays

### RUN and STOP LEDs

The RUN and STOP LEDs provide information about the currently active CPU operating status.

<table>
<thead>
<tr>
<th>LED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RUN</strong></td>
<td><strong>STOP</strong></td>
</tr>
<tr>
<td>Lit</td>
<td>The CPU is in RUN mode.</td>
</tr>
<tr>
<td>Dark</td>
<td>The CPU is in STOP mode. The user program is not being executed. Cold</td>
</tr>
<tr>
<td>Flashes</td>
<td>The CPU is DEFECTIVE. All other LEDs also flash at 2 Hz.</td>
</tr>
<tr>
<td>Flashes</td>
<td>HOLD status has been triggered by a test function.</td>
</tr>
<tr>
<td>Dark</td>
<td>A cold restart/restart was initiated. The cold restart/warm start may</td>
</tr>
<tr>
<td>Flashes</td>
<td>A high-quality RAM test (self-test) is executed after POWER ON. The self-</td>
</tr>
<tr>
<td>Flashes</td>
<td>Troubleshooting mode</td>
</tr>
<tr>
<td>Flashes</td>
<td>Troubleshooting mode</td>
</tr>
<tr>
<td><strong>MSTR</strong>, <strong>RACK0</strong>, and <strong>RACK1</strong> LEDs</td>
<td>The three LEDs MSTR, RACK0, and RACK1 provide information about the rack number set on the CPU and show which CPU controls the switched I/O.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTR</td>
<td>CPU controls switched I/O</td>
</tr>
<tr>
<td>RACK0</td>
<td>CPU on rack number 0</td>
</tr>
<tr>
<td>RACK1</td>
<td>CPU on rack number 1</td>
</tr>
</tbody>
</table>

### Troubleshooting mode

This display also indicates that internal processes are busy on the CPU and prevent access to the CPU until completed. This status can be triggered by the following routines:

- Startup (POWER ON) of a CPU on which a large number of blocks is loaded. If encrypted blocks are loaded, startup may take a longer time depending on the number of such blocks.
- Memory reset after you have inserted a large Memory Card, or if there are encrypted blocks.
### INTF, EXTF, and FRCE LEDs

The three LEDs INTF, EXTF, and FRCE provide information about errors and special events in the user program execution.

<table>
<thead>
<tr>
<th>LED</th>
<th>INTF</th>
<th>EXTF</th>
<th>FRCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lit</td>
<td>Irrelevant</td>
<td>Irrelevant</td>
<td>An internal error was detected (programming or parameter assignment error).</td>
<td></td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Lit</td>
<td>Irrelevant</td>
<td>An external error was detected (i.e. an error whose cause is not in the CPU module).</td>
<td></td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Irrelevant</td>
<td>Lit</td>
<td>A force request is active.</td>
<td></td>
</tr>
</tbody>
</table>

### BUSF1 BUSF2 and BUS5F LEDs

The BUSF1, BUSF2 and BUS5F LEDs indicate errors associated with the MPI/DP, PROFIBUS DP and PROFINET interfaces.

<table>
<thead>
<tr>
<th>LED</th>
<th>BUS1F</th>
<th>BUS2F</th>
<th>BUS5F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lit</td>
<td>Irrelevant</td>
<td>Irrelevant</td>
<td>An error was detected at the MPI/DP interface.</td>
<td></td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Lit</td>
<td>Irrelevant</td>
<td>An error was detected at the PROFIBUS DP interface.</td>
<td></td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Irrelevant</td>
<td>Lit</td>
<td>An error was detected at the PROFINET IO interface.</td>
<td></td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Irrelevant</td>
<td>Flashes</td>
<td>One or several devices on the PROFINET IO interface are not responding.</td>
<td></td>
</tr>
<tr>
<td>Flashes</td>
<td>Irrelevant</td>
<td>Irrelevant</td>
<td>CPU is DP master:</td>
<td>One or several slaves at the PROFIBUS DP interface are not responding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CPU is DP slave:</td>
<td>CPU is not addressed by the DP master.</td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Flashes</td>
<td>Irrelevant</td>
<td>CPU is DP master:</td>
<td>One or several slaves at the PROFIBUS DP interface are not responding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CPU is DP slave:</td>
<td>CPU is not addressed by the DP master.</td>
</tr>
</tbody>
</table>

### IFM1F and IFM2F LEDs

The IFM1F and IFM2F LEDs indicate errors on the first or second synchronization module.

<table>
<thead>
<tr>
<th>LED</th>
<th>IFM1F</th>
<th>IFM2F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lit</td>
<td>Irrelevant</td>
<td>An error was detected on synchronization module 1.</td>
<td></td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Lit</td>
<td>An error was detected on synchronization module 2</td>
<td></td>
</tr>
</tbody>
</table>
**5.3 Status and error displays**

**LINK and RX/TX LEDs**

The LINK and RX/TX LEDs indicate the current state of the PROFINET interface.

<table>
<thead>
<tr>
<th>LED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>LINK</td>
<td>RX/TX</td>
</tr>
<tr>
<td>Lit</td>
<td>Irrelevant</td>
</tr>
<tr>
<td></td>
<td>Connection at the PROFINET interface is active</td>
</tr>
<tr>
<td>Irrelevant</td>
<td>Receiving or sending data at the PROFINET interface.</td>
</tr>
</tbody>
</table>

**Table 5-3 Possible states of the LINK and RX/TX LEDs**

**Note**

The LINK and RX/TX LEDs are located directly next to the PROFINET interface sockets. They are not labeled.

**REDF LED**

The REDF LED indicates specific system states and redundancy errors.

<table>
<thead>
<tr>
<th>REDF LED</th>
<th>System state</th>
<th>Basic requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flashes</td>
<td>Link-up</td>
<td>-</td>
</tr>
<tr>
<td>0.5 Hz</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Flashes</td>
<td>Update</td>
<td>-</td>
</tr>
<tr>
<td>2 Hz</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Dark</td>
<td>Redundant (CPUs are redundant)</td>
<td>No redundancy error</td>
</tr>
<tr>
<td>Lit</td>
<td>Redundant (CPUs are redundant)</td>
<td>There is an I/O redundancy error:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Failure of a DP master, or partial or total failure of a DP master system</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Loss of redundancy on the DP slave</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Loss of redundancy at the PN IO device</td>
</tr>
</tbody>
</table>
LEDs LINK1 OK and LINK2 OK

When commissioning the fault-tolerant system, you can use the LINK1 OK and LINK2 OK LEDs to check the quality of the connection between the CPUs.

<table>
<thead>
<tr>
<th>LED LINKx OK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lit</td>
<td>The connection is OK</td>
</tr>
<tr>
<td>Flashes</td>
<td>The connection is not reliable, and the signal is disrupted</td>
</tr>
<tr>
<td></td>
<td>Check the connectors and cables</td>
</tr>
<tr>
<td></td>
<td>Check whether the fiber-optic cables are installed in accordance with the guidelines in chapter</td>
</tr>
<tr>
<td></td>
<td>Installation of fiber-optic cables (Page 327).</td>
</tr>
<tr>
<td></td>
<td>Check whether the synchronization module works in another CPU.</td>
</tr>
<tr>
<td>Dark</td>
<td>The connection is interrupted, or there is insufficient light intensity</td>
</tr>
<tr>
<td></td>
<td>Check the connectors and cables</td>
</tr>
<tr>
<td></td>
<td>Check whether the fiber-optic cables are installed in accordance with the guidelines in chapter</td>
</tr>
<tr>
<td></td>
<td>Installation of fiber-optic cables (Page 327).</td>
</tr>
<tr>
<td></td>
<td>Check whether the synchronization module works in another CPU.</td>
</tr>
</tbody>
</table>

LED MAINT

This LED indicates that maintenance is required. For more information, refer to the STEP 7 Online Help.

Diagnostic buffer

In STEP 7, you can select "Target system -> Module Information" to read the cause of an error from the diagnostics buffer.

5.4 Mode switch

5.4.1 Function of the mode switch

Function of the mode switch

The mode switch can be used to set the CPU to RUN mode or STOP mode, or to reset the CPU memory. STEP 7 offers further options of changing the mode.
5.4 Mode switch

Positions

The mode switch is designed as toggle switch. The following figure shows all possible positions of the mode switch.

![Mode switch positions](image)

Figure 5-3 Mode switch positions

The following table explains the positions of the mode switch. If an error or a startup problem occurs, the CPU will either change to or stay in STOP mode regardless of the position of the mode switch.

<table>
<thead>
<tr>
<th>Position</th>
<th>Explanations</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN</td>
<td>If there is no startup problem or error and the CPU was able to switch to RUN, the CPU either executes the user program or remains idle. The I/O can be accessed.</td>
</tr>
<tr>
<td></td>
<td>• You can upload programs from the CPU to the programming device (CPU -&gt; Programming device)</td>
</tr>
<tr>
<td></td>
<td>• You can download programs from the programming device to the CPU (Programming device -&gt; CPU).</td>
</tr>
<tr>
<td>STOP</td>
<td>The CPU does not execute the user program. The digital signal modules are disabled. The output modules are disabled.</td>
</tr>
<tr>
<td></td>
<td>• You can upload programs from the CPU to the programming device (CPU -&gt; Programming device)</td>
</tr>
<tr>
<td></td>
<td>• You can download programs from the programming device to the CPU (Programming device -&gt; CPU).</td>
</tr>
<tr>
<td>MRES (Memory reset; Master Reset)</td>
<td>Momentary-on position of the toggle switch for CPU memory reset; see chapter Performing a memory reset (Page 57).</td>
</tr>
<tr>
<td></td>
<td>Momentary-on position for the &quot;Reset CPU to factory state&quot; function; see chapter  Resetting the CPU to the factory state (Page 75)</td>
</tr>
</tbody>
</table>
5.4.2 Performing a memory reset

Case A: You want to download a new user program to the CPU.

1. Set the switch to the STOP position.
   Result: The STOP LED is lit.
2. Toggle the switch to MRES, and hold it in that position. In this position the mode switch acts as pushbutton.
   Result: The STOP LED is off for one second, then on for one second, then again off for one second, and then it remains lit.
3. Then release the switch, return it to MRES within the next 3 seconds, and then release it again.
   Result: The STOP LED flashes for at least 3 seconds at 2 Hz (memory is reset) and then remains lit.

Case B: The STOP LED is flashing slowly at 0.5 Hz. This indicates that the CPU is requesting a memory reset (memory reset requested by system, e.g. after a memory card has been removed or inserted).

Toggle the switch to MRES, and then release it again.

Result: The STOP LED flashes for at least 3 seconds at 2 Hz, the memory reset is executed, and the LED then remains lit.

Memory reset process in the CPU

During a memory reset, the following process occurs on the CPU:

- The CPU deletes the entire user program in the main memory.
- The CPU deletes the user program from the load memory. This process deletes the program from the integrated RAM and from any inserted RAM Card. The user program elements stored on a FLASH card will not be deleted if you have expanded the load memory with such a card.
- The CPU deletes all counters, bit memories, and timers, but not the time of day.
- The CPU tests its hardware.
- The CPU sets its parameters to default settings.
- If a FLASH card is inserted, the CPU copies the user program and the system parameters stored on the FLASH card into main memory after the memory reset.
Data retained after a memory reset...

The following values are retained after a memory reset:

- The content of the diagnostic buffer
  
  If no FLASH card was inserted during memory reset, the CPU resets the capacity of the diagnostic buffer to its default setting of 120 entries, i.e. the most recent 120 entries will be retained in the diagnostic buffer.
  
  You can read out the content of the diagnostic buffer using STEP 7.

- The MPI/DP interface parameters. Note the special features shown in the table below.
  
  - MPI address
  - Highest MPI address
  - Baud rate.

- Parameters of the PN interface. Note the special features shown in the table below.
  
  - Name (NameOfStation)
  - IP address of CPU
  - Subnet mask
  - Static SNMP parameters

- The time of day

- The status and value of the operating hours counter

Special feature

A special situation is presented for the MPI/DP and PN interface parameters when a memory reset is performed. The following parameters are valid after a memory reset:

- Memory reset with inserted FLASH card:
  
  The parameters stored on the FLASH card are valid

- Memory reset without inserted FLASH card:
  
  The parameters in the CPU are retained and valid.
5.4.3 Cold restart / Warm restart

Cold restart

- A cold restart resets the process image, all bit memories, timers, counters, and data blocks to the initial values stored in the load memory, regardless of whether these data were parameterized as being retentive or not.
- Program execution resumes with OB 1, or with OB 102 if available.

Warm restart

- A warm restart resets the process image and the non-retentive bit memories, timers, times, and counters.
  - Retentive bit memories, timers, counters, and all data blocks retain their last valid value.
- The associated startup OB is OB 100
- Program execution resumes with OB 1, or with OB 100 if available.
- If the power supply is interrupted, the warm restart function is only available in backup mode.

Note

Restart in buffered Power On mode

In buffered PowerOn mode of a fault-tolerant system with large configurations, many CPs and/or external DP masters, it may take up to 30 seconds until a requested restart is executed.

Operating sequence for warm restart

1. Set the switch to the STOP position.
   **Result:** The STOP LED lights up.
2. Set the switch to RUN.
   **Result:** The STOP LED goes dark, the RUN LED is lit.

Operating sequence for cold restart

You can only initiate a cold restart using the programming device command "Cold restart". For this purpose, the CPU must be in STOP mode and the mode switch must be set to RUN.
5.5 Design and function of the memory cards

Order numbers

The order numbers for memory cards are listed in the technical specifications, see section Technical data of memory cards (Page 406).

Design of a memory card

The memory card is slightly larger than a credit card and is protected by a strong metal casing. It is inserted into one of the slots on the front of the CPU. The memory card is designed so that it can only be inserted one way.

Function of the memory card

The memory card and an integrated memory area on the CPU together form the load memory of the CPU. During operation, the load memory contains the complete user program, including comments, symbols, and special additional information that enables decompilation of the user program, as well as all module parameters.

Data stored on the memory card

The following data can be stored on the memory card:

- The user program, i.e. OBs, FBs, FCs, DBs, and system data
- Parameters that determine the behavior of the CPU
- Parameters that determine the behavior of I/O modules
- The full set of project files on suitable memory cards.
Serial number

In version 5 or later, all memory cards have a serial number. This serial number is listed in INDEX 8 of the SSL Parts List W#16#xy1C. The parts list can be read using SFC 51 "RDSYSST".

You can determine the following when you read the serial number in your user program: The user program can only be executed when a specific memory card is inserted into the CPU. This protects against unauthorized copying of the user program, similar to a dongle.
5.6 Using memory cards

Types of memory cards for the S7–400

Two types of memory cards are used for S7–400H:

- RAM cards
- FLASH cards

What type of memory card should I use?

Whether you use a RAM card or a FLASH card depends on your application.

<table>
<thead>
<tr>
<th>If you ...</th>
<th>Types of memory card</th>
</tr>
</thead>
<tbody>
<tr>
<td>want to be able to edit your program in RUN mode,</td>
<td>use a <strong>RAM card</strong></td>
</tr>
<tr>
<td>want to keep a permanent backup of your user program on the memory card, even when power is off, i.e. without backup or outside the CPU,</td>
<td>use a <strong>FLASH card</strong></td>
</tr>
</tbody>
</table>

RAM card

Insert the RAM card to load the user program in the CPU. Load the user program in STEP 7 by selecting "Target system > Download".

You can load the entire user program or individual elements such as FBs, FCs, OBs, DBs, or SDBs in the load memory in STOP or RUN mode.

When you remove the RAM card from the CPU, the information stored on it will be lost. The RAM card is not equipped with an integrated backup battery.

If the power supply is equipped with an operational backup battery, or the CPU is supplied with an external backup voltage at the "EXT. BATT." socket, the RAM card memory contents are retained when power is switched off, provided the RAM card remains inserted in the CPU and the CPU remains inserted in the rack.
FLASH card

If you use a FLASH card, there are two ways of loading the user program:

- Use the mode switch to set the CPU to STOP, insert the FLASH card into the CPU, and then download the user program to the FLASH card in STEP 7 by selecting "Target system > Download user program to memory card".
- You download the user program to the FLASH card in offline mode on the programming device/programming adapter, and then insert the FLASH card into the CPU.

The FLASH card is a non-volatile memory, i.e. its data are retained when it is removed from the CPU or your S7-400 is being operated without backup voltage (without a backup battery in the power supply module or external backup voltage at the "EXT. BATT." input of the CPU).

Automatic restart or cold restart without backup

If you operate your CPU without a backup battery, CPU memory reset followed by restart or cold restart, as configured, will automatically be carried out after switch-on or voltage recovery after power off. The user program must be available on the FLASH card and the battery indicator switch on the power supply module may not be set to battery monitoring.

If battery monitoring is set, you must carry out a restart or cold restart either with the mode switch or via a programming device after CPU switch on or voltage recovery following power off. The absence of or a defective backup battery is reported as an external fault and the LED EXTF lights up.

Downloading a user program

You can only download the full user program to a FLASH card.

Downloading additional user program elements

You can download further elements of the user program from the programming device to the integrated load memory of the CPU. Note that the content of this integrated RAM will be deleted if the CPU performs a memory reset, i.e. the load memory is updated with the user program stored on the FLASH card after a memory reset.

What memory card capacity should I use?

The capacity of your memory card is determined by the scope of the user program.
Determining memory requirements using SIMATIC Manager

You can view the block lengths offline in the "Properties - Block folder offline" dialog box (Blocks > Object Properties > Blocks tab).

The offline view shows the following lengths:

- Size (sum of all blocks, without system data) in the load memory of the target system
- Size (sum of all blocks, without system data) in the work memory of the target system

Block lengths on the programming device (PG/PC) are not shown in the properties of the block container.

Block lengths are shown in "byte" units.

The following values are shown in the properties of a block:

- Required local data volume: Length of local data in bytes
- MC7: Length of MC7 code in bytes
- Length of DB user data
- Length in load memory of the target system
- Length in work memory of the target system (only if hardware assignment is known)

The views always show these block data, regardless whether it is located in the window of an online view or of an offline view.

When a block container is opened and "View Details" is set, the project window always indicates work memory requirements, regardless of whether the block container appears in the window of an online or offline view.

You can add up the block lengths by selecting all relevant blocks. SIMATIC Manager outputs the total length of the selected blocks in its status bar.

Lengths of blocks (VATs, for example) which can not be downloaded to the target system are not shown.

Block lengths on the programming device (PG/PC) are not shown in the Details view.

See also [Technical data of memory cards](Page 406)
5.7 Multi Point Interface MPI/DP (X1)

Connectable devices

You can, for example, connect the following devices to the MPI:

- Programming devices (PG/PC)
- Operating and monitoring devices (OPs and TDs)
- Further SIMATIC S7 controllers

Various compatible devices take the 24 V supply from the interface. This voltage is non-isolated.

PG/OP–CPU communication

A CPU is capable of handling several online connections to PGs/OPs in parallel. By default, however, one of these connections is always reserved for a PG, and one for an OP/HMI device.

CPU–CPU communication

CPUs exchange data by means of S7 communication.

For additional information, refer to the Programming with STEP 7 manual.

Connectors

Always use bus connectors with an angular cable outlet for PROFIBUS DP or PG cables to connect devices to the MPI (see Installation Manual).

MPI as DP interface

You can also parameterize the MPI for operation as DP interface. To do so, reparameterize the MPI under STEP 7 in the SIMATIC Manager. You can configure a DP segment with up to 32 slaves.
5.8 PROFIBUS DP interface (X2)

Connectable devices

The PROFIBUS DP interface can be used to set up a PROFIBUS master system, or to connect PROFIBUS I/O devices.

You can connect redundant I/O to the PROFIBUS DP interface.

You can connect any standard-compliant DP slaves to the PROFIBUS DP interface.

Here, the CPU represents the DP master, and is connected to the passive slave stations or, in stand-alone mode, to other DP masters via the PROFIBUS DP fieldbus.

Various compatible devices take the 24 V supply from the interface. This voltage provided at the PROFIBUS DP interface is non-isolated.

Connectors

Always use bus connectors for PROFIBUS DP and PROFIBUS cables to connect devices to the PROFIBUS DP interface (refer to the Installation Manual).

Redundant mode

In redundant mode, the PROFIBUS DP interfaces have the same parameters.

5.9 PROFINET interface (X5)

Assigning an IP address

You have the following options of assigning an IP address to the Ethernet interface:

- By editing the CPU properties in HW Config. Download the modified configuration to the CPU.

You can also set up the IP address parameters and the station name (NameOfStation, NoS) locally without having to modify the configuration data.

- Using the "PLC -> Edit Ethernet Node" command in SIMATIC Manager.

Devices which can be connected via PROFINET (PN)

- Programming device/PC with Ethernet adapter and TCP protocol
- Active network components, e.g. Scalance X200
- S7-300/S7-400, e.g. CPU 417-5H PN/DP
- PROFINET IO devices, e.g. IM 153-4 PN in an ET 200M
Connectors

Always use RJ45 connectors to hook up devices to the PROFINET interface.

Properties of the PROFINET interface

Protocols and communication functions

- PROFINET IO
- In accordance with IEC61784-2, Conformance Class A and BC
- Open block communication over
  - TCP
  - UDP
  - ISO-on-TCP
- S7 communication
- PG functions
- Port statistics of PN IO devices (SNMP)
- Detection of the network topology (LLDP)
- Media redundancy (MRP)
- Time synchronization using the NTP method as a client, or the SIMATIC method

For more information on the properties of the PROFINET interface, refer to the technical specifications of the respective CPU. In Chapter [Technical data](Page 363).

<table>
<thead>
<tr>
<th>Connection</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Version</td>
<td>2 x RJ45</td>
</tr>
<tr>
<td>Media</td>
<td>Switch with 2 ports</td>
</tr>
<tr>
<td></td>
<td>Twisted pair Cat5</td>
</tr>
<tr>
<td>Transmission rate</td>
<td>10/100 Mbps</td>
</tr>
<tr>
<td></td>
<td>Autosensing</td>
</tr>
<tr>
<td></td>
<td>Autocrossing</td>
</tr>
<tr>
<td></td>
<td>Autonegotiation</td>
</tr>
</tbody>
</table>
Note

Networking PROFINET components

The PROFINET interfaces of our devices are set to "automatic setting" (autonegotiation) by default. Verify that all devices connected to the PROFINET interface of the CPU are also set to the "Autonegotiation" mode. This is the default setting of standard PROFINET / Ethernet components.

If connecting a device to the on-board PROFINET interface of the CPU that does not support the "automatic setting" (Autonegotiation) operating mode, or selecting a setting other than the "automatic setting" (Autonegotiation), note the following:

- PROFINET IO needs to be operated at 100 Mbps in full-duplex mode, which means if the on-board PROFINET interface of the CPU for PROFINET IO communication and Ethernet communication is used at the same time, the PROFINET interface may only be operated at 100 Mbps in full-duplex mode.

- Operation at 100 Mbps full-duplex is possible if the on-board PROFINET interface(s) of the CPU is(are) used for Ethernet communication only. Half-duplex mode is not allowed in any situation.

Background: If a switch that is permanently set to 10 Mbps half-duplex is connected to the interface of the CPU, the "Autonegotiation" setting forces the CPU to adapt itself to the settings of the partner device, i.e. the communication operates de facto at "10 Mbps half-duplex". However, this would not be a valid operating mode because PROFINET IO demands operation at 100 Mbps full-duplex.

Reference

- For additional information on PROFINET, refer to PROFINET System Description [http://support.automation.siemens.com/WW/view/en/19292127]


- For additional information about PROFINET, refer to: PROFINET [http://www.profibus.com/]


5.10 Overview of the parameters for the S7-400H CPUs

Default values

All parameters are set to factory defaults. These defaults are suitable for a wide range of standard applications and can be used to operate the S7-400H directly without having to make any additional settings.

You can determine the CPU-specific default values by selecting "Configuring Hardware" in STEP 7.

Parameter blocks

The responses and properties of the CPU are defined in parameters which are stored in system data blocks. The CPUs have a defined default setting. You can modify these default setting by editing the parameters in the hardware configuration.

The list below provides an overview of the parameterizable system properties of the CPUs.

- General properties such as the CPU name
- Start-up
- Cycle/clock memory, e.g. the scan cycle monitoring time
- Retentivity, i.e., the number of bit memories, timers, and counters that are retained after restart
- Memory, e.g. local data

Note: If you change the work memory allocation by modifying parameters, this work memory is reorganized when you download system data to the CPU. As a consequence, the data blocks generated by means of SFC are deleted and the remaining data blocks are initialized with values from load memory.

If you change the following parameters, the work memory area available for logic blocks and data blocks will be modified when loading the system data:

- Size of the process image, byte-oriented in the "Cycle/Clock memory" tab
- Communication resources in the "Memory" tab
- Size of the diagnostic buffer in the "Diagnostics/Clock" tab
- Number of local data for all priority classes in the "Memory" tab

- Assignment of interrupts (hardware interrupts, time delay interrupts, asynchronous error interrupts) to the priority classes
- Time-of-day interrupts such as start, interval duration, priority
- Watchdog interrupts, e.g. priority, interval duration
- Diagnostics/clock, e.g. time-of-day synchronization
5.10 Overview of the parameters for the S7-400H CPUs

- Security levels
- Fault tolerance parameters

Note
16 bit memory bytes and 8 counters are set by default in retentive memory, i.e., they are not deleted at a CPU restart.

Parameter assignment tool
You can set the individual CPU parameters using "HW Config" in STEP 7.

Note
If you modify the parameters listed below, the operating system initializes the following:
- Size of the process input image
- Size of the process output image
- Size of the local data
- Number of diagnostic buffer entries
- Communication resources

This involves the following initialization actions:
- Data blocks are initialized with the load values
- Bit memories, timers, counters, inputs and outputs are deleted, regardless of their retentivity setting (0).
- DBs generated by SFC will be deleted
- Permanently configured, basic communication connections are shut down
- All run levels are initialized.

Further settings
- The rack number of a fault-tolerant CPU, 0 or 1
  Use the selector switch on the rear panel of the CPU to change the rack number.
- The operating mode of a fault-tolerant CPU: Stand-alone or redundant mode
  For information on how to change the operating mode of a fault-tolerant CPU, refer to Appendix Stand-alone operation (Page 419).
6.1 Security levels

You can define a security level for your project in order to prevent unauthorized access to the CPU programs. The objective of these security level settings is to grant a user access to specific programming device functions which are not protected by password, and to allow that user to execute those functions on the CPU. When logged on with a password, the user may execute all PG functions.

Setting security levels

You can set the CPU security levels 1 to 3 under "STEP 7/Configure Hardware". If you do not know the password, you can clear the set security level by means of a manual memory reset using the mode selector. No Flash card must be inserted in the CPU when you perform such an operation.

The following table lists the security levels of an S7–400 CPU.

Table 6-1 Security levels of a CPU

<table>
<thead>
<tr>
<th>CPU function</th>
<th>Security level 1</th>
<th>Security level 2</th>
<th>Security level 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display of list of blocks</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>Monitor variables</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>Module status STACKS</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>Operator control and monitoring functions</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>Reading the time</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>Setting the time</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Access granted</td>
</tr>
<tr>
<td>Block status</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Password required</td>
</tr>
<tr>
<td>Load in PG</td>
<td>Access granted</td>
<td>Access granted</td>
<td>Password required</td>
</tr>
<tr>
<td>Load in CPU</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Delete blocks</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Compress memory</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Download user program to memory card</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Controlling selection</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Modify variable</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Breakpoint</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Clear breakpoint</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
<tr>
<td>Memory reset</td>
<td>Access granted</td>
<td>Password required</td>
<td>Password required</td>
</tr>
</tbody>
</table>
### Setting the security level with SFC 109 "PROTECT"

You can set the following security levels on your CPU with SFC 109:

- **SFC 109 call with MODE=0**: Setting of security level 1. The SFC 109 call with MODE=0 overrides any existing lock of password legitimization.

- **SFC 109 call with MODE=1**: Setting of security level 2 with password legitimization. This means you can cancel the write protection set with SFC 109 if you know the valid password. The SFC 109 call with MODE=1 overrides any existing lock of password legitimization.

- **SFC 109 call with MODE=12**: Setting of security level 3 without password legitimization. This means you cannot cancel the write and read protection set with SFC 109 even if you know the valid password. If a legitimate connection exists when you call SFC-109 with MODE=12, the SFC-109 call has no effect on this connection.

### Note

**Setting a lower security level**

You can use SFC 109 "PROTECT" to set a lower security level than the one you configured with STEP 7 "Configure hardware".

### Additional aspects

- Both fault-tolerant CPUs of a fault-tolerant system can have different security levels in STOP.

- The security level is transferred from the master to the standby during link-up/update operations.

- The set security levels of both fault-tolerant CPUs are retained if you make modifications to the plant during operation.

- The security level is transferred to the target CPU in the following cases:
  - Switching to CPU with modified configuration
  - Switching to a CPU with expanded memory configuration
  - Switching to a CPU with modified operating system
  - Switching to a CPU using only one intact redundant link
6.2 Access-protected blocks

S7-Block Privacy

The STEP 7 add-on package S7-Block Privacy can be used to protect the functions and function blocks against unauthorized access.

Observe the following information when using S7-Block Privacy:

- S7-Block Privacy is operated by means of shortcut menus. To view a specific menu help, press the "F1" function key.
- You can no longer edit protected blocks in STEP 7. Moreover, testing and commissioning functions such as "Monitor blocks" or breakpoints are no longer available. Only the interfaces of the protected block remain visible.
- Protected blocks can only be released again for editing if you have the correct key and the corresponding decompilation information included in your package. Make sure that the key is always kept in a safe place.
- The loading of protected blocks is only supported on CPUs as of version 6.0.
- If your project contains sources, you can use these to restore the protected blocks by means of compilation. The S7-Block Privacy sources can be removed from the project.

Note

Memory requirements

Each protected block with decompilation information occupies 232 additional bytes in load memory.

Each protected block without decompilation information occupies 160 additional bytes in load memory.

Extended runtimes

The startup time of the CPU at power on, the loading time of blocks and the startup after a system modification at runtime may be significantly prolonged.

Operation with FlashCard can significantly prolong the time for memory reset.

To optimize additional time requirements, it is best practice to protect one large block instead of many small blocks.

If you have many protected blocks and change one of the following parameters, the error "Unable to load system data..." could occur during the loading process.

- Size of the process image
- Size of the diagnostic buffer
- Maximum number of communication jobs
- Total amount of local data

Download the system data once again in this case.
Additional information

For additional information, refer to "S7 block privacy" in the STEP 7 Online Help.
6.3 Resetting the CPU to the factory state

CPU factory settings

A general memory reset is performed when you reset the CPU to its factory settings and the properties of the CPU are set to the following values:

Table 6-2 CPU properties in the factory settings

<table>
<thead>
<tr>
<th>Properties</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPI address</td>
<td>2</td>
</tr>
<tr>
<td>MPI transmission rate</td>
<td>187.5 Kbps</td>
</tr>
<tr>
<td>Contents of the diagnostic buffer</td>
<td>Empty</td>
</tr>
<tr>
<td>IP parameters</td>
<td>None</td>
</tr>
<tr>
<td>IP parameters</td>
<td>Default values</td>
</tr>
<tr>
<td>Operating hours counter</td>
<td>0</td>
</tr>
<tr>
<td>Date and time</td>
<td>01.01.94, 00:00:00</td>
</tr>
</tbody>
</table>

Procedure

Proceed as follows to reset a CPU to its factory settings:

1. Switch off the mains voltage.
2. If a memory card is inserted in the CPU, always remove the memory card.
3. Hold the toggle switch in the MRES setting and switch the mains voltage on again.
4. Wait until LED pattern 1 from the following overview is displayed.
5. Release the toggle switch, set it back to MRES within 3 seconds and hold it in this position. After approx. 4 seconds all the LEDs light up.
6. Wait until LED pattern 2 from the following overview is displayed. This LED pattern lights up for approximately 5 seconds. During this period you can abort the resetting procedure by releasing the toggle switch.
7. Wait until LED pattern 3 from the following overview is displayed, and release the toggle switch again.

The CPU is now reset to its factory settings. It starts without buffering and goes to STOP mode. The event "Reset to factory setting" is entered in the diagnostic buffer.

Note

Canceling the operation

If the described operation is canceled prematurely and the CPU remains in an undefined state, you can once again set it to a defined state by cycling power off and on.
LED patterns during CPU reset

While you are resetting the CPU to its factory settings, the LEDs light up consecutively in the following LED patterns:

Table 6-3  LED patterns

<table>
<thead>
<tr>
<th>LED</th>
<th>LED pattern 1</th>
<th>LED pattern 2</th>
<th>LED pattern 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTF</td>
<td>Flashes at 0.5 Hz</td>
<td>Flashes at 0.5 Hz</td>
<td>Lit</td>
</tr>
<tr>
<td>EXT</td>
<td>Dark</td>
<td>Dark</td>
<td>Dark</td>
</tr>
<tr>
<td>BUSxF</td>
<td>Dark</td>
<td>Dark</td>
<td>Dark</td>
</tr>
<tr>
<td>FORCE</td>
<td>Flashes at 0.5 Hz</td>
<td>Dark</td>
<td>Dark</td>
</tr>
<tr>
<td>MAINT</td>
<td>Dark</td>
<td>Dark</td>
<td>Dark</td>
</tr>
<tr>
<td>IFMxF</td>
<td>Dark</td>
<td>Dark</td>
<td>Dark</td>
</tr>
<tr>
<td>RUN</td>
<td>Flashes at 0.5 Hz</td>
<td>Dark</td>
<td>Dark</td>
</tr>
<tr>
<td>STOP</td>
<td>Flashes at 0.5 Hz</td>
<td>Dark</td>
<td>Dark</td>
</tr>
</tbody>
</table>
6.4 Updating the firmware without a memory card

Basic procedure

To update the firmware of a CPU, you will receive several files (*.UPD) containing the current firmware. Download these files to the CPU. You do not need a memory card to perform an online update. However, it is still possible to update the firmware using a memory card.

Requirement

The CPU whose firmware you want to update must be accessible online, e.g. via PROFIBUS, MPI, or Industrial Ethernet. The files containing the current firmware versions must be available in the programming device/PC file system. A folder may contain only the files of one firmware version. If security level 2 or 3 is set for the CPU, you require the password to update the firmware.

Note

You can update the firmware of the fault-tolerant CPUs via Industrial Ethernet. Updating the firmware over a MPI can take a long time if the transfer rate is low (e.g. approximately 10 minutes at 187.5 Kbit/s).

Procedure in HW Config

Proceed as follows to update the firmware of a CPU:

1. Open the station containing the CPU you want to update in HW Config.
2. Select the CPU.
3. Select the "PLC -> Update Firmware" menu command.
4. In the "Update Firmware" dialog, select the path to the firmware update files (*.UPD) using the "Browse" button.
   After you have selected a file, the information in the bottom boxes of the "Update Firmware" dialog box indicate the modules for which the file is suitable and from which firmware version.
5. Click on "Run".

STEP 7 verifies that the selected file can be interpreted by the CPU and then downloads the file to the CPU. If this requires changing the operating state of the CPU, you will be prompted to do this in the relevant dialog boxes.
6.4 Updating the firmware without a memory card

Procedure in SIMATIC Manager

The command procedure is the same as in HW Config, i.e. "PLC > Update firmware". However, STEP 7 waits until the command is executed before it verifies that the module supports this function.

Note

Update security

For reasons of firmware security, the CPU validates a digital signature before it runs the firmware update. If it detects an error, it retains the current firmware version and rejects the new one.

Values retained after a firmware update

The following values are retained after a CPU memory reset:

- Parameters of the MPI (MPI address and highest MPI address).
- IP address of the CPU
- Device name (NameOfStation)
- Subnet mask
- Static SNMP parameters
6.5 Firmware update in RUN mode

Requirement

The size of the load memory on the master and reserve CPU is the same. Both Sync links exist and are working.

Procedure for automatic firmware update

Initial situation: Both CPUs are in redundant operation.

1. Select one of the two CPUs using either SIMATIC Manager -> Project, or HW Config.
   Do not use the "Accessible nodes" menu command in SIMATIC Manager.
2. Select the "PLC > Update Firmware" menu command.
   A wizard is started that can automatically update the firmware on both CPUs.

Alternative procedure for progressive firmware update

Follow the steps below to update the firmware of the CPUs of an H system in RUN:

1. Set one of the CPUs to STOP using the programming device
2. Select this CPU in HW Config or in SIMATIC Manager in your STEP 7 project.
3. Select the "PLC -> Update Firmware" menu command.
   The "Update Firmware" dialog box opens. Select the firmware file from which the current firmware will be downloaded to the selected CPU.
4. In SIMATIC Manager or HW Config, select the "PLC -> Operating Mode -> Switch to CPU 41x-H" and select the "with altered operating system" check box.
   The fault-tolerant system switches the master/standby roles, after which the CPU will be in RUN again.
5. Repeat steps 1 to 3 for the other CPU.
6. Restart the CPU. The fault-tolerant system will return to redundant mode.

Both CPUs have updated firmware (operating system) and are in redundant mode.

Note

Only the third number of the firmware versions of the master and reserve CPU may differ by 1. You can only update to the newer version.

Example: From V6.0.0 to V6.0.1

Please take note of any information posted in the firmware download area.

The constraints described in section System and operating states of the S7–400H (Page 115) also apply to a firmware update in RUN.
6.6 Reading service data

Application case

If you need to contact Customer Support due to a service event, the department may require specific diagnostic information on the CPU status of your system. This information is stored in the diagnostic buffer and in the service data.

Select the "PLC -> Save service data" command to read this information and save the data to two files. You can then send these to Customer Support.

Note the following:

- If possible, save the service data immediately after the CPU goes into STOP or the synchronization of a fault-tolerant system has been lost.
- Always save the service data of both CPUs in an H system.

Procedure

1. Select the "PLC > Save service data" command.
   
   In the dialog box that opens up, select the file path and the file names.

2. Save the files.

3. Forward these files to Customer Support on request.
PROFIBUS DP

7.1 CPU 41x–H as PROFIBUS DP master

Introduction

This chapter describes how to use the CPU as DP master and configure it for direct data exchange.

Further references

The STEP 7 Online Help provides descriptions and information on the following topics:

● Planning of a PROFIBUS subnet
● Configuration of a PROFIBUS subnet
● Diagnostics in the PROFIBUS subnet

Additional information

Details and information on migrating from PROFIBUS DP to PROFIBUS DPV1 is available under entry ID 7027576 at the Internet address:
http://support.automation.siemens.com

7.1.1 DP address ranges of CPUs 41x-H

Address ranges of CPUs 41x-H

Table 7-1 CPUs 41x-H, MPI/DP interface as PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Address range</th>
<th>412-5H</th>
<th>414-5H</th>
<th>416-5H</th>
<th>417-5H</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPI as PROFIBUS DP, inputs and outputs (bytes) in each case</td>
<td>2048</td>
<td>2048</td>
<td>2048</td>
<td>2048</td>
</tr>
<tr>
<td>DP interface as PROFIBUS DP, inputs and outputs (bytes) in each case</td>
<td>4096</td>
<td>6144</td>
<td>8192</td>
<td>8192</td>
</tr>
<tr>
<td>Of those addresses you can configure up to x bytes for each I/O in the process image</td>
<td>0 to 8192</td>
<td>0 to 8192</td>
<td>0 to 16384</td>
<td>0 to 16384</td>
</tr>
</tbody>
</table>

DP diagnostics addresses occupy at least 1 byte for the DP master and each DP slave in the input address area. At these addresses, the DP standard diagnostics can be called for the relevant node by means of the LADDR parameter of SFC 13, for example. Define the DP diagnostics addresses when you configure the project data. If you do not specify any DP diagnostics addresses, STEP 7 automatically assigns the addresses as DP diagnostics addresses in descending order, starting at the highest byte address.
7.1 CPU 41x–H as PROFIBUS DP master

7.1.2 CPU 41x–H as PROFIBUS DP master

Requirement

You have to configure the relevant CPU interface for use as PROFIBUS DP master. This means you must make the following settings in STEP 7:

- Assign a network
- Configure the CPU as PROFIBUS DP master
- Assign a PROFIBUS address
- Change the operating mode, if necessary; the default setting is DPV1.
- Link DP slaves to the DP master system

Note

Is one of the PROFIBUS DP slaves a CPU 31x or CPU 41x?

If yes, you will find it in the PROFIBUS DP catalog as "preconfigured station". Assign this DP slave CPU a slave diagnostics address in the PROFIBUS DP master. Link the PROFIBUS DP master to the DP slave CPU, and specify the address areas for data exchange with the DP slave CPU.

Monitor/Modify, programming via PROFIBUS

As an alternative to the MPI, you can use the PROFIBUS DP interface to program the CPU or execute the Monitor/Modify programming device functions.

Note

The "Programming" or "Monitor/Modify" applications prolong the DP cycle if executed via the PROFIBUS DP interface.

DP master system startup

Use the following parameters to set startup time monitoring of the PROFIBUS DP master:

- Ready message from module
- Transfer of parameters to modules

This means the DP slaves must start up within the set time and be parameterized by the CPU (as PROFIBUS DP master).

PROFIBUS address of the PROFIBUS DP master

All PROFIBUS addresses are permissible.
From IEC 61158 to DPV1

The IEC 61158 standard for distributed I/Os has been enhanced. The enhancements were incorporated into IEC 61158/IEC 61784–1:2002 Ed1 CP 3/1. The SIMATIC documentation uses the term "DPV1" in this context. The new version features various expansions and simplifications.

SIEMENS automation components feature DPV1 functionality. In order to be able to use these new features, you first have to make some modifications to your system. A full description of the migration from IEC 61158 to DPV1 is available in the FAQ section titled "Migrating from IEC 61158 to DPV1", FAQ entry ID 7027576, on the Customer Support Internet site.

Components supporting PROFIBUS DPV1 functionality

**DPV1 master**

- The S7-400 CPUs with integrated DP interface.
- CP 443-5 with order number 6GK7 443–5DX03–0XE0, 6GK7 443–5DX04–0XE0, 6GK7 443-5DX05-0XE0.

**DPV1 slaves (default setting in SIMATIC)**

- DP slaves listed in the STEP 7 hardware catalog under their family names can be identified as DPV1 slaves in the information text.
- DP slaves that are integrated in STEP 7 by means of GSD files, revision 3 or higher.

What operating modes are there for DPV1 components?

- **S7-compatible mode**
  
  In this mode, the component is compatible with IEC 61158. However, you cannot use the full DPV1 functionality.

- **DPV1 mode**
  
  In this mode the component can make full use of DPV1 functionality. Automation components in the station that do not support DPV1 can be used as before. The DPV1 mode is set by default in SIMATIC.

Compatibility between DPV1 and IEC 61158?

You can continue to use all existing slaves after converting to DPV1. These do not, however, support the enhanced functions of DPV1.

You can also use DPV1 slaves without a conversion to DPV1. In this case they behave like conventional slaves. SIEMENS DPV1 slaves can be operated in S7-compatible mode. To integrate DPV1 slaves from other manufacturers, you need a GSD file complying with IEC 61158 earlier than revision 3.
Determining the bus topology in a DP master system using SFC 103 "DP_TOPOL"

A diagnostic repeater is available to make it easier to localize disrupted modules or DP cable breaks when failures occur during operation. This module is a slave that discovers the topology of a PROFIBUS subnet and detects any problems caused by it.

You can use SFC 103 "DP_TOPOL" to trigger the determination of the bus topology of a DP master system by the diagnostic repeater. SFC 103 is described in the corresponding online help and in the "System and Standard Functions manual. For information on the diagnostic repeater refer to the "Diagnostic Repeater for PROFIBUS DP manual, order number 6ES7972–0AB00–8BA0."
7.1.3 Diagnostics of the CPU 41x-H operating as PROFIBUS DP master

Diagnostics using LEDs

The following table shows the meaning of the BUSF LEDs. Always the BUSF LED assigned to the interface configured as PROFIBUS DP interface lights up or flashes when a problem occurs.

Table 7-2 Meaning of the "BUSF" LED of the CPU 41x operating as DP master

<table>
<thead>
<tr>
<th>BUSF</th>
<th>Meaning</th>
<th>What to do</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Configuration correct; all configured slaves are addressable</td>
<td>-</td>
</tr>
<tr>
<td>Lit</td>
<td>• DP interface error&lt;br&gt; • Different Baud rates in multi-DP master&lt;br&gt; operation (only in stand-alone mode)</td>
<td>• Evaluate the diagnosis. Reconfigure or correct the configuration.</td>
</tr>
<tr>
<td>Flashes</td>
<td>• Station failure&lt;br&gt; • At least one of the assigned slaves cannot be addressable</td>
<td>• Check whether the bus cable is connected to the CPU 41x or whether the bus is interrupted.&lt;br&gt; • Wait until the CPU 41x has powered up. If the LED does not stop flashing, check the DP slaves or evaluate the diagnosis of the DP slaves.&lt;br&gt; • Check whether the bus cable has a short-circuit or a break.</td>
</tr>
</tbody>
</table>

Reading out the diagnostics information with STEP 7

Table 7-3 Reading out the diagnostics information with STEP 7

<table>
<thead>
<tr>
<th>DP master</th>
<th>Block or tab in STEP 7</th>
<th>Application</th>
<th>See ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU 41x</td>
<td>&quot;DP slave diagnostics&quot; tab</td>
<td>Display the slave diagnosis as plain text on the STEP 7 user interface</td>
<td>See &quot;Hardware diagnostics&quot; in the STEP 7 Online Help, and Configuring hardware and connections with STEP 7 in the manual</td>
</tr>
<tr>
<td>SFC 13 &quot;DPNRM_DG&quot;</td>
<td>Reading slave diagnostics data, i.e. saving them to the data area of the user program</td>
<td>For information on the configuration of a CPU 41x, refer to the CPU Data Reference Manual; for information on the SFC, refer to the System and Standard Functions Reference Manual. For information on the configuration of other slaves, refer to the corresponding description.</td>
<td></td>
</tr>
<tr>
<td>SFC 59 &quot;RD_REC&quot;</td>
<td>Readout of data records of the S7 diagnosis (saving them to the data area of the user program)</td>
<td>Refer to the System and Standard Functions Reference Manual</td>
<td></td>
</tr>
</tbody>
</table>
### PROFIBUS DP

#### 7.1 CPU 41x-H as PROFIBUS DP master

<table>
<thead>
<tr>
<th>DP master</th>
<th>Block or tab in STEP 7</th>
<th>Application</th>
<th>See ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFC 51 &quot;RDSYSST&quot;</td>
<td></td>
<td>Readout of system status lists (SSL). Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.</td>
<td></td>
</tr>
<tr>
<td>SFB 52 &quot;RDREC&quot;</td>
<td></td>
<td>Reading data records of S7 diagnostics, i.e. saving them to the data area of the user program.</td>
<td></td>
</tr>
<tr>
<td>SFB 54 &quot;RALRM&quot;</td>
<td></td>
<td>Readout of interrupt information within the associated interrupt OB.</td>
<td></td>
</tr>
</tbody>
</table>

**Evaluating diagnostics data in the user program**

The figure below shows how to evaluate the diagnostics data in the user program.

![Diagram of diagnostics with CPU 41xH](image)

**Figure 7-1** Diagnostics with CPU 41xH
Diagnostics addresses in connection with DP slave functionality

Assign the diagnostics addresses for PROFIBUS DP at the CPU 41xH. Verify in the configuration that the DP diagnostics addresses are assigned once to the DP master and once to the DP slave.

During configuration of the DP master, specify a diagnostic address for the DP slave (in the associated project of the DP master). This diagnostic address is identified as assigned to the DP master below.

This diagnostic address is used by the DP master to obtain information about the status of the DP slave or about bus interruptions. See also table below.

During configuration of the DP slave, also specify a diagnostic address that is assigned to the DP slave (in the associated project of the DP slave). This diagnostic address is identified as assigned to the DP slave below.

This diagnostic address is used by the DP slave to obtain information about the status of the DP master or about bus interruptions.

Figure 7-2  Diagnostics addresses for DP master and DP slave

Event detection

The table below shows how the CPU 41xH in DP master mode detects operating state changes on an I-slave or interruptions of the data transfer.

Table 7-4  Event detection of the CPU 41xH as a DP master

<table>
<thead>
<tr>
<th>Event</th>
<th>What happens in the DP master</th>
</tr>
</thead>
</table>
| Bus interruption due to short-circuit or disconnection of the connector | • OB 86 is called with the message **Station failure** as an incoming event; diagnostics address of the DP slave/I-slave assigned to the DP master  
• With I/O access: Call of OB 122, I/O area access error |
| Time-outs when the system updates the process image | • Call of OB 85                                                                                   |
| I-slave: RUN → STOP                         | • OB 82 is called with the message **Module error** as incoming event; diagnostic address of the I-slave assigned to the DP master; tag OB82_MDL_STOP=1 |
| I-slave: STOP → RUN                         | • OB 82 is called with the message **Module OK** as incoming event; diagnostic address of the I-slave assigned to the DP master; tag OB82_MDL_STOP=0 |
Evaluation in the user program

The table below shows you how to evaluate RUN-STOP changes of the I-slave on the DP master. Also refer to previous table.

<table>
<thead>
<tr>
<th>On the DP master</th>
<th>In the I-slave (CPU 41x)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Example of diagnostics addresses:</td>
<td>• Example of diagnostics addresses:</td>
</tr>
<tr>
<td>Master diagnostics address=1023</td>
<td>Slave diagnostics address=422</td>
</tr>
<tr>
<td>Slave diagnostics address in master system=1022</td>
<td>Master diagnostics address=irrelevant</td>
</tr>
</tbody>
</table>

The CPU calls OB 82 with the following information, for example:
- OB 82_MDL_ADDR:=1022
- OB82_EV_CLASS:=B#16#39
  As incoming event
- OB82_MDL_DEFECT:=module error

The CPU diagnostic buffer also contains this information

You also program SFC 13 "DPNRM_DG" in the user program for reading the diagnostic data of the I-slave.

Use SFB 54 in the DPV1 environment. This outputs the full interrupt information.

CPU: RUN → STOP
CPU generates an I-slave diagnostics frame.
8.1 Introduction

What is PROFINET?

PROFINET is the open, non-proprietary Industrial Ethernet standard for automation. It enables comprehensive communication from the business management level down to the field level.

PROFINET fulfills the high demands of industry, for example:
- Industrial-compliant installation engineering
- Real-time capability
- Non-proprietary engineering

There are a wide range of products from active and passive network components, controllers, distributed field devices to components for industrial wireless LAN and industrial security available for PROFINET.

Information about the use of I/Os at the PROFINET interface is available in the chapter System redundancy (Page 99).

With PROFINET IO a switching technology is implemented that allows all stations to access the network at any time. In this way, the network can be used much more efficiently through the simultaneous data transfer of several nodes. Simultaneous sending and receiving is enabled through the full-duplex operation of Switched Ethernet.

PROFINET IO is based on Switched Ethernet full-duplex operation and a bandwidth of 100 Mbit/s.

In PROFINET IO communication, a slice of the transmission time is reserved for cyclic, deterministic data transmission. This allows you to split the communication cycle into a deterministic and an open part. Communication takes place in real-time.

Direct connection of distributed field devices (IO devices, such as signal modules) to Industrial Ethernet. PROFINET IO supports a consistent diagnostics concept for efficient error localization and troubleshooting.

Note

No changes to the PROFINET interface at runtime

I/O components that are connected to a PROFINET interface as well as parameters of the PROFINET interface cannot be modified during operation.
**8.1 Introduction**

**Documentation on the Internet**


Also observe the following documents:

- Installation guideline
- Assembly guideline
- PROFINET_Guideline_Assembly

Additional information on the use of PROFINET in automation engineering is available at the following Internet address [http://www.siemens.com/profinet/](http://www.siemens.com/profinet/).
8.2 PROFINET IO systems

Functions of PROFINET IO

The following graphic shows the new functions in PROFINET IO:

<table>
<thead>
<tr>
<th>The graphic shows</th>
<th>Examples of connection paths</th>
</tr>
</thead>
<tbody>
<tr>
<td>The connection of company network and field level</td>
<td>You can access devices at the field level from PCs in your company network</td>
</tr>
<tr>
<td>Connections between the automation system and field level</td>
<td>You can also access other areas on the Industrial Ethernet from a programming device at the field level.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>The connection of company network and field level</th>
<th>You can access devices at the field level from PCs in your company network</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example: PC - Switch 1 - Router - Switch 2 - CPU 41x-5H PN/DP ①.</td>
<td></td>
</tr>
<tr>
<td>Connections between the automation system and field level</td>
<td>You can also access other areas on the Industrial Ethernet from a programming device at the field level.</td>
</tr>
<tr>
<td>Example: Programming device - integrated Switch 3 - Switch 2 - Switch 4 - integrated Switch CPU 41x-5H PN/DP ③ - on IO device ET 200⑧.</td>
<td></td>
</tr>
</tbody>
</table>
The graphic shows

<table>
<thead>
<tr>
<th>The graphic shows</th>
<th>Examples of connection paths</th>
</tr>
</thead>
<tbody>
<tr>
<td>The IO controller of CPU 41x5 PN/DP ① sets up PROFINET IO system 1 and directly controls devices on Industrial Ethernet and PROFIBUS.</td>
<td>At this point, you can see the IO feature between the IO controller, intelligent device, and the IO devices on Industrial Ethernet:</td>
</tr>
<tr>
<td></td>
<td>• The CPU 41x-5 PN/DP ① is the IO controller for the IO device ET 200 ⑤, for Switch 3 and for the intelligent device CPU 317-2 PN/DP ④.</td>
</tr>
<tr>
<td></td>
<td>• The CPU 41x-5H PN/DP ① is also the master for the DP slave ⑩ via the IE/PB Link.</td>
</tr>
<tr>
<td>The fault-tolerant system, consisting of CPU 41x-5H PN/DP ② + ③, sets up PROFINET system 2 as IO controller. A one-sided IO device is operated in system redundancy in addition to IO devices at this IO controller.</td>
<td>The fault-tolerant system, consisting of CPU 41x-5H PN/DP ② + ③, sets up PROFINET system 2 as IO controller. A one-sided IO device is operated in system redundancy on this IO controller in addition to IO devices.</td>
</tr>
<tr>
<td></td>
<td>Here you see that a fault-tolerant system can operate system-redundant IO devices as well as a one-sided IO device:</td>
</tr>
<tr>
<td></td>
<td>• The fault-tolerant system is the IO controller for both system-redundant IO devices ET 200 ⑦ + ⑧ as well as the one-sided IO device ⑨.</td>
</tr>
</tbody>
</table>

Further information

You will find further information about PROFINET in the documents listed below:

- In the From PROFIBUS DP to PROFINET IO programming manual. This manual also provides a clear overview of the new PROFINET blocks and system status lists.
8.3 Blocks in PROFINET IO

Compatibility of the New Blocks

For PROFINET IO, some new blocks were created, among other things, because larger configurations are now possible with PROFINET. You can also use the new blocks with PROFIBUS.

Comparison of the system and standard functions of PROFINET IO and PROFIBUS DP

For CPUs with an integrated PROFINET interface, the table below provides you with an overview of the following functions:

- System and standard functions for SIMATIC that you may need to replace when migrating from PROFIBUS DP to PROFINET IO.
- New system and standard functions

<table>
<thead>
<tr>
<th>Blocks</th>
<th>PROFINET IO</th>
<th>PROFIBUS DP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFC 13 &quot;DPNRM_DG&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Reading diagnostics data of a DP slave</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFC 58 &quot;WR_REC&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>SFC 59 &quot;RD_REC&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Write/read record in the I/O devices</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFB 52 &quot;RDREC&quot;</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>SFB 53 &quot;WRREC&quot;</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Read/write record</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFB 54 &quot;RALRM&quot;</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Evaluating alarms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFB 81 &quot;RD_DPAR&quot;</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Reading predefined parameters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFC 5 &quot;GADR_LGC&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Determining the start address of a module</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFC 70 &quot;GEO_LOG&quot;</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Determining the start address of a module</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
8.3 Blocks in PROFINET IO

<table>
<thead>
<tr>
<th>Blocks</th>
<th>PROFINET IO</th>
<th>PROFIBUS DP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFC 49 &quot;LGC_GADR&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Determining the slot that</td>
<td>Replacement: SFC 71</td>
<td></td>
</tr>
<tr>
<td>belongs to a logical address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFC 71 &quot;LOG_GEO&quot;</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Determining the slot that</td>
<td></td>
<td></td>
</tr>
<tr>
<td>belongs to a logical address</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The following table provides an overview of the system and standard functions for SIMATIC, whose functionality must be implemented by other functions when converting from PROFIBUS DP to PROFINET IO.

Table 8-2 System and standard functions of PROFIBUS DP that can be emulated in PROFINET IO

<table>
<thead>
<tr>
<th>Blocks</th>
<th>PROFINET IO</th>
<th>PROFIBUS DP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFC 54 &quot;RD_DPARM&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Reading predefined parameters</td>
<td>Replacement: SFB 81 &quot;RD_DPAR&quot;</td>
<td></td>
</tr>
<tr>
<td>SFC 55 &quot;WR_PARM&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Writing dynamic parameters</td>
<td>Emulation by means of SFB 53</td>
<td></td>
</tr>
<tr>
<td>SFC 56 &quot;WR_DPARM&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Writing predefined parameters</td>
<td>Emulation by means of SFB 81 and SFB 53</td>
<td></td>
</tr>
<tr>
<td>SFC 57 &quot;PARM_MOD&quot;</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Assigning module parameters</td>
<td>Emulation by means of SFB 81 and SFB 53</td>
<td></td>
</tr>
</tbody>
</table>

The following SIMATIC system function is not supported for PROFINET IO:
- SFC 103 "DP_TOPOL" Determine the bus typology in a DP master

**Comparison of the Organization Blocks of PROFINET IO and PROFIBUS DP**

The following table lists the changes to OBs 83 und OB 86:

Table 8-3 OBs in PROFINET IO and PROFIBUS DP

<table>
<thead>
<tr>
<th>Blocks</th>
<th>PROFINET IO</th>
<th>PROFIBUS DP</th>
</tr>
</thead>
<tbody>
<tr>
<td>OB 70 I/O redundancy error,</td>
<td>New</td>
<td>Unchanged</td>
</tr>
<tr>
<td>for fault-tolerant systems</td>
<td></td>
<td></td>
</tr>
<tr>
<td>only</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OB 83 Removing and inserting</td>
<td>New error information</td>
<td>Unchanged</td>
</tr>
<tr>
<td>modules at runtime</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OB 86 Rack failure</td>
<td>New error information</td>
<td>Unchanged</td>
</tr>
</tbody>
</table>

**Detailed information**

For more information about the blocks, refer to the manual *System Software for S7-300/400 System and Standard Functions.*
8.4 System status lists for PROFINET IO

Introduction
The CPU makes certain information available and stores this information in the "System status list".

The system status list describes the current status of the automation system. It provides an overview of the configuration, the current parameter assignment, the current statuses and sequences in the CPU, and the assigned modules.

The system status list data can only be read, but not be changed. The system status list is a virtual list that is compiled only on request.

From a system status list you receive the following information via the PROFINET IO system:
- System data
- Module status information in the CPU
- Diagnostic data from a module
- Diagnostic buffer

Compatibility of the new system status lists
For PROFINET IO, some new system status lists were created, among other things, because larger configurations are now possible with PROFINET.

You can also use these new system status lists with PROFIBUS.

You can continue to use a known PROFIBUS system status list that is also supported by PROFINET. If you use a system status list in PROFINET that PROFINET does not support, an error code is returned in RET_VAL (8083: Index wrong or not permitted).

Comparison of the system status lists of PROFINET IO and PROFIBUS DP

Table 8-4 Comparison of the system status lists of PROFINET IO and PROFIBUS DP

<table>
<thead>
<tr>
<th>SSL-ID</th>
<th>PROFINET IO</th>
<th>PROFIBUS DP</th>
<th>Applicability</th>
</tr>
</thead>
<tbody>
<tr>
<td>W#16#0591</td>
<td>Yes Parameter adr1 changed</td>
<td>Yes</td>
<td>Module status information for the interfaces of a module</td>
</tr>
<tr>
<td>W#16#0C91</td>
<td>Yes, internal interface Parameter adr1/adr2 and set/actual type identifier changed No, external interface</td>
<td>Yes, internal interface No, external interface</td>
<td>Module status information of a module in a central configuration or at an integrated DP or PROFIBUS interface, or at an integrated DP interface using the logical address of the module.</td>
</tr>
<tr>
<td>W#16#4C91</td>
<td>No</td>
<td>No, internal interface Yes, external interface</td>
<td>Module status information of a module attached to an external DP or PROFIBUS interface using the start address.</td>
</tr>
</tbody>
</table>
**PROFINET**

**8.5 Device replacement without removable medium/programming device**

<table>
<thead>
<tr>
<th>SSL-ID</th>
<th>PROFINET IO</th>
<th>PROFIBUS DP</th>
<th>Applicability</th>
</tr>
</thead>
</table>
| W#16#0D91 | Yes Parameter adr1 changed  
No, external interface          | Yes               | Module status information of all modules in the specified rack/station       |
| W#16#0696 | Yes, internal interface  
No, external interface          | No                | Module status information of all submodules on an internal interface of a module using the logical address of the module, not possible for submodule 0 (= module) |
| W#16#0C75 | Yes, parameter adr1 changed        | Yes               | Communication status between the fault-tolerant system and a switched DP slave/PN device |
| W#16#0C96 | Yes, internal interface  
No, external interface          | Yes, internal interface  
No, external interface          | Module status information of a submodule using the logical address of this submodule |
| W#16#xy92 | No Replacement: SSL-ID W#16#0x94 | Yes               | Rack/stations status information Replace this system status list with the system status list with ID W#16#xy94 in PROFIBUS DP, as well. |
| W#16#0x94 | Yes, internal interface  
No, external interface          | Yes, internal interface  
No, external interface          | Rack/station status information |

**Detailed information**

For detailed descriptions of the individual system status lists, refer to the manual *System Software for S7-300/400 System and Standard Functions.*

### 8.5 Device replacement without removable medium/programming device

IO devices having this function can be replaced in a simple manner:

- A removable medium (e.g. SIMATIC Micro Memory Card) with stored device name is not required.
- The PN-IO topology must be configured in STEP 7.
- The device name does not have to be assigned with the programming device.

The replacement IO device is now assigned a device name from the IO controller. It is no longer assigned using a removable medium or programming device. The IO controller uses the configured topology and the relations determined by the IO devices. The configured target topology must match the actual topology.

Before reusing IO devices that you already had in operation, reset these to factory settings.

**Additional information**

8.6 Shared Device

The "Shared Device" functionality facilitates distribution of the submodules of an IO device to different IO controllers. An intelligent IO device can also be operated as shared device.

Prerequisite for using the "Shared Device" function is that the IO controller and shared device are located on the same Ethernet subnet.

The IO controllers can be located in the same or different STEP 7 projects. If they are located in the same STEP 7 project, a consistency check is initiated automatically.

Note

Note that the power modules and electronic modules belonging to the same potential group of a shared IO device (e.g. ET 200S) must be assigned to the same IO controller in order to enable the diagnosis of load voltage failure.

Additional information


8.7 Media redundancy

Media redundancy is a function that ensures network and system availability. Redundant transmission links in a ring topology ensure that an alternative communication path is always available if a transmission link fails.

You can enable the media redundancy protocol (MRP) for IO devices, switches, and CPUs with PROFINET interface V6.0 or higher. MRP is a component of PROFINET standardization to IEC 61158.

Installing a ring topology

To set up a ring topology with media redundancy, you must join both free ends of a line network topology in the same device. You join the line topology to form a ring via two ports (ring ports, port ID "R") of a device connected to the ring. Specify the ring ports in the configuration data of the relevant device.

Topology

You can also combine system redundancy under PROFINET with other PROFINET functions.
System redundancy with media redundancy

![Diagram of system redundancy with media redundancy]

**Note**
RT communication is interrupted (station failure) if the reconfiguration time of the ring is greater than the selected response monitoring time of the IO device. This means that you should select a response monitoring time of the IO device of sufficient length. The same applies to IO devices configured with MRP outside the ring.

**Additional information**
8.8 System redundancy

System redundancy is the connection of IO devices via PROFINET with a communication connection between each IO device and each of the two fault-tolerant CPUs. This communication connection can be set up using any topological interconnection. The topology of a system alone does not indicate if an IO device is integrated in system redundancy.

Contrary to a one-sided connection of IO devices, the failure of a CPU does not result in the failure of the IO devices connected with this CPU.

Requirement

You need the following component versions to set up a fault-tolerant system with system-redundant I/Os:

- CPU 41x-5H PN/DP as of version 6.0
- IM 153-4BA00 as of version 4.0
- STEP7 as of V5.5, SP2 HF1

Configuration

The figure below shows a configuration with two IO devices connected in system redundancy.

![Figure 8-2 S7-400H system with IO devices connected in system redundancy](image-url)
This topology has the following advantage: The entire system can continue to operate in case of an interrupted connection, no matter where it occurs. One of the two communication connections of the IO devices will always remain intact. The IO devices that were redundant until now will continue operating as one-sided IO devices.

The figure below shows the view in STEP7, the logical view and the physical view of the configuration with two integrated IO devices in system redundancy. Note that the view in STEP7 does not exactly match the physical view.

Figure 8-3  System redundancy in different views
Commissioning a system-redundant configuration

It is imperative that you assign unique names during commissioning.

Proceed as follows when you change or reload a project:

1. Set the fault-tolerant system to STOP on both sides.
2. Reset the standby CPU memory.
3. Download the new project to the master CPU.
4. Start the fault-tolerant system.

Note
Using the topology editor

Use the topology editor in HW Config.

Maximum number of IO devices

You can connect up to 256 IO devices to both integrated PROFINET interfaces. These can be configured for one-sided or redundant mode. The station numbers must be unique for both PROFINET interfaces and between 1 and 256.
PN/IO with system redundancy

The figure below shows the system-redundant connection of three IO devices using one switch. Two additional IO devices are also connected in system redundancy.

Figure 8-4  PN/IO with system redundancy
The figure below shows the system-redundant connection of nine IO devices using three switches. This configuration, for example, allows you to arrange IO devices in several cabinets.

![Diagram of system redundancy](image)

Figure 8-5  PN/IO with system redundancy

**Note**

**Logical structure and topology**

The topology itself does not determine if IO devices are connected one-sided or in a configuration with system redundancy. This is determined in the course of configuration. You can configure the IO devices in the first figure as one-sided instead of the system-redundant setup.
Consistent data

Overview

Data that belongs together in terms of its content and describe a process state at a specific point in time is known as consistent data. In order to maintain data consistency, do not modify or update the data during their transfer.

Example 1:

In order to provide a consistent image of the process signals to the CPU for the duration of cyclic program processing, the process signals are written to the process image of inputs prior to program execution, or the processing results are written to the process image of outputs after program execution. Subsequently, during program processing when the inputs (I) and outputs (O) operand areas are addressed, the user program addresses the internal memory area of the CPU on which the process image is located instead of directly accessing the signal modules.

Example 2:

Inconsistency may develop when a communication block, such as SFB 14 "GET" or SFB 15 "PUT", is interrupted by a process alarm OB of higher priority. If the user program modifies any data of this process alarm OB which in part have already been processed by the communication block, certain parts of the transferred data will have retained their original status which was valid prior to process alarm processing, while others represent data from after process alarm processing.

This results in inconsistent data, i.e. data which are no longer associated.

SFC 81 "UBLKMOV"

Use SFC 81 "UBLKMOV" to copy the content of a memory range, the source area, consistently to another memory range, the target range. The copy operation cannot be interrupted by other operating system activities.

SFC 81 "UBLKMOV" enables you to copy the following memory areas:

- Bit memory
- DB contents
- Process input image
- Process output image

The maximum amount of data you can copy is 512 bytes. Make allowances for the CPU-specific restrictions listed in the instruction list.

Since copying cannot be interrupted, the alarm response times of your CPU may increase when using SFC 81 "UBLKMOV".
The source and destination areas must not overlap. If the specified destination area is larger than the source area, the function only copies the amount of data contained in the source area to the destination area. If the specified destination area is smaller than the source area, the function only copies as much data as can be written to the destination area.

For information on SFC 81, refer to the corresponding online help and to the "System and Standard Functions" manual.

9.1 Consistency of communication blocks and functions

On the S7-400H, communication jobs are not processed in the cycle control point but rather in fixed time slices during the program cycle.

The byte, word and double word data formats can always be processed consistently in the system, in other words, the transmission or processing of 1 byte, 1 word = 2 bytes or 1 double word = 4 bytes cannot be interrupted.

If the user program calls communication blocks, such as SFB 12 "BSEND" and SFB 13 "BRCV", which are only used in pairs and access shared data, access to this data area can be coordinated by the user by means of the "DONE" parameter, for example. The consistency of data transmitted locally with these communication blocks can thus be ensured in the user program.

In contrast, S7 communication functions do not require a block such as SFB 14 "GET", SFB 15 "PUT", in the user program of the target device. Here, you must make allowance for the volume of consistent data in the programming phase.

Access to work memory of the CPU

The communication functions of the operating system access the CPU's work memory in fixed block lengths. Blocks for S7-400H CPUs have a variable length of up to 472 bytes.

This ensures that the interrupt response time is not prolonged due to communication load. Because this access is performed asynchronously to the user program, you cannot transmit an unlimited number of bytes of consistent data.

The rules to ensure data consistency are described below.
9.2 Consistency rules for SFB 14 "GET" or read variable, and SFB 15 "PUT" or write variable

SFB 14

The data are received consistently if you observe the following points:

Evaluate the entire, currently used part of the receive area RD_i before you activate a new request.

SFB 15

When a send operation is initiated (rising edge at REQ), the data to be sent from the send areas SD_i are copied from the user program. You can write new data to these areas after the block call command without corrupting the current send data.

Note

Completion of transfer

The send operation is not completed until the status parameter DONE assumes value 1.

9.3 Consistent reading and writing of data from and to DP standard slaves/IO devices

Reading data consistently from a DP standard slave using SFC 14 "DPRD_DAT"

Using SFC14 "DPRD_DAT" (read consistent data of a DP standard slave), you can consistently read the data of a DP standard slave of IO device.

The data read is entered into the destination area defined by RECORD if no error occurs during data transfer.

The destination area must have the same length as the one you have configured for the selected module with STEP 7.

By calling SFC 14 you can only access the data of one module/DP identifier at the configured start address.

For information on SFC 14, refer to the corresponding Online Help and to the "System and Standard Functions" manual.

Note

Evaluate the entire currently used part of the receive area RD_i before you activate a new job.
Writing data consistently to a DP standard slave using SFC 15 "DPWR_DAT"

Using SFC 15 "DPWR_DAT" (write consistent data to a DP standard slave), you transmit the data in RECORD consistently to the addressed DP standard slave or IO device.

The source area must have the same length as the one you configured for the selected module with STEP 7.

For information on SFC 15, refer to the corresponding Online Help and to the “System and Standard Functions” manual.

Note
When a send operation is activated (positive edge at REQ), the data to be transmitted from the send areas SD_i is copied from the user program. You can write new data to these areas after the block call command without corrupting the current send data.

Upper limits for the transfer of consistent user data to a DP slave

The PROFIBUS DP standard defines upper limits for the transfer of consistent user data to a DP slave. For this reason a maximum of 64 words = 128 bytes of user data can be consistently transferred in a block to the DP standard slave.

You can define the length of the consistent area in your configuration. In the special identification format (SIF), you can define a maximum length of consistent data of 64 words = 128 bytes; 128 bytes for inputs and 128 bytes for outputs. A greater length is not possible.

This upper limit applies only to pure user data. Diagnostics and parameter data are grouped to form complete data records, and are thus always transferred consistently.

In the general identification format (GIF), you can define a maximum length of consistent data of 16 words = 32 bytes; 32 bytes for inputs, and 32 bytes for outputs. A greater length is not possible.

In this context, consider that a CPU 41x operating as DP slave generally has to support its configuration at an external master (implementation by means of GSD file) using the general identification format. A CPU 41x operated as DP slave thus supports only a maximum length of 16 words = 32 bytes in its transfer memory for PROFIBUS DP.

Note
The PROFIBUS DP standard defines the upper limits for transmission of consistent user data. Typical DP standard slaves adhere to this upper limit. Older CPUs (<1999) had CPU-specific restrictions in terms of the transmission of consistent user data. The maximum length of data this CPU can consistently read and write to and from a DP standard slave is specified in your technical specifications, keyword "DP Master – User data per DP slave". With this value, newer CPUs exceed the length of data that a DP standard slave provides or receives.
Upper limits of the length of consistent user data transmitted to an IO Device

The length of consistent user data that you can transmit to an IO device is limited to 1025 bytes (= 1024 bytes user data + 1 byte secondary value). Irrespective of whether you can transmit more than 1024 bytes to an IO device, the transmission of consistent data is still limited to 1024 bytes.

When operating in PN-IO mode, the length of data transmission via CP 443-1 is limited to 240 bytes.

Consistent data access without using SFC 14 or SFC 15

Consistent data access > 4 bytes is also possible without using SFC 14 or SFC 15. The data area of a DP slave or IO device to be transmitted consistently is transferred to a process image partition. The data in this area are thus always consistent. You can then access the process image partition using the load/transfer commands (L EW 1, for example). This provides a particularly convenient and efficient (low runtime load) method of accessing consistent data. Thus an efficient integration and parameterization of, for example, drives or other DP slaves is made possible.

Any direct access to a consistently configured data area, e.g. L PEW or T PAW, does not result in an I/O area access error.

Important aspects in the conversion from the SFC14/15 solution to the process image solution are:

- SFC 50 "RD_LGADR" outputs different address areas with the SFC 14/15 method as with the process image method.
- PROFIBUS DP via internal interface:
  When converting from the SFC14/15 method to the process image method, it is not advisable to use the system functions and the process image concurrently. Although the process image is updated when writing with system function SFC15, this is not the case when reading. In other words, consistency between the values of the process image and of the system function SFC14 is not ensured.
- PROFIBUS DP via CP 443-5 ext:
  If you use a CP 443–5 ext, the parallel use of system functions and process image causes the following errors: Read/write access to the process image is blocked, and/or SFC 14/15 is no longer able to perform any read/write access operations.

Note

Forcing variables

It is not allowed to force variables in the I/O or process image range of a DP slave or IO device and that belong to a consistency range. The user program may overwrite these variables in spite of the force job.
Example:

The example of the process image partition 3 "PIP 3" below shows a possible configuration in HW Config. Requirement: The process image was previously updated by means of SFC 26/27 call, or the update of the process image was linked to an OB.

- PIP 3 at output: Those 50 bytes are stored consistently in process image partition 3 (drop down list box "Consistent over > Total length"), and can thus be read by means of standard "Load input xy" commands.

- Selecting "Process image -> ---" under Input in the drop down list box means: no storage in a process image. You must work with the system functions SFC14/15.
10.1 Overview of the memory concept of S7-400H CPUs

Organization of Memory Areas

The memory of the S7-400H CPUs can be divided into the following areas:

<table>
<thead>
<tr>
<th>Area</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load memory, external</td>
<td>RAM with battery backup or non-volatile Flash Memory</td>
</tr>
<tr>
<td>Load memory integrated</td>
<td>RAM with battery backup</td>
</tr>
<tr>
<td>Work memory code</td>
<td>For program, RAM with battery backup, Process image of inputs and outputs, Diagnostics buffer</td>
</tr>
<tr>
<td>Work memory data</td>
<td>for data, RAM with battery backup, Local data stack</td>
</tr>
<tr>
<td>System memory</td>
<td>contains bit memories, timers, counters block stack and interrupt stack, RAM with battery backup</td>
</tr>
</tbody>
</table>

Load memory for project data (blocks, configuration and programming data)

Work memory for executable blocks

Figure 10-1 Memory areas of the S7-400H CPUs
Memory concept

10.1 Overview of the memory concept of S7-400H CPUs

Memory types of the S7-400H CPUs

- Load memory for the project data, e.g. blocks, configuration, and parameter settings.
- Work memory for the runtime-relevant blocks (logic blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as bit memories, timers and counters. System memory also contains the block stack and interrupt stack.
- System memory of the CPU also provides a temporary memory area (local data stack, diagnostics buffer, and communication resources) that is assigned to the program for the temporary data of a called block. This data is only valid as long as the block is active.

By changing the default values for the process image, local data, diagnostics buffer, and communication resources (see object properties of the CPU in HW Config), you can influence the work memory available to the runtime-relevant blocks.

Note

Please note the following if you expand the process image of a CPU. Reconfigure the modules whose addresses have to be above the highest address of the process image so that the new addresses are still above the highest address of the expanded process image.

Important note for CPUs after the parameter settings for the allocation of RAM have been changed

If you change the work memory allocation by modifying parameters, this work memory is reorganized when you load system data into the CPU. As a consequence, the data blocks generated by means of SFC are deleted and the remaining data blocks are initialized with values from load memory.

The amount of work memory that is made available for logic or data blocks during the download of system data is adapted if you modify the following parameters:

- Size of the process image (byte-oriented; in the "Cycle/Clock Memory" tab)
- Communication resources (in the "Memory" tab)
- Size of the diagnostics buffer ("Diagnostics/Clock" tab)
- Number of local data for all priority classes ("Memory" tab)
Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory on the CPU, you must take into consideration the following memory requirements when assigning parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Required working memory</th>
<th>In code/data memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size of the process image</td>
<td>20 bytes per byte in the process image of inputs</td>
<td>Code memory</td>
</tr>
<tr>
<td>(inputs)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size of the process image</td>
<td>20 bytes per byte in the process image of inputs</td>
<td>Code memory</td>
</tr>
<tr>
<td>(outputs)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Communication resources</td>
<td>72 bytes per communication job</td>
<td>Code memory</td>
</tr>
<tr>
<td>(communication jobs)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size of the diagnostics buffer</td>
<td>32 bytes per entry in the diagnostics buffer</td>
<td>Code memory</td>
</tr>
<tr>
<td>Quantity of local data</td>
<td>1 byte per byte of local data</td>
<td>Data memory</td>
</tr>
</tbody>
</table>

Flexible memory space

- Work memory:
  The capacity of the work memory is determined by selecting the appropriate CPU from the graded range of CPUs.

- Load memory:
  The integrated load memory is sufficient for small and medium-sized programs.
  The load memory can be increased for larger programs by inserting the RAM memory card.
  Flash memory cards are also available to ensure that programs are retained in the event of a power failure even without a backup battery. Flash memory cards (8 MB or more) are also suitable for sending and carrying out operating system updates.

Backup

- The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.
10.1 Overview of the memory concept of S7-400H CPUs
This chapter features an introduction to the subject of S7-400H fault-tolerant systems. You will learn the basic terms that are used in describing how fault-tolerant systems operate. Following that, you will receive information on fault-tolerant system states. They depend on the operating states of the different fault-tolerant CPUs, which will be described in the next section.

In describing these operating states, this section concentrates on the behavior that differs from a standard CPU. You will find a description of the standard behavior of a CPU in the corresponding operating mode in the Programming with STEP 7 manual.

The final section provides details on the modified time response of fault-tolerant CPUs.

11.1 Introduction

The S7-400H consists of two redundantly configured subsystems that are synchronized via fiber-optic cables.

Both subsystems create a fault-tolerant automation system operating with a two-channel (1-out-of-2) structure based on the “active redundancy” principle.

What does active redundancy mean?

Active redundancy means that all redundant resources are constantly in operation and simultaneously involved in the execution of the control task.

For the S7-400H this means that the user programs in both CPUs are identical and executed synchronously by the CPUs.

Convention

To identify the two subsystems, we use the traditional expressions of “master” and "reserve" for dual-channel fault-tolerant systems in this description. The reserve always processes events in synchronism with the master, and does not explicitly wait for any errors before doing so.

The distinction made between the master and reserve CPUs is primarily important for ensuring reproducible error reactions. For example, the reserve CPU may go into STOP when the redundant link fails, while the master CPU remains in RUN.
11.1 Introduction

Master/reserve assignment

When the S7-400H is initially switched on, the CPU that started up first assumes master mode, and the partner CPU assumes reserve mode.

The preset master/reserve assignment is retained when both CPUs power up simultaneously.

The master/reserve assignment changes when:
1. The reserve CPU starts up before the master CPU (interval of at least 3 s)
2. The master CPU fails or goes into STOP in redundant system mode
3. No error was found in ERROR-SEARCH mode (see also section ERROR-SEARCH mode (Page 128))
4. Programmed master-standby switchover with SFC 90 "H_CTRL"

Synchronizing the subsystems

The master and reserve CPUs are linked by fiber-optic cables. Both CPUs maintain event-synchronous program execution via this connection.

Synchronization is performed automatically by the operating system and has no effect on the user program. You create your program in the same way as for standard S7-400 CPUs.

Event-driven synchronization procedure

The "event-driven synchronization" procedure patented by Siemens was used for the S7-400H. This procedure has proved itself in practice and has already been used for the S5-115H and S5-155H controllers.

Event-driven synchronization means that the master and reserve always synchronize their data when an event occurs which may lead to different internal states of the subsystems.

The master and reserve CPUs are synchronized when:
- There is direct access to the I/O
- Interrupts occur
- User timers (e.g. S7 timers) are updated
- Data is modified by communication functions
Continued bumpless operation even if redundancy of a CPU is lost

The event-driven synchronization method ensures bumpless continuation of operation by the reserve CPU even if the master CPU fails.

Self-test

Malfunctions or errors must be detected, localized and reported as quickly as possible. Consequently, extensive self-test functions have been implemented in the S7-400H that run automatically and entirely in the background.

The following components and functions are tested:
- Coupling of the central racks
- Processor
- Internal memory of the CPU
- I/O bus

If the self-test detects an error, the fault-tolerant system tries to eliminate it or to suppress its effects.

For detailed information on the self-test, refer to section Self-test (Page 130).

11.2 System states of the S7–400H

11.2.1 The system states of the S7–400H

The system states of the S7-400H result from the operating states of the two CPUs. The term "system state" is used as a simplified term which identifies the concurrent operating states of the two CPUs.

Example: Instead of "the master CPU is in RUN and the reserve CPU is in LINK-UP mode" we say "the S7-400H system is in link-up mode".

Overview of system states

The table below provides an overview of the possible states of the S7-400H system.

<table>
<thead>
<tr>
<th>System states of the S7–400H</th>
<th>Operating states of the two CPUs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Master</td>
</tr>
<tr>
<td>Stop</td>
<td>STOP</td>
</tr>
<tr>
<td>Start-up</td>
<td>STARTUP</td>
</tr>
<tr>
<td>Single mode</td>
<td>RUN</td>
</tr>
</tbody>
</table>
11.2 System states of the S7–400H

<table>
<thead>
<tr>
<th>System states of the S7–400H</th>
<th>Operating states of the two CPUs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Master</td>
</tr>
<tr>
<td>Link-up</td>
<td>RUN</td>
</tr>
<tr>
<td>Update</td>
<td>RUN</td>
</tr>
<tr>
<td>Redundant</td>
<td>RUN</td>
</tr>
<tr>
<td>Hold</td>
<td>HOLD</td>
</tr>
</tbody>
</table>

11.2.2 Displaying and changing the system state of a fault-tolerant system

Procedure:

1. In SIMATIC Manager, select a CPU with existing MPI connection.
2. Select the PLC > Operating mode menu command.

Result:

The "Operating mode" dialog shows the current system state of the fault-tolerant system, the operating states of the individual CPUs, as well as the current position of the mode switches on the modules.

The CPU that was selected in SIMATIC Manager when the menu command was executed is the first one displayed in the table.
Changing the system state:

The options of changing the system state depend on the current system state of the fault-tolerant system.

11.2.3 System status change from the STOP system state

Requirement

You have selected one of the two CPUs in SIMATIC Manager and opened the "Operating mode" dialog using the PLC > Operating state menu command.

Changing to redundant system mode (starting the fault-tolerant system)

1. Select the fault-tolerant system in the table.
2. Select the Restart button (warm restart).

Result:

The CPU displayed first in the table starts up as master CPU. Then the second CPU starts up and will become the standby CPU after link-up and update operations.
Changing to standalone mode (starting only one CPU)

1. In the table, select the CPU you want to start up.
2. Select the Restart (warm restart) button.

11.2.4 System status change from the standalone mode system status

Requirements:
- You have opened the “Operating state” dialog using the PLC > Operating state menu command in SIMATIC Manager.
- The standby CPU is not in ERROR-SEARCH operating state.

Changing to redundant system state (starting the standby CPU)

1. In the table, select the CPU that is in STOP, or the fault-tolerant system.
2. Select the Restart button (warm restart).

Changing to system status STOP (stopping the running CPU)

1. In the table, select the CPU that is in RUN, or the fault-tolerant system.
2. Select the Stop button.
11.2.5 System status change from the redundant system state

Requirement:
You have opened the "Operating state" dialog using the PLC > Operating state menu command in SIMATIC Manager.

Changing to STOP system state (stopping the fault-tolerant system)
1. Select the fault-tolerant system in the table.
2. Select the Stop button.

Changing to standalone mode (stop of one CPU)
1. In the table, select the CPU that you want to stop.
2. Select the Stop button.

Result:
The selected CPU goes into the STOP state, while the other CPU remains in RUN state; the fault-tolerant system continues operating in standalone mode.

11.2.6 System diagnostics of a fault-tolerant system

The diagnose hardware function identifies the state of the entire fault-tolerant system.

Procedure:
1. Select the fault-tolerant station in SIMATIC Manager.
2. Select the PLC > Diagnose hardware menu command.
3. In the "Select CPU" dialog, select the CPU and confirm with OK.

Result:
The operating state of the selected CPU can be identified based on the display of the selected CPU in the "Diagnose hardware" dialog:

<table>
<thead>
<tr>
<th>CPU icon</th>
<th>Operating state of the respective CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>![Master CPU icon]</td>
<td>Master CPU is in RUN state</td>
</tr>
<tr>
<td>![Standby CPU icon]</td>
<td>Standby CPU is in RUN state</td>
</tr>
</tbody>
</table>
### System and operating states of the S7–400H

#### 11.3 The operating states of the CPUs

<table>
<thead>
<tr>
<th>CPU icon</th>
<th>Operating state of the respective CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Master CPU icon" /></td>
<td>Master CPU is in STOP state</td>
</tr>
<tr>
<td><img src="image2" alt="Standby CPU icon" /></td>
<td>Standby CPU is in STOP state</td>
</tr>
<tr>
<td><img src="image3" alt="Master CPU icon" /></td>
<td>Master CPU is in STARTUP state</td>
</tr>
<tr>
<td><img src="image4" alt="Standby CPU icon" /></td>
<td>Standby CPU is in LINK-IN or UPDATE state</td>
</tr>
<tr>
<td><img src="image5" alt="Standby CPU icon" /></td>
<td>Standby CPU is in ERROR-SEARCH operating state</td>
</tr>
<tr>
<td><img src="image6" alt="Error icon" /></td>
<td>Malfunction of the master CPU or of a module parameterized by it.</td>
</tr>
<tr>
<td><img src="image7" alt="Error icon" /></td>
<td>Malfunction of the standby CPU, or of a module parameterized by it.</td>
</tr>
<tr>
<td><img src="image8" alt="Maintenance icon" /></td>
<td>Maintenance required on master CPU</td>
</tr>
<tr>
<td><img src="image9" alt="Maintenance icon" /></td>
<td>Maintenance required on standby CPU</td>
</tr>
<tr>
<td><img src="image10" alt="Maintenance request icon" /></td>
<td>Maintenance request on master CPU</td>
</tr>
<tr>
<td><img src="image11" alt="Maintenance request icon" /></td>
<td>Maintenance request on standby CPU</td>
</tr>
</tbody>
</table>

**Note**

The view is not updated automatically in the Online view. Use the F5 function key to view the current operating mode.
11.3 The operating states of the CPUs

Operating states describe the behavior of the CPUs at any given point in time. Knowledge of the operating states of the CPUs is useful for programming the startup, test, and error diagnostics.

Operating states from POWER ON to redundant system state

Generally speaking, the two CPUs enjoy equal rights so that either can be the master or the standby CPU. For reasons of legibility, the illustration presumes that the master CPU (CPU 0) is started up before the standby CPU (CPU 1) is switched on.

The following figure shows the operating states of the two CPUs, from POWER ON to redundant system state. The HOLD HOLD mode (Page 128) and ERROR-SEARCH ERROR-SEARCH mode (Page 128) states are a special feature and are not shown.

![Operating states diagram](image)

Figure 11-2 System and operating states of the fault-tolerant system
11.3 The operating states of the CPUs

Explanation of the figure

<table>
<thead>
<tr>
<th>Point</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>After the power supply has been turned on, the two CPUs (CPU 0 and CPU 1) are in STOP state.</td>
</tr>
<tr>
<td>2.</td>
<td>CPU 0 changes to the STARTUP state and executes OB 100 or OB 102 according to the startup mode; see also section STARTUP mode (Page 125).</td>
</tr>
<tr>
<td>3.</td>
<td>If startup is successful, the master CPU (CPU 0) changes to standalone mode. The master CPU executes the user program alone. At the transition to the LINK-UP system state, no block may be opened by the &quot;Monitor&quot; option, and no tag table may be active.</td>
</tr>
<tr>
<td>4.</td>
<td>If the standby CPU (CPU 1) requests LINK-UP, the master and standby CPUs compare their user programs. If any differences are found, the master CPU updates the user program of the standby CPU, see also section LINK-UP and UPDATE modes (Page 126).</td>
</tr>
<tr>
<td>5.</td>
<td>After a successful link-up, updating is started, see section Update sequence (Page 143). The master CPU updates the dynamic data of the standby CPU. Dynamic data includes inputs, outputs, timers, counters, bit memories and data blocks. Following the update, the memories of both CPUs have the same content; see also section LINK-UP and UPDATE modes (Page 126).</td>
</tr>
<tr>
<td>6.</td>
<td>The master and standby CPUs are in RUN after the update. Both CPUs process the user program in synchronous mode. Exception: Master/standby changeover for configuration/program modifications. The redundant system state is only supported with CPUs of the same version and firmware version.</td>
</tr>
</tbody>
</table>

11.3.1 STOP mode

Except for the additions described below, the behavior of S7-400H CPUs in STOP state corresponds to that of standard S7-400 CPUs.

When you download a configuration to one of the CPUs while both are in STOP state, observe the points below:

- Start the CPU to which you downloaded the configuration first in order to set it up for master mode.
- By initiating the system startup request on the programming device, you first start the CPU to which an active connection exists, regardless of the master or standby status.

**Note**

A system startup may trigger a master–standby changeover.

A fault-tolerant CPU can only exit the STOP state with a loaded configuration.

**Memory reset**

The memory reset function affects only the selected CPU. To reset both CPUs, you must reset one and then the other.
11.3.2 STARTUP mode

Except for the additions described below, the behavior of S7-400H CPUs in STARTUP mode corresponds to that of standard S7-400 CPUs.

Startup modes

The fault-tolerant CPUs distinguish between cold restart and warm restart. Fault-tolerant CPUs do not support warm restarts.

Startup processing by the master CPU

The startup system mode of an S7-400H is always processed by the master CPU.

During STARTUP, the master CPU compares the existing I/O configuration with the hardware configuration that you created in STEP 7. If any differences are found, the master CPU reacts in the same way as a standard S7-400 CPU.

The master CPU checks and parameterizes the following:

- the switched I/O devices
- its assigned one-sided I/O devices
11.3 The operating states of the CPUs

Startup of the standby CPU

The standby CPU startup routine does not call an OB 100 or OB 102.

The standby CPU checks and parameterizes the following:

- its assigned one-sided I/O devices

Special features at startup

If the master CPU returns to STOP immediately after transition to RUN during startup of a fault-tolerant system, the standby CPU takes over the master role and continues to start up.

In buffered PowerOn mode of a fault-tolerant system with large configurations, many CPs and/or external DP masters, it may take up to 30 seconds until a requested restart is executed. During this time, the LEDs on the CPU light up successively as follows:

1. All LEDs light up
2. The STOP LED flashes as it does during a memory reset
3. The RUN and STOP LEDs flash for about 2 seconds
4. The RUN LED flashes briefly 2 to 3 times
5. The STOP LED lights up for about 25 seconds
6. The RUN LED restarts flashing

Start up is about to begin.

Additional information

For detailed information on STARTUP mode, refer to the Programming with STEP 7 manual.

11.3.3 LINK-UP and UPDATE modes

The master CPU checks and updates the memory content of the reserve CPU before the fault-tolerant system assumes redundant system mode. This is implemented in two successive phases: link-up and update.

The master CPU is always in RUN mode and the reserve CPU is in LINK-UP or UPDATE mode during the link-up and update phases.

In addition to the link-up and update functions, which are carried out to establish redundant system mode, the system also supports linking and updating in combination with master/reserve changeover.

For detailed information on link-up and updating, refer to section Link-up and update (Page 135).
11.3.4 RUN mode

Except for the additions described below, the behavior of S7-400H CPUs in RUN mode corresponds to that of standard S7-400 CPUs.

The user program is executed by at least one CPU in the following system states:

- Single mode
- Link-up, update
- Redundant

Single mode, link-up, update

In the system states standalone mode, link-up and update, the master CPU is in RUN and executes the user program in standalone mode.

Redundant system mode

The master CPU and standby CPU are always in RUN when operating in redundant system mode. Both CPUs execute the user program in synchronism, and perform mutual checks.

In redundant system mode it is not possible to test the user program with breakpoints.

The redundant system state is only supported with CPUs of the same version and firmware version. Redundancy will be lost if one of the errors listed in the following table occurs.

<table>
<thead>
<tr>
<th>Cause of error</th>
<th>Reaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure of one CPU</td>
<td>Failure and replacement of a CPU (Page 253)</td>
</tr>
<tr>
<td>Failure of the redundant link (synchronization</td>
<td>Failure and replacement of a synchronization</td>
</tr>
<tr>
<td>module or fiber-optic cable)</td>
<td>module or fiber-optic cable (Page 259)</td>
</tr>
<tr>
<td>RAM comparison error</td>
<td>ERROR-SEARCH mode (Page 128)</td>
</tr>
</tbody>
</table>

Redundant use of modules

The following rule applies to the redundant system mode:

Modules interconnected in redundant mode (e.g. DP slave interface module IM 153-2) must be in identical pairs, i.e. the two redundant linked modules have the same order number and product or firmware version.
11.3.5 **HOLD mode**

Except for the additions described below, the behavior of the S7-400H CPU in HOLD mode corresponds to that of a standard S7-400 CPU.

The HOLD mode has an exceptional role, as it is used only for test purposes.

**When is the HOLD mode possible?**

A transition to HOLD is only available during STARTUP and in RUN in single mode.

**Properties**

- Link-up and update operations are not available while the fault-tolerant CPU is in HOLD mode; the reserve CPU remains in STOP and outputs a diagnostics message.
- It is not possible to set breakpoints when the fault-tolerant system is in redundant system mode.

11.3.6 **ERROR-SEARCH mode**

The ERROR-SEARCH mode can only be adopted from the redundant system mode. During troubleshooting, the redundant system state is exited, the other CPU becomes master and continues running in Solo mode.

**Note**

If the master CPU changes to STOP during troubleshooting, the troubleshooting is continued on the standby CPU. However, once troubleshooting is completed, the standby CPU does not start up again.

The following events will trigger ERROR-SEARCH mode:

1. If a one-sided call of OB 121 (on only one CPU) occurs in redundant mode, the CPU assumes a hardware fault and enters ERROR-SEARCH mode. The partner CPU assumes master mode as required, and continues operation in standalone mode.

2. If a checksum error occurs on only one CPU in redundant mode, that CPU enters ERROR-SEARCH mode. The partner CPU assumes master mode as required, and continues operation in standalone mode.

3. If a RAM/POI comparison error is detected in redundant mode, the standby CPU enters ERROR-SEARCH mode (default response), and the master CPU continues operation in standalone mode.

The response to RAM/POI comparison errors can be modified in the configuration (for example, the standby CPU goes into STOP).
4. If a multiple-bit error occurs on a CPU in redundant mode, that CPU will enter ERROR-SEARCH mode. The partner CPU assumes master mode as required, and continues operation in standalone mode.

**But:** OB 84 is called if 2 or more single-bit errors occur on a CPU in redundant operation within 6 months. The CPU does not change to ERROR-SEARCH mode.

5. If synchronization is lost during redundant mode, the standby CPU changes to ERROR-SEARCH mode. The other CPU remains master and continues operation in standalone mode.

The purpose of ERROR-SEARCH mode is to find a faulty CPU. The standby CPU runs the full self-test, while the master CPU remains in RUN. If a hardware fault is detected, the CPU changes to DEFECTIVE state. If no fault is detected the CPU is linked up again. The fault-tolerant system resumes the redundant system state. An automatic master-standby changeover then takes place. This ensures that when the next error is detected in error-search mode, the hardware of the previous master CPU is tested.

For CPU memories extended with FLASH Memory Cards, the following special condition applies: A general reset request is set if the CPU exits the ERROR-SEARCH operating state and is not able to establish a connection to the master CPU, e.g. when both synchronization lines are interrupted. This prevents that the stand-by CPU starts up as second master CPU using the configuration on the FLASH memory card.

No communication is possible, e.g. by means of access from a programming device, while the CPU is in ERROR-SEARCH operating state. The ERROR-SEARCH operating state is indicated by the RUN and STOP LEDs, see Chapter Status and error displays (Page 52).

For additional information on the self-test, refer to Chapter Self-test (Page 130).
11.4 Self-test

Processing the self-test

The CPU executes the complete self-test program after POWER ON without backup, e.g. POWER ON after initial insertion of the CPU or POWER ON without backup battery, and in the ERROR-SEARCH mode.

The self-test takes at least 10 minutes. The larger the load memory used (e.g. the size of the inserted RAM memory card), the longer the self-test.

When the CPU of a fault-tolerant system requests a memory reset and is then shut down with backup power, it performs a self-test even though it was backed up. A memory reset is requested when you remove the memory card, for example.

In RUN the operating system splits the self-test routine into several small program sections ("test slices") which are processed in multiple successive cycles. The cyclic self-test is organized to perform a single, complete pass in a certain time. The default time of 90 minutes can be modified in the configuration.

Response to errors during the self-test

If the self-test returns an error, the following happens:

Table 11-3 Response to errors during the self-test

<table>
<thead>
<tr>
<th>Type of error</th>
<th>System response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware fault without one-sided call of OB 121</td>
<td>The faulty CPU enters the DEFECTIVE state. The fault-tolerant system switches to standalone mode. The cause of the error is written to the diagnostic buffer.</td>
</tr>
<tr>
<td>Hardware fault with one-sided call of OB 121</td>
<td>The CPU with the one-sided OB 121 enters ERROR-SEARCH mode. The fault-tolerant system switches to standalone mode (see below).</td>
</tr>
<tr>
<td>RAM/POI comparison error</td>
<td>The cause of the error is written to the diagnostic buffer. The CPU enters the configured system or operating state (see below).</td>
</tr>
<tr>
<td>Checksum errors</td>
<td>The response depends on the error situation (see below).</td>
</tr>
<tr>
<td>Multiple-bit errors</td>
<td>The faulty CPU enters ERROR-SEARCH mode.</td>
</tr>
</tbody>
</table>

Hardware fault with one-sided call of OB 121

If a hardware fault occurs with a one-sided OB 121 call for the first time since the previous POWER ON without backup, the faulty CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to standalone mode. The cause of the error is written to the diagnostic buffer.
RAM/POI comparison error

If the self-test returns a RAM/POI comparison error, the fault-tolerant system quits redundant mode and the standby CPU enters ERROR-SEARCH mode (in default configuration). The cause of the error is written to the diagnostic buffer.

The response to a recurring RAM/POI comparison error depends on whether the error occurs in the subsequent self-test cycle after troubleshooting or not until later.

Table 11-4 Response to a recurring comparison error

<table>
<thead>
<tr>
<th>Comparison error recurs ...</th>
<th>Reaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>in the first self-test cycle after troubleshooting</td>
<td>The standby CPU first enters ERROR-SEARCH mode, and then goes into STOP. The fault-tolerant system switches to standalone mode.</td>
</tr>
<tr>
<td>after two or more self-test cycles after troubleshooting</td>
<td>Standby CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to standalone mode.</td>
</tr>
</tbody>
</table>

Checksum errors

When a checksum error occurs for the first time after the last POWER ON without backup, the system reacts as follows:

Table 11-5 Reaction to checksum errors

<table>
<thead>
<tr>
<th>Time of detection</th>
<th>System response</th>
</tr>
</thead>
<tbody>
<tr>
<td>During the startup test after POWER ON</td>
<td>The faulty CPU enters the DEFECTIVE state. The fault-tolerant system switches to standalone mode.</td>
</tr>
<tr>
<td>In the cyclic self-test (STOP or standalone mode)</td>
<td>The error is corrected. The CPU remains in STOP or in standalone mode.</td>
</tr>
<tr>
<td>In the cyclic self-test (redundant system mode)</td>
<td>The error is corrected. The faulty CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to standalone mode.</td>
</tr>
<tr>
<td>In the ERROR-SEARCH mode</td>
<td>The faulty CPU enters the DEFECTIVE state.</td>
</tr>
<tr>
<td>Single-bit errors</td>
<td>The CPU calls OB 84 after detection and elimination of the error.</td>
</tr>
</tbody>
</table>

The cause of the error is written to the diagnostic buffer.

In an F system, the F program is informed that the self-test has detected an error the first time a checksum error occurs in STOP or standalone mode. The reaction of the F program to this is described in the *S7-400F and S7-400FH Automation Systems* manual.
Hardware fault with one-sided call of OB 121, checksum error, second occurrence

A CPU 41x–5H reacts to a second occurrence of a hardware fault with a one-sided call of OB 121 and to checksum errors as set out in the table below, based on the various operating modes of the CPU 41x–5H.

<table>
<thead>
<tr>
<th>Error</th>
<th>CPU in standalone mode</th>
<th>CPU in stand-alone mode</th>
<th>CPU in redundant mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware fault with one-sided call of OB 121</td>
<td>OB 121 is executed</td>
<td>OB 121 is executed</td>
<td>The faulty CPU enters ERROR-SEARCH mode. The fault-tolerant system switches to standalone mode.</td>
</tr>
<tr>
<td>Checksum errors</td>
<td>The CPU enters the DEFECTIVE state if two errors occur within two successive test cycles (configure the length of the test cycle in HW Config).</td>
<td>The CPU enters the DEFECTIVE state if two errors occur within two successive test cycles (configure the length of the test cycle in HW Config).</td>
<td>The CPU enters the DEFECTIVE state if a second error triggered by the first error event occurs in ERROR-SEARCH mode.</td>
</tr>
</tbody>
</table>

If a second checksum error occurs in single/stand-alone mode after twice the test cycle time has expired, the CPU reacts as it did on the first occurrence of the error. If a second error (hardware fault with one-sided call of OB 121, checksum error) occurs in redundant mode when troubleshooting is finished, the CPU reacts as it did on the first occurrence of the error.

Multiple-bit errors

The CPU changes to ERROR-SEARCH mode when a multiple-bit error is detected while the fault-tolerant system is operating in redundant mode. When troubleshooting is finished, the CPU can automatically connect and update itself, and resume redundant operation. At the transition to error-search mode, the address of the errors is reported in the diagnostic buffer.

Single-bit errors

The CPU calls OB 84 after detection and elimination of the error.

Influencing the cyclic self-test

SFC 90 "H_CTRL" allows you to influence the scope and execution of the cyclic self-test. For example, you can remove various test components from the overall test and re-introduce them. In addition, you can explicitly call and process specific test components.

For detailed information on SFC 90 "H_CTRL", refer to the System Software for S7-300/400, System and Standard Functions manual.

Note

In a fail-safe system, you are not allowed to disable and then re-enable the cyclic self-tests. For more details, refer to the S7-400F and S7-400FH Automation Systems manual.
11.5 Evaluation of hardware interrupts in the S7-400H system

When using a hardware interrupt-triggering module in the S7-400H system, it is possible that the process values which can be read from the hardware interrupt OB by direct access do not match the process values valid at the time of the interrupt. Evaluate the temporary variables (start information) in the hardware interrupt OB instead.

When using the process interrupt-triggering module SM 321-7BH00, it is not advisable to have different responses to rising or falling edges at the same input, because this would require direct access to the I/O. If you want to respond differently to the two edge changes in your user program, assign the signal to two inputs from different channel groups and parameterize one input for the rising edge and the other for the falling edge.
System and operating states of the S7–400H

11.5 Evaluation of hardware interrupts in the S7-400H system
Link-up and update

12.1 Effects of link-up and updating

Link-up and updating are indicated by the REDF LEDs on the two CPUs. During link-up, the LEDs flash at a frequency of 0.5 Hz, and when updating at a frequency of 2 Hz.

Link-up and update have various effects on user program execution and on communication functions.

Table 12-1 Properties of link-up and update functions

<table>
<thead>
<tr>
<th>Process</th>
<th>Link-up</th>
<th>Update</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execution of the user program</td>
<td>All priority classes (OBs) are processed.</td>
<td>Processing of the priority classes is delayed section by section. All requests are caught up with after the update. For details, refer to the sections below.</td>
</tr>
<tr>
<td>Deleting, loading, generating, and compressing of blocks</td>
<td>Blocks cannot be deleted, loaded, created or compressed. When such actions are busy, link-up and update operations are inhibited.</td>
<td>Blocks cannot be deleted, loaded, created or compressed.</td>
</tr>
<tr>
<td>Execution of communication functions, PG operation</td>
<td>Communication functions are executed.</td>
<td>Execution of the functions is restricted section by section and delayed. All the delayed functions are caught up with after the update. For details, refer to the sections below.</td>
</tr>
<tr>
<td>CPU self-test</td>
<td>Not performed</td>
<td>Not performed</td>
</tr>
<tr>
<td>Test and commissioning functions, such as &quot;Monitor and modify tag&quot;, &quot;Monitor (On/Off)&quot; and &quot;Force&quot;</td>
<td>Test and commissioning functions are disabled. When such actions are busy, link-up and update operations are inhibited.</td>
<td>Test and commissioning functions are disabled.</td>
</tr>
<tr>
<td>Handling of the connections on the master CPU</td>
<td>All connections are retained; no new connections can be made.</td>
<td>All connections are retained; no new connections can be made. Interrupted connections are not restored until the update is completed</td>
</tr>
<tr>
<td>Handling of the connections on the reserve CPU</td>
<td>All the connections are cancelled; no new connections can be made.</td>
<td>All connections are already down. They were cancelled during link-up.</td>
</tr>
</tbody>
</table>
12.2 Conditions for link-up and update

Which commands you can use on the programming device to initiate a link-up and update operation is determined by the current conditions on the master and reserve CPU. The table below shows the correlation between those conditions and available programming device commands for link-up and update operations.

Table 12-2 Conditions for link-up and update

<table>
<thead>
<tr>
<th>Link-up and update as PG command:</th>
<th>Size and type of load memory in the master and reserve CPUs</th>
<th>FW version in the master and reserve CPUs</th>
<th>Available sync connections</th>
<th>Hardware version on master and reserve CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Restart of the reserve</td>
<td>Are identical</td>
<td>Are identical</td>
<td>2</td>
<td>Are identical</td>
</tr>
<tr>
<td>Switch to CPU with modified configuration</td>
<td>RAM and EPROM mixed</td>
<td>Are identical</td>
<td>2</td>
<td>Are identical</td>
</tr>
<tr>
<td>Switchover to CPU with expanded memory configuration</td>
<td>Size of load memory in the reserve CPU is larger than that of the master</td>
<td>Are identical</td>
<td>2</td>
<td>Are identical</td>
</tr>
<tr>
<td>Switchover to CPU with modified operating system</td>
<td>Are identical</td>
<td>Are different</td>
<td>2</td>
<td>Are identical</td>
</tr>
<tr>
<td>CPUs with changed hardware version</td>
<td>Are identical</td>
<td>Are identical</td>
<td>2</td>
<td>Are different</td>
</tr>
<tr>
<td>Only one synchronization link-up is available over one intact redundant link</td>
<td>Are identical</td>
<td>Are identical</td>
<td>1</td>
<td>Are identical</td>
</tr>
</tbody>
</table>
12.3 Link-up and update sequence

There are two types of link-up and update operation:

- Within a "normal" link-up and update operation, the fault-tolerant system should change over from standalone mode to redundant mode. The two CPUs then process the same program synchronized with each other.

- When the CPUs link up and update with master/standby changeover, the second CPU with modified components can assume control over the process. Either the hardware configuration, or the memory configuration, or the operating system may have been modified.

In order to return to redundant system mode, a "normal" link-up and update operation must be performed subsequently.

How to start the link-up and update operation?

Initial situation: Single mode, i.e. only one of the CPUs of a fault-tolerant system connected via fiber-optic cables is in RUN.

To establish system redundancy, initiate the link-up and update operation as follows:

- Toggle the mode selector switch of the standby CPU from STOP to RUN.
- POWER ON the standby (mode selector in RUN position) if prior to POWER OFF the CPU was not in STOP mode.
- Operator input on the PG/ES.

A link-up and update operation with master/standby changeover is always started on the PG/ES.

Note

If a link-up and update operation is interrupted on the standby CPU (for example due to POWER OFF, STOP), this may cause data inconsistency and lead to a memory reset request on this CPU.

The link-up and update functions are possible again after a memory reset on the standby.
Flow chart of the link-up and update operation

The figure below outlines the general sequence of the link-up and update. In the initial situation, the master is operating in standalone mode. In the figure, CPU 0 is assumed to be the master.

Figure 12-1 Sequence of link-up and update

*) If the "Switchover to CPU with altered configuration" option is set, the content of the load memory is not copied; what is copied from the user program blocks of the work memory (OBs, FCs, FBs, DBs, SDBs) of the master CPU is listed in section Switch to CPU with modified configuration or expanded memory configuration (Page 146)
Figure 12-2  Update sequence

*) For details on the relevant SFCs, SFBs and communication functions, refer to the next chapters.
**Minimum duration of input signals during update**

Program execution is stopped for a certain time during the update (the sections below describe this in greater detail). To ensure that the CPU can reliably detect changes to input signals during the update, the following condition must be satisfied:

Min. signal duration > 2 x the time required for I/O update (DP and PNIO only)  
+ call interval of the priority class  
+ program execution time of the priority class  
+ update time  
+ execution time for programs of higher-priority classes

Example:

Minimum signal duration of an input signal that is evaluated in a priority class > 15 (e.g. OB 40).

![Figure 12-3 Example of minimum signal duration of an input signal during the update](image-url)

Figure 12-3  Example of minimum signal duration of an input signal during the update
12.3.1 Link-up sequence

For the link-up sequence, you need to decide whether to carry out a master/reserve changeover, or whether redundant system mode is to be achieved after that.

Link-up with the objective of setting up system redundancy

To exclude differences in the two subsystems, the master and the reserve CPU run the following comparisons.

The following are compared:
1. Consistency of the memory configuration
2. Consistency of the operating system version
3. Consistency of the load memory (FLASH card) content
4. Consistency of load memory (integrated RAM and RAM card) content

If 1., 2., or 3. are inconsistent, the reserve CPU changes to STOP mode and outputs an error message.

If 4. is inconsistent, the master CPU copies the user program from its load memory in RAM to the reserve CPU.

The user program stored in load memory on the FLASH card is not transferred. It must be identical before initiating link-up.

Link-up with master/reserve changeover

In STEP 7 you can select one of the following options:

- "Switch to CPU with modified configuration"
- "Switchover to CPU with expanded memory configuration"
- "Switchover to CPU with modified operating system"
- "Switchover to CPU with modified hardware version"
- "Switchover to CPU via only one intact redundant link"

Switch to CPU with modified configuration

You may have modified the following elements on the reserve CPU:

- The hardware configuration
- The type of load memory (for example, you have replaced a RAM card with a FLASH card). The new load memory may be larger or smaller than the old one.

The master does not transfer any blocks to the reserve during the link-up. For detailed information, refer to section Switch to CPU with modified configuration or expanded memory configuration (Page 146).
12.3 Link-up and update sequence

For information on the required steps based on the scenarios described above (alteration of the hardware configuration, or of the type of load memory), refer to section Failure and replacement of components during operation (Page 253).

Note
Even though you have not modified the hardware configuration or the type of load memory on the reserve CPU, there is nevertheless a master/reserve changeover and the previous master CPU changes to STOP.

Switchover to CPU with expanded memory configuration
You may have expanded the load memory on the reserve CPU. The memory media for storing load memory must be identical, i.e. either RAM cards or FLASH cards. The contents of FLASH cards must be identical.

During the link-up, the user program blocks (OBs, FCs, FBs, DBs, SDBs) of the master are transferred from the load memory and work memory to the reserve. Exception: If the load memory modules are FLASH cards, the system only transfers the blocks from work memory.

For information on changing the type of memory or on load memory expansions, refer to section Changing the CPU memory configuration (Page 313).

Note
Assuming you have implemented a different type of load memory or operating system on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer.
Assuming you have not expanded load memory on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer.
The system does not perform a master/reserve changeover, and the previous master CPU remains in RUN.
12.3.2 Update sequence

What happens during updating?

The execution of communication functions and OBs is restricted section by section during updating. Likewise, all the dynamic data (content of the data blocks, timers, counters, and bit memories) are transferred to the standby CPU.

Update procedure:

1. Until the update is completed, all asynchronous SFCs and SFBs which access data records of I/O modules (SFCs 13, 51, 52, 53, 55 to 59, SFB 52 and 53) are acknowledged as "negative" with the return values W#16#80C3 (SFCs 13, 55 to 59, SFB 52 and 53) or W#16#8085 (SFC 51). When these values are returned, the jobs should be repeated by the user program.

2. Message functions are delayed until the update is completed (see list below).

3. The execution of OB 1 and of all OBs up to priority class 15 is delayed.

   In the case of cyclic interrupts, the generation of new OB requests is disabled, so no new cyclic interrupts are stored and as a result no new request errors occur.

   The system waits until the update is completed, and then generates and processes a maximum of one request per cyclic interrupt OB. The time stamp of delayed cyclic interrupts cannot be evaluated.

4. Transfer of all data block contents modified since link-up.

5. The following communication jobs are acknowledged negatively:
   - Reading/writing of data records using HMI functions
   - Reading diagnostic information using STEP 7
   - Disabling and enabling messages
   - Logon and logoff for messages
   - Acknowledgement of messages

6. Initial calls of communication functions are acknowledged negatively. These calls manipulate the work memory, see also System Software for S7-300/400, System and Standard Functions. All remaining communication functions are executed with delay, after the update is completed.

7. The system disables the generation of new OB requests for all OBs of priority class > 15, so new interrupts are not saved and as a result do not generate any request errors.

   Queued interrupts are not requested again and processed until the update is completed. The time stamp of delayed interrupts cannot be evaluated.

   The user program is no longer processed and there are no more I/O updates.
8. Generating the start event for the cyclic interrupt OB with special handling.

**Note**

The cyclic interrupt OB with special handling is particularly important in situations where you need to address certain modules or program parts within a specific time. This is a typical scenario in fail-safe systems. For details, refer to the *S7-400F and S7-400FH Automation Systems* and *S7-300 Automation Systems, Fail-safe Signal Modules* manuals.

To prevent an extension of the special cyclic interrupt, the cyclic alarm OB with special handling must be assigned top priority.


During this data synchronization, the system interrupts the clock pulse for cyclic interrupts, time-delay interrupts and S7 timers. This results in the loss of any synchronism between cyclic and time-of-day interrupts.

10. Cancel all restrictions. Delayed interrupts and communication functions are executed. All OBs are executed again.

A constant bus cycle time compared with previous calls can no longer be guaranteed for delayed cyclic interrupt OBs.

**Note**

Process interrupts and diagnostic interrupts are stored by the I/O devices. Such interrupt requests issued by distributed I/O modules are executed when the block is re-enabled. Any such requests by central I/O modules can only be executed provided the same interrupt request did not occur repeatedly while the status was disabled.

If the PG/ES requested a master/standby changeover, the previous standby CPU assumes master mode and the previous master CPU goes into STOP when the update is completed. Both CPUs will otherwise go into RUN (redundant system mode) and execute the user program in synchronism.

When there is a master/standby changeover, in the first cycle after the update OB 1 is assigned a separate identifier (see *System Software for S7-300/400, System and Standard Functions Reference Manual*). For information on other aspects resulting from modifying the configuration, refer to section **Switch to CPU with modified configuration or expanded memory configuration** (Page 146).
Delayed message functions

The listed SFCs, SFBs and operating system services trigger the output of messages to all logged-on partners. These functions are delayed after the start of the update:

- SFC 17 "ALARM_SQ", SFC 18 "ALARM_S", SFC 107 "ALARM_DQ", SFC 108 "ALARM_D"
- SFC 52 "WR_USMSG"
- SFB 31 "NOTIFY_8P", SFB 33 "ALARM", SFB 34 "ALARM_8", SFB 35 "ALARM_8P", SFB 36 "NOTIFY", SFB 37 "AR_SEND"
- Process control alarms
- System diagnostics messages

From this time on, any requests to enable and disable messages by SFC 9 "EN_MSG" and SFC 10 "DIS_MSG" are rejected with a negative return value.

Communication functions and resulting jobs

After it has received one of the jobs specified below, the CPU must in turn generate communication jobs and output them to other modules. These include, for example, jobs for reading or writing parameterization data records from/to distributed I/O modules. These jobs are rejected until the update is completed.

- Reading/writing of data records using HMI functions
- Reading data records using SSL information
- Disabling and enabling messages
- Logon and logoff for messages
- Acknowledgement of messages

Note

The last three of the functions listed are registered by a WinCC system, and automatically repeated when the update is completed.
12.3.3 Switch to CPU with modified configuration or expanded memory configuration

Switch to CPU with modified configuration

You may have modified the following elements on the reserve CPU:

- The hardware configuration
- The type of load memory. You may have replaced a RAM card with a FLASH card, for example. The new load memory may be larger or smaller than the old one.

For information on steps required in the scenarios mentioned above, refer to section Failure and replacement of components during operation (Page 253).

Note

Even though you have not modified the hardware configuration or the type of load memory on the reserve CPU, there is nevertheless a master/reserve changeover and the previous master CPU changes to STOP.

Note

If you have downloaded connections using NETPRO, you can no longer change the memory type of the load memory from RAM to FLASH.

When you initiate a link-up and update operation with the "Switch to CPU with modified configuration" option in STEP 7, the system reacts as follows with respect to handling of the memory contents.

Load memory

The contents of the load memory are not copied from the master to the reserve CPU.

Work memory

The following components are transferred from the work memory of the master CPU to the reserve CPU:

- Contents of all data blocks assigned the same interface time stamp in both load memories and whose attributes "read only" and "unlinked" are not set.
- Data blocks generated in the master CPU by SFCs.
  
  The DBs generated in the reserve CPU by means of SFC are deleted.
  
  If a data block with the same number is also found in the load memory of the reserve CPU, link-up is cancelled with an entry in the diagnostic buffer.
- Process images, timers, counters, and bit memories
  
  If there is insufficient memory, link-up is cancelled with an entry in the diagnostic buffer.
The status of SFB instances of S7 communication contained in modified data blocks is restored to the status prior to their initial call.

**Note**
When changing over to a CPU with modified configuration, the size of load memories in the master and reserve may be different.

**Switch to CPU with expanded memory configuration**

You may have expanded the load memory on the reserve CPU. The memory media for storing load memory must be identical, i.e. either RAM cards or FLASH cards. The contents of FLASH cards must be identical.

**Note**
Assuming you have implemented a different type of load memory or operating system on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer.
Assuming you have not expanded load memory on the reserve CPU, this CPU does not go into RUN, but rather returns to STOP and writes a corresponding message to the diagnostic buffer.
The system does not perform a master/reserve changeover, and the previous master CPU remains in RUN.

For information on changing the type of memory or on load memory expansions, refer to section [Failure and replacement of components during operation](Page 253).

When you initiate a link-up and update with the “Switch to CPU with expanded memory configuration” option in STEP 7, the system reacts as follows with respect to the handling of memory contents.

**RAM and load memory**

During the link-up, the user program blocks (OBs, FCs, FBs, DBs, SDBs) of the master are transferred from the load memory and work memory to the reserve. Exception: If the load memory modules are FLASH cards, the system only transfers the blocks from work memory.
12.3.4 Disabling of link-up and update

Link-up and update entails a cycle time extension. This includes a period during which the I/O is not updated; see section Time monitoring (Page 149). Make allowances for this feature in particular when using distributed I/Os and on master/reserve changeover after updating (that is, when modifying the configuration during operation).

--- CAUTION ---

Always perform link-up and update operations when the process is not in a critical state.

---

You can set specific start times for link-up and update operations at SFC 90 "H_CTRL". For detailed information on this SFC, refer to the System Software for S7-300/400, System and Standard Functions manual.

--- Note ---

If the process tolerates cycle time extensions at any time, you do not need to call SFC 90 "H_CTRL".

The CPU does not perform a self-test during link-up and updating. If you use a fail-safe user program, you should avoid any excessive delay for the update operation. For more details, refer to the S7-400F and S7-400FH Automation Systems manual.

--- Example of a time-critical process ---

A slide block with a 50 mm cam moves on an axis at a constant velocity \( v = 10 \text{ km/h} = 2.78 \text{ m/s} = 2.78 \text{ mm/ms} \). A switch is located on the axis. So the switch is actuated by the cam for the duration of \( \Delta t = 18 \text{ ms} \).

For the CPU to detect the actuation of the switch, the inhibit time for priority classes \( > 15 \) (see below for definition) must be significantly below 18 ms.

With respect to maximum inhibit times for operations of priority class \( > 15 \), STEP 7 only supports settings of 0 ms or between 100 and 60000 ms, so you need to work around this by taking one of the following measures:

- Shift the start time of link-up and updating to a time at which the process state is non-critical. Use SFC 90 "H_CTRL" to set this time (see above).
- Use a considerably longer cam and/or substantially reduce the approach velocity of the slide block to the switch.
12.4 Time monitoring

Program execution is interrupted for a certain time during updating. This section is relevant to you if this period is critical in your process. If this is the case, configure one of the monitoring times described below.

During updating, the fault-tolerant system monitors the cycle time extension, communication delay and inhibit time for priority classes > 15 in order to ensure that their configured maximum values are not exceeded, and that the configured minimum I/O retention time is maintained.

Note

If you have not defined any default values for the monitoring times, make allowance for the update in the scan cycle monitoring time. If in this case the update is cancelled, the fault-tolerant system switches to standalone mode: The previous master CPU remains in RUN, and the standby CPU goes into STOP.

You can either configure all the monitoring times or none at all.

You made allowances for the technological requirements in your configuration of monitoring times.

The monitoring times are described in detail below.

- **Maximum cycle time extension**
  - Cycle time extension: The time during the update in which neither OB 1 nor any other OBs up to priority class 15 are executed. "Normal" cycle time monitoring is disabled within this time span.
  - Max. cycle time extension: The maximum permissible cycle time extension configured by the user.

- **Maximum communication delay**
  - Communication delay: The time span during the update during which no communication functions are processed. Note: The master CPU, however, maintains all existing communication links.
  - Maximum communication delay: The maximum permissible communication delay configured by the user.

- **Maximum inhibit time for priority classes > 15**
  - Inhibit time for priority classes > 15: The time span during an update during which no OBs (and thus no user program) are executed nor any I/O updates are implemented.
  - Maximum inhibit time for priority classes > 15: The maximum permissible inhibit time for priority classes > 15 configured by the user.

- **Minimum I/O retention time:**
  This represents the interval between copying of the outputs from the master CPU to the standby CPU, and the time of the transition to the redundant system mode or master/standby changeover (time at which the previous master CPU goes into STOP and the new master CPU goes into RUN). Both CPUs control the outputs within this period, in order to prevent the I/O from going down when the system performs an update with master/standby changeover.
The minimum I/O retention time is of particular importance when updating with master/standby changeover. If you set the minimum I/O retention time to 0, the outputs could possibly shut down when you modify the system during operation.

The monitoring start times are indicated in the highlighted boxes in Figure 12-2. These times expire when the system enters the redundant system mode or when there is a master/standby changeover, i.e. on the transition of the new master to RUN when the update is completed.

The figure below provides an overview of the relevant update times.

**Update:**

1. **t1**: End of current OBs up to priority class 15
2. **t2**: Stop all communication functions
3. **t3**: End of watchdog interrupt OB with special handling
4. **t4**: End of copying of outputs to the standby CPU
5. **t5**: Redundant system status, or master/standby changeover

**Figure 12-4** Meanings of the times relevant for updates
Response to time-outs

If one of the times monitored exceeds the configured maximum value, the following procedure is started:

1. Cancel update
2. Fault-tolerant system remains in standalone mode, with the previous master CPU in RUN
3. Cause of cancelation is entered in diagnostic buffer
4. Call OB 72 (with corresponding start information)

The standby CPU then reevaluates its system data blocks. Then, but after at least one minute, the CPU tries again to perform the link-up and update. If still unsuccessful after a total of 10 retries, the CPU abandons the attempt. You yourself will then need to start the link-up and update again.

A monitoring timeout can be caused by:

- High interrupt load (e.g. from I/O modules)
- High communication load causing prolonged execution times for active functions
- In the final update phase, the system needs to copy large amounts of data to the standby CPU.

12.4.1 Time response

Time response during link-up

The influence of link-up operations on your plant's control system should be kept to an absolute minimum. The current load on your automation system is therefore a decisive factor in the increase of link-up times. The time required for link-up is in particular determined by

- the communication load
- the cycle time

The following applies to no-load operation of the automation system:

\[
\text{Link-up runtime} = \text{size of load memory and work memory in MB} \times 1 \text{ s} + \text{base load}
\]

The base load is a few seconds.

Whenever your automation system is subject to high load, the memory-specific share may increase up to 1 minute per MB.
12.4 Time monitoring

Time response during updating

The update transfer time is determined by the number and overall length of modified data blocks, rather than by the modified volume of data within a block. It is also determined by the current process status and communication load.

As a simple approximation, we can interpret the maximum inhibit time to be configured for priority classes > 15 as a function of the data volume in the work memory. The volume of code in the work memory is irrelevant.

12.4.2 Determining the monitoring times

Calculation using STEP 7 or formulas

STEP 7 automatically calculates the monitoring times listed below for each new configuration. You can also calculate these times using the formulas and procedures described below. They are equivalent to the formulas provided in STEP 7.

- Maximum cycle time extension
- Maximum communication delay
- Maximum inhibit time for priority classes
- Minimum I/O retention time

You can also start automatic calculation of monitoring times with Properties CPU > H Parameters in HW Config.

Monitoring time accuracy

Note

The monitoring times determined by STEP 7 or by using formulas merely represent recommended values.

These times are based on a fault-tolerant system with two communication peers and an average communication load.

Your system profile may differ considerably from those scenarios, therefore the following rules must be observed.

- The cycle time extension factor may increase sharply at a high communication load.
- Any modification of the system in operation may lead to a significant increase in cycle times.
- Any increase in the number of programs executed in priority classes > 15 (in particular processing of communication blocks) automatically increases the communication delay and cycle time extension.
- You can even undercut the calculated monitoring times in small plants with high-performance requirements.
Configuration of the monitoring times

When configuring monitoring times, always make allowances for the following dependencies; conformity is checked by STEP 7:

- Maximum cycle time extension
- > maximum communication delay
- > (maximum inhibit time for priority classes > 15)
- > minimum I/O retention time

If you have configured different monitoring times in the CPUs and perform a link-up and update operation with master/standby changeover, the system always applies the higher of the two values.

Calculating the minimum I/O retention time ($T_{PH}$)

The following applies to the calculation of the minimum I/O retention time:

- With central I/O: $T_{PH} = 30$ ms
- For distributed I/O (PROFIBUS DP): $T_{PH} = 3 \times T_{TR\text{max}}$
  Where $T_{TR\text{max}}$ = maximum target rotation time of all DP master systems of the fault-tolerant station
- For distributed I/O (PROFINET IO): $T_{PH} = T_{wd\text{,max}}$
  with $T_{wd\text{,max}}$ = maximum cyclic interrupt time (product of WD factor and update time) of a switched device in all IO subsystems of the fault-tolerant station

When using central and distributed I/Os, the resultant minimum I/O retention time is:

$T_{PH} = \text{MAX (30 ms, } 3 \times T_{TR\text{max}}, T_{wd\text{,max}})$

The following figure shows the correlation between the minimum I/O retention time and the maximum inhibit time for priority classes > 15.

![Figure 12-5 Correlation between the minimum I/O retention time and the maximum inhibit time for priority classes > 15](image)

Note the following condition:

$50 \text{ ms } + \text{minimum I/O retention time } \leq (\text{maximum inhibit time for priority classes } > 15)$

It follows that a high minimum I/O retention time can determine the maximum inhibit time for priority classes > 15.
Calculating the maximum inhibit time for priority classes > 15 (\(T_{P15}\))

The maximum inhibit time for priority classes > 15 is determined by 4 main factors:

- As shown in Figure 12–2, all the contents of data blocks modified since last copied to the standby CPU are once again transferred to the standby CPU on completion of the update. The number and structure of the DBs you write to in the high-priority classes is a decisive factor in the duration of this operation, and thus in the maximum inhibit time for priority classes > 15. Relevant information is available in the remedies described below.

- In the final update phase, all OBs are either delayed or inhibited. To avoid any unnecessary extension of the maximum inhibit time for priority classes > 15 due to unfavorable programming, you should always process the time-critical I/O components in a selected cyclic interrupt. This is particularly relevant in fail-safe user programs. You can define this cyclic interrupt in your configuration. It is then executed again right after the start of the maximum inhibit time for priority classes > 15, provided you have assigned it a priority class > 15.

- In link-up and update operations with master/standby changeover (see section Link-up sequence (Page 141)), you also need to changeover the active communication channel on the switched DP slaves and switched IO devices on completion of the update. This operation prolongs the time within which valid values can neither be read nor output. How long this process takes is determined by your hardware configuration.

- The technological conditions in your process also decide how long an I/O update can be delayed. This is particularly important in time-monitored processes in fail-safe systems.

Note

For details, refer to the S7-400F and S7-400FH Automation Systems and S7-300 Automation Systems, Fail-safe Signal Modules manuals. This applies in particular to the internal execution times of fail-safe modules.

1. Based on the bus parameters in STEP 7, for each DP master system you must define:
   - \(T_{TR}\) for the DP master system
   - DP changeover time (referred to below as \(T_{DP,UM}\))

2. For each IO subsystem from the STEP 7 configuration,
   - define the maximum update time of the IO subsystem (as of herewith named \(T_{max,Akt}\))
   - PN changeover time (as of herewith named \(T_{PN,UM}\))

3. Based on the technical data of the switched DP slaves, define for each DP master system:
   - The maximum changeover time of the active communication channel (referred to below as \(T_{SLAVE,UM}\)).

4. Based on the technical specifications of the switched PN devices, determine the following for each IO subsystem:
   - the maximum changeover time of the active communication channel (as of herewith named \(T_{Device,UM}\)) for each DP master system.
5. Based on the technological settings of your system, define:
   – The maximum permissible time during which there is no update of your I/O modules (referred to below as TPTO).

6. Based on your user program, determine:
   – The cycle time of the highest-priority or selected (see above) cyclic interrupt (TWA)
   – The execution time of your program in this cyclic interrupt (TPROG)

7. For each DP master system this results in:
   \[ T_{P15}^{(DP \, master \, system)} = T_{PTO} - (2 \times T_{TR} + T_{WA} + T_{PROG} + T_{DP\_UM} + T_{SLAVE\_UM}) \] [1]

8. Derived for each IO subsystem:
   \[ T_{P15}^{(IO \, subsystem)} = T_{PTO} - (2 \times T_{max\,Akt} + T_{WA} + T_{PROG} + T_{PN\_UM} + T_{Device\_UM}) \] [1]

**Note**
- If \( T_{P15}^{(DP \, master \, system)} \) < 0 or \( T_{P15}^{(IO \, subsystem)} \) < 0, stop the calculation here. Possible remedies are shown below the following example calculation. Make appropriate changes and then restart the calculation at 1.

9. Select the minimum of all \( T_{P15} \) (DP master system, IO subsystem) values.
   This time is then known as TP15_HW.

10. Define the share of the maximum inhibit time for I/O classes > 15 determined by the minimum I/O retention time (TP15_OD): 
    \[ T_{P15\_OD} = 50 \, ms + \text{min. I/O retention time} \] [2]

**Note**
- If \( T_{P15\_OD} > T_{P15\_HW} \), stop the calculation here. Possible remedies are shown below the following example calculation. Make appropriate changes and then restart the calculation at 1.

11. Using the information in Chapter Performance values for link-up and update (Page 159), calculate the share of the maximum inhibit time for priority classes > 15 that is required by the user program (TP15_AWP).

**Note**
- If \( T_{P15\_AWP} > T_{P15\_HW} \), stop the calculation here. Possible remedies are shown below the following example calculation. Make appropriate changes and then restart the calculation at 1.

12. The recommended value for the maximum inhibit time for priority classes > 15 is now obtained from:
    \[ T_{P15} = \text{MAX} (T_{P15\_AWP}, T_{P15\_OD}) \] [3]
Example of the calculation of $T_{P15}$

In the next steps, we take an existing system configuration and define the maximum permitted time span of an update, during which the operating system does not execute any programs or I/O updates.

Assuming two DP master systems and one IO subsystem are available: DP master system_1 is connected to the CPU via the MPI/DP interface of the CPU, and DP master system_2 via an external DP master interface. The IO subsystem is connected via the integrated Ethernet interface.

1. Based on the bus parameters in STEP 7:
   - $T_{TR,1} = 25$ ms
   - $T_{TR,2} = 30$ ms
   - $T_{DP,UM,1} = 100$ ms
   - $T_{DP,UM,2} = 80$ ms

2. Based on the configuration in STEP 7:
   - $T_{max,Akt} = 8$ ms
   - $T_{PN,UM} = 110$ ms

3. Based on the technical data of the DP slaves used:
   - $T_{SLAVE,UM,1} = 30$ ms
   - $T_{SLAVE,UM,2} = 50$ ms

4. Based on the technical specifications of the PN devices used:
   - $T_{Device,UM} = 20$ ms

5. Based on the technological settings of your system:
   - $T_{PTO,1} = 1250$ ms
   - $T_{PTO,2} = 1200$ ms
   - $T_{PTO,PN} = 1000$ ms

6. Based on the user program:
   - $T_{WA} = 300$ ms
   - $T_{PROG} = 50$ ms

7. Based on the formula [1]:
   - $T_{P15} (\text{DP master system}_1) = 1250$ ms - (2 x 25 ms + 300 ms + 50 ms + 100 ms + 30 ms) = 720 ms
   - $T_{P15} (\text{DP master system}_2) = 1200$ ms - (2 x 30 ms + 300 ms + 50 ms + 80 ms + 50 ms) = 660 ms
8. Based on the formula [1]:
\[ T_{P15} (IO \text{ subsystem}) = 1200 \text{ ms} - (2 \times 8 \text{ ms} + 300 \text{ ms} + 50 \text{ ms} + 110 \text{ ms} + 20 \text{ ms}) = 704 \text{ ms} \]

Check: Since \( T_{P15} > 0 \), continue with

1. \( T_{P15,\text{HW}} = \text{MIN} (720 \text{ ms}, 660 \text{ ms}, 704 \text{ ms}) = 660 \text{ ms} \)

2. Based on the formula [2]:
\[ T_{P15,\text{OD}} = 50 \text{ ms} + T_{PH} = 50 \text{ ms} + 90 \text{ ms} = 140 \text{ ms} \]

Check: Since \( T_{P15,\text{OD}} = 140 \text{ ms} < T_{P15,\text{HW}} = 660 \text{ ms} \), continue with

1. Based on section "Performance values for link-up and update" (Page 159) with 170 Kbytes of user program data:
\[ T_{P15,\text{AWP}} = 194 \text{ ms} \]

Check: Since \( T_{P15,\text{AWP}} = 194 \text{ ms} < T_{P15,\text{HW}} = 660 \text{ ms} \), continue with

1. Based on formula [3], we obtain the recommended max. inhibit time for priority classes > 15:
\[ T_{P15} = \text{MAX} (194 \text{ ms}, 140 \text{ ms}) \]
\[ T_{P15} = 194 \text{ ms} \]

This means that by setting a maximum inhibit time of 194 ms for priority classes > 15 in STEP 7, you ensure that any signal changes during the update are detected with a signal duration of 1250 ms or 1200 ms.

**Remedies if it is not possible to calculate \( T_{P15} \)**

If no recommendation results from calculating the maximum inhibit time for priority classes > 15, you can remedy this by taking various measures:

- Reduce the cyclic interrupt cycle of the configured cyclic interrupt.
- If \( T_{TR} \) times are particularly high, distribute the slaves across several DP master systems.
- If possible, reduce the maximum update time of switched devices on the IO subsystem.
- Increase the baud rate on the affected DP master systems.
- Configure the DP/PA links and Y links in separate DP master systems.
- If there is a great difference in changeover times on the DP slaves, and thus (generally) great differences in \( T_{PT0} \), distribute the slaves involved across several DP master systems.
If you do not expect any significant load caused by interrupts or parameter assignments in the various DP master systems, you can also reduce the calculated $T_{TR}$ times by around 20% to 30%. However, this increases the risk of a station failure in the distributed I/O.

- The time value $T_{P15, AWP}$ represents a guideline and depends on your program structure. You can reduce it by taking the following measures, for example:
  - Save data that changes often in different DBs than data that does not change as often.
  - Specify a smaller DB sizes in the work memory.

If you reduce the time $T_{P15, AWP}$ without taking the measures described, you run the risk that the update operation will be canceled due to a monitoring timeout.

**Calculation of the maximum communication delay**

Use the following formula:

$$\text{Maximum communication delay} = 4 \times (\text{maximum inhibit time for priority classes > 15})$$

Decisive factors for determining this time are the process status and the communication load in your system. This can be understood as the absolute load or as the load relative to the size of your user program. You may have to adjust this time.

**Calculation of the maximum cycle time extension**

Use the following formula:

$$\text{Maximum cycle time extension} = 10 \times (\text{maximum inhibit time for priority classes > 15})$$

Decisive factors for determining this time are the process status and the communication load in your system. This can be understood as the absolute load or as the load relative to the size of your user program. You may have to adjust this time.
12.4.3 Performance values for link-up and update

User program share $T_{P15,AWP}$ of the maximum inhibit time for priority classes $> 15$

The user program share $T_{P15,AWP}$ of the maximum inhibit time for priority classes $> 15$ can be calculated using the following formula:

$$T_{P15,AWP} \text{ in ms} = 0.7 \times \text{size of DBs in work memory in KB} + 75$$

The table below shows the derived times for some typical values in work memory data.

Table 12-3  Typical values for the user program part

<table>
<thead>
<tr>
<th>Work memory data</th>
<th>$T_{P15,AWP}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 KB</td>
<td>220 ms</td>
</tr>
<tr>
<td>1 MB</td>
<td>400 ms</td>
</tr>
<tr>
<td>2 MB</td>
<td>0.8 s</td>
</tr>
<tr>
<td>5 MB</td>
<td>1.8 s</td>
</tr>
<tr>
<td>10 MB</td>
<td>3.6 s</td>
</tr>
</tbody>
</table>

The following assumptions were made for this formula:

- 80% of the data blocks are modified prior to delaying the interrupts of priority classes $> 15$.

  In particular for fail-safe systems, this calculated value must be more precise to avoid any timeout of driver blocks (see section Determining the monitoring times (Page 152)).

- For active or queued communication functions, allowance is made for an update time of approximately 100 ms per MB in the work memory occupied by data blocks. Depending on the communication load of your automation system, you will need to add or deduct a value when you set $T_{P15,AWP}$. 
12.4.4 Influences on time response

The period during which no I/O updates take place is primarily determined by the following influencing factors:

- The number and size of data blocks modified during the update
- The number of instances of SFBs in S7 communication and of SFBs for generating block-specific messages
- System modifications during operation
- Settings by means of dynamic quantity structures
- Expansion of distributed I/Os with PROFIBUS DP (a lower baud rate and higher number of slaves increases the time it takes for I/O updates).
- Expansion of distributed I/Os with PROFINET IO (a higher update time and higher number of devices increases the time it takes for I/O updates).

In the worst case, this period is extended by the following amounts:

- Maximum cyclic interrupt used
- Duration of all cyclic interrupt OBs
- Duration of high-priority interrupt OBs executed until the start of interrupt delays

Explicit delay of the update

Delay the update using SFC 90 "H_CTRL", and re-enable it only when the system state shows less communication or interrupt load.

<table>
<thead>
<tr>
<th>CAUTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>The update delay increases the time of standalone mode operation of the fault-tolerant system.</td>
</tr>
</tbody>
</table>

CAUTION
12.5 Special features in link-up and update operations

Requirement for input signals during the update

Any process signals read previously are retained and not included in the update. The CPU only recognizes changes of process signals during the update if the changed signal state remains after the update is completed.

The CPU does not detect pulses (signal transitions "0 → 1 → 0" or "1 → 0 → 1") which are generated during the update.

You should therefore ensure that the interval between two signal transitions (pulse period) is always greater than the required update period.

Communication links and functions

Connections on the master CPU are not be shut down. However, associated communication jobs are not executed during updates. They are queued for execution as soon as one of the following cases occurs:

- The update is completed, and the system is in the redundant state.
- The update and master/reserve changeover are completed, the system is in single mode.
- The update was canceled (e.g. due to timeout), and the system has returned to single mode.

An initial call of communication blocks is not possible during the update.

Memory reset request on cancelation of link-up

If the link-up operation is canceled while the content of load memory is being copied from the master to the reserve CPU, the reserve CPU requests a memory reset. This indicated in the diagnostic buffer by event ID W#16#6523.
12.5 Special features in link-up and update operations
This section provides an overview of the different I/O installations in the S7-400H automation system and their availability. It also provides information on configuration and programming of the selected I/O installation.

13.1 Introduction

I/O installation types

In addition to the power supply module and CPUs, which are always redundant, the operating system supports the following I/O installations:

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-channel one-sided</td>
<td>normal</td>
</tr>
<tr>
<td>Single-channel switched</td>
<td>enhanced</td>
</tr>
<tr>
<td>System redundant</td>
<td>enhanced</td>
</tr>
<tr>
<td>Dual-channel redundant</td>
<td>high</td>
</tr>
</tbody>
</table>

A dual-channel redundant configuration at user level is also possible. You nevertheless need to implement the high availability in the user program (see chapter Other options for connecting redundant I/Os (Page 198)).

Addressing

No matter whether you are using a single-channel one-sided or switched I/O, you always access the I/O via the same address.

Limits of I/O configuration

If there are insufficient slots in the central racks, you can add up to 20 expansion units to the S7-400H configuration.

Module racks with even numbers are always assigned to central rack 0, and racks with odd numbers are always assigned to central rack 1.

For applications with distributed I/O, each of the subsystems supports the connection of up to 12 DP master systems (2 DP master systems on the integrated interfaces of the CPU and 10 via external DP master systems).

The integrated MPI/DP interface supports the operation of up to 32 slaves. You can connect up to 125 distributed I/O devices to the integrated DP master interface and to the external DP master systems.
13.1 Introduction

You can connect up to 256 IO devices to both integrated PROFINET interfaces.

**Note**

**PROFIBUS DP and PROFINET IO in combination**

You can operate PROFINET IO devices as well as PROFIBUS DP stations on a fault-tolerant CPU.

---

**Distributed I/O over PNIO**

You can also operate distributed I/O on the integrated PROFINET interface. Refer to chapter [System redundancy](Page 99).

**Note**

**Fail-safe signal modules**

If you want to operate fail-safe modules redundantly at the PNIO interface, you require the optional package S7 F Systems as of V6.1 SP1.
13.2 Using single-channel, one-sided I/Os

What is single-channel one-sided I/O?

In the single-channel one-sided configuration, the input/output modules exist only once (single-channel). The I/O modules are located in only one subsystem, and are only addressed by this subsystem.

A single-channel one-sided I/O configuration is possible in the following devices:

- Central and expansion devices
- Distributed I/O devices at the PROFIBUS DP interface
- Distributed I/O devices at the PROFINET interface

A configuration with single-channel one-sided I/O is useful for single I/O channels up to system components which only require standard availability.

Single-channel one-sided I/O configuration

Single-channel one-sided I/O and user program

In redundant system mode, the data read from one-sided components (such as digital inputs) is transferred automatically to the second subsystem.

When the transfer is completed, the data read from the single-channel one-sided I/O is available on both subsystems and can be evaluated in their identical user programs. For data processing in the redundant system mode, it is therefore irrelevant whether the I/O is connected to the master or to the standby CPU.

In standalone mode, access to one-sided I/O assigned to the partner subsystem is not possible. This must be considered as follows when programming: Assign functions to the single-channel one-sided I/O that can only be executed conditionally. This ensures that specific I/O access functions are only called in redundant system mode and when the relevant subsystem is in standalone mode.
13.2 Using single-channel, one-sided I/Os

Note
The user program also has to update the process image for single-channel, one-sided output modules when the system is in standalone mode (direct access, for example). If you use process image partitions, the user program must update them (SFC 27 “UPDAT_PO”) in OB 72 (recovery of redundancy). The system would otherwise first output old values on the single-channel one-sided output modules of the standby CPU when the system changes to redundant mode.

Failure of the single-channel one-sided I/O
The fault-tolerant system with single-channel one-sided I/O responds to errors just like a standard S7-400 system.

- The I/O is no longer available after it fails.
- If the subsystem to which the I/O is connected fails, the entire process I/O of this subsystem is no longer available.
13.3 Using single-channel switched I/O

What is single-channel switched I/O?

In the single-channel switched configuration, the input/output modules are present singly (single-channel).

In redundant mode, these can be addressed by both subsystems.

In standalone mode, the master subsystem can always address all switched I/Os (in contrast to one-sided I/O).

Single-channel switched I/O configuration at the PROFIBUS DP interface

The system supports single-channel switched I/O configurations containing an ET 200M distributed I/O module with active backplane bus and a redundant PROFIBUS DP slave interface module.

![Diagram of S7-400H automation system with ET 200M distributed I/O configuration at the PROFIBUS DP interface](image)

Figure 13-1 Single-channel switched distributed I/O configuration at the PROFIBUS DP interface

You can use the following interfaces for the I/O configuration at the PROFIBUS DP interface:

<table>
<thead>
<tr>
<th>Interface</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IM 153–2</td>
<td>6ES7 153–2BA81–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2BA02–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2BA01–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2BA00–0XB0</td>
</tr>
<tr>
<td>IM 153–2FO</td>
<td>6ES7 153–2AB02–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2AB01–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2AB00–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2AA02–0XB0</td>
</tr>
</tbody>
</table>

Each S7–400H subsystem is interconnected with one of the two DP slave interfaces of the ET 200M via a DP master interface.

PROFIBUS PA can be connected to a redundant system via a DP/PA link.
You can use the following DP/PA links:

<table>
<thead>
<tr>
<th>DP/PA link</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IM 157</td>
<td>6ES7 157–0BA82–0XA0</td>
</tr>
<tr>
<td></td>
<td>6ES7 157–0AA82–0XA0</td>
</tr>
<tr>
<td></td>
<td>6ES7 157–0AA81–0XA0</td>
</tr>
<tr>
<td></td>
<td>6ES7 157–0AA80–0XA0</td>
</tr>
<tr>
<td>ET 200M as DP/PA link with</td>
<td>6ES7 153–2BA02–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2BA01–0XB0</td>
</tr>
<tr>
<td></td>
<td>6ES7 153–2BA81–0XB0</td>
</tr>
</tbody>
</table>

A single-channel DP master system can be connected to a redundant system via a Y coupler. The following IM 157 Y coupler is permitted: 6ES7 197-1LB00 0XA0

The single-channel switched I/O configuration is recommended for system components which tolerate the failure of individual modules within the ET 200M.

**Rule**

A single-channel switched I/O configuration must always be symmetrical.

- This means, the fault-tolerant CPU and other DP masters must be installed in the same slots in both subsystems (e.g. slot 4 in both subsystems)
- or the DP masters must be connected to the same integrated interface in both subsystems (e.g. to the PROFIBUS DP interfaces of both fault-tolerant CPUs).

**Single-channel switched I/O configuration at the PROFINET interface**

The system supports single-channel switched I/O configurations containing an ET 200M distributed I/O module with active backplane bus and a redundant PROFINET interface.

Each S7–400H subsystem is interconnected (via a PROFINET interface) separately with the PROFINET interface of the ET 200M. Refer to chapter System redundancy (Page 99).
You can use the following interface for the I/O configuration at the PROFINET interface:

Table 13- 2  Interface for use of single-channel switched I/O configuration at the PROFINET interface

<table>
<thead>
<tr>
<th>Interface</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IM 153-4 PN</td>
<td>6ES7153-4BA00-0XB0</td>
</tr>
</tbody>
</table>

**Single-channel switched I/O and user program**

In redundant mode, in principle any subsystem can access single-channel switched I/O. The data is automatically transferred via the synchronization link and compared. An identical value is available to the two subsystems at all times owing to the synchronized access. The fault-tolerant system uses only one of the DP interfaces or PROFINET interface at any given time. The active DP interface is indicated by the ACT LED on the corresponding IM 153–2 or IM 157.

The path via the currently active DP interface or PROFINET interface is called the **active channel**, while the path via the other interface is called the **passive channel**. The DP or PNIO cycle is always active on both channels. However, only the input and output values of the active channel are processed in the user program or output to the I/O. The same applies to asynchronous activities, such as interrupt processing and the exchange of data records.

**Failure of the single-channel switched I/O**

The fault-tolerant system with single-channel switched I/O responds to errors as follows:

- The I/O is no longer available after it fails.
- In certain failure situations (such as the failure of a subsystem, DP master system or DP slave interface module IM153-2 or IM 157; see chapter Communication (Page 205)), the single-channel switched I/O remains available to the process. This is achieved by a switchover between the active and passive channel. This switchover takes place separately for each DP or PNIO station. A distinction is made between the following two types of failure:
  - Failures affecting only one station (such as failure of the DP slave interface of the currently active channel)
  - Failures affecting all stations of a DP master system or PNIO system.

This includes unplugging of the connector at the DP master interface or at the PNIO interface, shutdown of the DP master system (e.g. RUN-STOP transition on a CP 443-5), and a short-circuit at the cable harness of a DP master system or PNIO system.

The following applies to each station affected by a failure: If both DP slave interfaces or PNIO connections are currently functional and the active channel fails, the previously passive channel automatically becomes active. A redundancy loss is reported to the user program when OB 70 starts (event W#16#73A3).

Once the problem is eliminated, redundant mode is restored. This also starts OB 70 (event W#16#72A3). In this situation, there is no changeover between the active and passive channel.
If one channel has already failed, and the remaining (active) channel also fails, then there is a complete station failure. This starts OB 86 (event W#16#39C4).

**Note**
If the DP master interface module can detect failure of the entire DP master system (due to short-circuit, for example), it reports only this event ("Master system failure entering state" W#16#39C3). The operating system no longer reports individual station failures. This feature can be used to accelerate the changeover between the active and passive channel.

### Duration of a changeover of the active channel

The maximum changeover time is

\[
\text{DP error detection time} + \text{DP changeover time} + \text{changeover time of the DP slave interface}
\]

You can determine the first two values from the bus parameters of your DP master system in STEP 7. You can obtain the last value from the manuals of the relevant DP slave interface module (distributed I/O device ET 200M or DP/PA bus link).

**Note**
When using fail-safe modules, always set a monitoring time for each fail-safe module that is longer than the changeover time of the active channel in the fault-tolerant system. If you ignore this rule, you risk failure of the fail-safe modules during the changeover of the active channel.

**Note**
The above calculation also includes the processing time in OB 70 or OB 86. Make sure that the processing time for a DP or PNIO station is **no longer than 1 ms**. In situations requiring extensive processing, exclude this processing from direct execution of the OBs mentioned.

**Note**
Note that the CPU can only detect a signal change if the signal duration is greater than the specified changeover time.

When there is a changeover of the entire DP master system, the changeover time of the slowest component applies to all DP components. A DP/PA link or Y link usually determines the changeover time and the associated minimum signal duration. We therefore recommend that you connect DP/PA and Y links to a separate DP master system.

When using fail-safe modules, always set a monitoring time for each fail-safe module that is longer than the changeover time of the active channel in the fault-tolerant system. If you ignore this, you risk failure of the fail-safe modules during the changeover of the active channel.

### Changeover of the active channel during link-up and updating

During link-up and updating with master/standby changeover (see chapter [Link-up sequence](Page 141)), a changeover between the active and passive channels occurs for all stations of the switched I/O. At the same time OB 72 is called.
Bumpless changeover of the active channel

To prevent the I/O failing temporarily or outputting substitute values during the changeover between the active and passive channel, the DP or PNIO stations of the switched I/O put their outputs on hold until the changeover is completed and the new active channel has taken over.

To ensure that total failure of a DP or PNIO station is also detected during the changeover, the changeover is monitored by the various DP stations and by the DP master system.

Provided the minimum I/O retention time is set correctly (see chapter Time monitoring (Page 149)), no interrupts or data records will be lost due to a changeover. There is an automatic repetition when necessary.

System configuration and project engineering

You should allocate switched I/O with different changeover times to separate chains. This, for example, simplifies the calculation of monitoring times.

13.4 Connecting redundant I/O to the PROFIBUS DP interface

What is redundant I/O?

Input/output modules are termed redundant when they exist twice and they are configured and operated as redundant pairs. The use of redundant I/O provides the highest degree of availability, because the system tolerates the failure of a CPU or of a signal module.

Note

PROFINET

The use of redundant I/O at the PROFINET interface is not possible.
13.4 Connecting redundant I/O to the PROFIBUS DP interface

Configurations

The following redundant I/O configurations are supported:

1. Redundant signal modules in the central and expansion devices
   For this purpose, the signal modules are installed in pairs in the CPU 0 and CPU 1 subsystems. Redundant I/O in central and expansion devices

   ![Redundant module pair in central and expansion devices](image)

   Figure 13-3 Redundant I/O in central and expansion devices

2. Redundant I/O in the one-sided DP slave
   To achieve this, the signal modules are installed in pairs in ET 200M distributed I/O devices with active backplane bus.
13.4 Connecting redundant I/O to the PROFIBUS DP interface

Figure 13-4   Redundant I/O in the one-sided DP slave
3. Redundant I/O in the switched DP slave

To achieve this, the signal modules are installed in pairs in ET 200M distributed I/O devices with active backplane bus.

![Redundant I/O in the switched DP slave](image)

Figure 13-5 Redundant I/O in the switched DP slave

4. Redundant I/O connected to a fault-tolerant CPU in standalone mode

![Redundant I/O in stand-alone mode](image)

Figure 13-6 Redundant I/O in stand-alone mode
Principle of channel group-specific redundancy

Channel errors due to discrepancy cause the passivation of the respective channel. Channel errors due to diagnostic interrupts (OB82) cause the passivation of the channel group affected. Depassivation de-passivates all affected channels as well as the modules passivated due to module errors. Channel group-specific passivation significantly increases availability in the following situations:

- Relatively frequent encoder failures
- Repairs that take a long time
- Multiple channel errors on one module

Note

Channel and channel group

Depending on the module, a channel group contains a single channel, a group of several channels, or all channels of the module. You can therefore operate all modules with redundancy capability in channel group-specific redundancy mode.

An up-to-date list of modules with redundancy capability can be found in section Signal modules for redundancy (Page 179).

Principle of module-specific redundancy

Redundancy always applies to the entire module, rather than to individual channels. When a channel error occurs in the first redundant module, the entire module and all of its channels are passivated. If an error occurs on another channel on the second module before the first error has been eliminated and the first module has been depassivated, this second error cannot be handled by the system.

An up-to-date list of modules with redundancy capability can be found in section Signal modules for redundancy (Page 179).
"Functional I/O redundancy" block libraries

The blocks you use for channel group-specific redundancy are located in the "Redundant IO CGP V50" library. The blocks in the library "Redundant IO CGP V40" can also be set for channel group-specific redundancy but only for a limited range of modules.

The blocks you use for module-specific redundancy are located in the "Redundant IO MGP V30" library. Module-specific redundancy is a special form of redundant module operation; see above.

**Note**

**Operating redundant modules**

When you are operating signal modules for the first time, use channel group-specific redundancy with the blocks in the "Redundant IO CGP V50" library. This ensures maximum flexibility when using redundant modules.

The "Functional I/O redundancy" block libraries that support the redundant I/O each contain the following blocks:

- **FC 450 "RED_INIT"**: Initialization function
- **FC 451 "RED_DEPA"**: Initiate depassivation
- **FB 450 "RED_IN"**: Function block for reading redundant inputs
- **FB 451 "RED_OUT"**: Function block for controlling redundant outputs
- **FB 452 "RED_DIAG"**: Function block for diagnostics of redundant I/O
- **FB 453 "RED_STATUS"**: Function block for redundancy status information

Configure the numbers of the management data blocks for the redundant I/O in HW Config "Properties CPU -> H Parameter". Assign free DB numbers to these data blocks. The data blocks are created by FC 450 "RED_INIT" during CPU startup. The default setting for the numbers of the management data blocks is 1 and 2. These data blocks are not the instance data blocks of FB 450 "RED_IN" or FB 451 "RED_OUT".

You can open the libraries in the SIMATIC Manager with "File -> Open -> Libraries".

The functions and use of the blocks are described in the corresponding online help.

**Note**

**Blocks from different libraries**

Always use blocks from a single library. Simultaneous use of blocks from different libraries is not permitted.

If you wish to replace one of the earlier libraries Redundant IO (V1) or Redundant IO CGP with the Redundant IO CGP V5.0, you must first of all edit your user program accordingly. Refer to the context-sensitive block help or the STEP 7 Readme for more information.
Switching to channel group-specific redundancy

To activate channel group-specific passivation, you have to stop the automation system (memory reset and reload user program in STOP).

Observe the following:

Mixing blocks from various libraries in one CPU is not permitted and can lead to unpredictable behavior.

When converting a project, make sure that all library blocks named FB450–453 and FC450–451 have been deleted from the block folder and replaced by the blocks from Red-IO CGP V5.0. Perform this step in every relevant program. Compile and load your project.

Using the blocks

Before you use the blocks, parameterize the redundant modules as redundant in HW Config.

The OBs into which you need to link the various blocks are listed in the table below:

<table>
<thead>
<tr>
<th>Block</th>
<th>OB</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC 450 &quot;RED_INIT&quot;</td>
<td>• OB 72 &quot;CPU redundancy error&quot; (only with fault-tolerant systems)</td>
</tr>
<tr>
<td></td>
<td>• FC 450 is only executed after the start event B#16#33:&quot;Standby-</td>
</tr>
<tr>
<td></td>
<td>• master changeover by operator&quot;</td>
</tr>
<tr>
<td></td>
<td>• OB 80 &quot;Timeout error&quot; (only in standalone mode)</td>
</tr>
<tr>
<td></td>
<td>• FC 450 is only executed after the start event &quot;Resume RUN after</td>
</tr>
<tr>
<td></td>
<td>• reconfiguring&quot;</td>
</tr>
<tr>
<td></td>
<td>• OB 100 &quot;Restart&quot; (the administration DBs are recreated, see the</td>
</tr>
<tr>
<td></td>
<td>• online help)</td>
</tr>
<tr>
<td></td>
<td>• OB 102 &quot;Cold restart&quot;</td>
</tr>
<tr>
<td>FC 451 &quot;RED_DEPA&quot;</td>
<td>• OB 83 &quot;insert/remove module interrupt&quot; or OB 85&quot;Program</td>
</tr>
<tr>
<td></td>
<td>• execution error&quot;</td>
</tr>
<tr>
<td></td>
<td>• If you call FC 451 in OB 83 while inserting modules, or in OB 85</td>
</tr>
<tr>
<td></td>
<td>• by means of outgoing interrupt, depassivation is delayed by 3</td>
</tr>
<tr>
<td></td>
<td>• seconds.</td>
</tr>
<tr>
<td></td>
<td>• OB 1 &quot;Cyclic program&quot; and/or OB 30 to 38 &quot;cyclic interrupt&quot;</td>
</tr>
<tr>
<td></td>
<td>• You must also call FC 451 conditionally in OB1 or OB 30 to 38</td>
</tr>
<tr>
<td></td>
<td>• after having eliminated the malfunction, for example, with a user</td>
</tr>
<tr>
<td></td>
<td>• acknowledgment. The FC 451 only depassivates modules in the</td>
</tr>
<tr>
<td></td>
<td>• corresponding process image partition. Depassivation is delayed by</td>
</tr>
<tr>
<td></td>
<td>• 10 seconds with Version 3.5 or higher of FB 450 &quot;RED_IN&quot; in the</td>
</tr>
<tr>
<td></td>
<td>• library &quot;Redundant IO MGP&quot; and Version 5.8 or higher of FB 450</td>
</tr>
<tr>
<td></td>
<td>• &quot;RED_IN&quot; in the library &quot;Redundant IO CGP&quot; V50.</td>
</tr>
<tr>
<td>FB 450 &quot;RED_IN&quot;</td>
<td>• OB 1 &quot;Cyclic program&quot;</td>
</tr>
<tr>
<td></td>
<td>• OB 30 to OB 38 &quot;Cyclic interrupt&quot;</td>
</tr>
<tr>
<td>FB 451 &quot;RED_OUT&quot;</td>
<td>• OB 1 &quot;Cyclic program&quot;</td>
</tr>
<tr>
<td></td>
<td>• OB 30 to OB 38 &quot;Cyclic interrupt&quot;</td>
</tr>
</tbody>
</table>
To be able to address redundant modules using process image partitions in cyclic interrupts, the relevant process image partition must be assigned to this pair of modules and to the cyclic interrupt. Call FB 450 "RED_IN" in this cyclic interrupt before you call the user program. Call FB 451 "RED_OUT" in this cyclic interrupt after you call the user program. The valid values that can be processed by the user program are always located at the lower address of both redundant modules. This means that only the lower address can be used for the application; the values of the higher address are not relevant for the application.

**Note**

**Use of FB 450 "RED_IN" and 451 "RED_OUT" when using process image partitions**

For each priority class used (OB 1, OB 30 .. OB 38), you must use a separate process image partition.
Hardware configuration and project engineering of the redundant I/O

Follow the steps below to use redundant I/O:

1. Insert all the modules you want to operate redundantly. Remember the following basic rules for configuration.

2. Configure the module redundancy using HW Config in the object properties of the relevant module.

   Either browse for a partner module for each module, or accept the default settings

   **In a centralized configuration:** If the module is in slot X of the even-numbered rack, the module at the same slot position in the next odd-numbered rack is proposed.
   If the module is in slot X of the odd-numbered rack, the module at the same slot position in the previous even-numbered rack is proposed.

   **Distributed configuration in a one-sided DP slave:** If the module is inserted in slot X of the slave, the module at the same slot X of the slave at the same PROFIBUS address in the partner DP subsystem is proposed, provided the DP master system is redundant.

   **Distributed configuration in a switched DP slave, stand-alone mode:** If the module in the slave with a DP address is inserted in slot X, the module in the slave with the next PROFIBUS address at slot X is proposed.

3. Enter the remaining redundancy parameters for the input modules.

---

**Note**

System modifications during operation are also supported with redundant I/O. You are not permitted to change the parameter settings for a redundant module per SFC.

---

**Note**

Always switch off power to the station or rack before you remove a redundant digital input module that does not support diagnostics functions and is not passivated. You might otherwise passivate the wrong module. This procedure is necessary, for example, when replacing the front connector of a redundant module.

Redundant modules must be in the process image of the inputs or outputs. Redundant modules are always accessed using the process image.

When using redundant modules, select the "Cycle/Clock Memory" tab from "HW Config - > Properties CPU 41x-H" and set the following:

"OB 85 call on I/O area access error > Only incoming and outgoing errors"

---

13.4.1 Signal modules for redundancy

Signal modules as redundant I/O

The signal modules listed below can be used as redundant I/O. Refer to the latest information about the use of modules available in the readme file and in the SIMATIC FAQ at http://www.siemens.com/automation/service&support under the keyword "Redundant I/O".
Take into account that you can only use modules of the same product version and same firmware version as redundant pairs.

Table 13-3 Signal modules for redundancy

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
</table>
| Central: Redundant DI dual-channel
| X            | X            | D1 16xDC 24V interrupt | 6ES7 421–7BH0x–0AB0       |
|              |              | Use with non-redundant encoder
|              |              | • This module supports the "wire break" diagnostic function. To implement this function, make sure that a total current between 2.4 mA and 4.9 mA flows even at signal state "0" when you use an encoder that is evaluated at two inputs in parallel.
|              |              | You achieve this by connecting a resistor across the encoder. Its value depends on the type of switch and usually ranges between 6800 and 8200 ohms for contacts.
|              |              | For BEROS, calculate the resistance based on this formula: 
|              |              | $30 \text{ V}/(4.9 \text{ mA} – I_{R_{Bero}}) < R < (20 \text{ V}/(2.4 \text{ mA} – I_{R_{Bero}})$ |
| X            | X            | DI 32xDC 24V | 6ES7 421–1BL0x–0AA0          |
| X            | X            | DI 32xUC 120V | 6ES7 421–1EL00–0AA0          |
| Distributed: Redundant DI dual-channel
| X            | X            | D1 16xDC 24 V, interrupt | 6ES7 321–7BH00–0AB0       |
|              |              | Use with non-redundant encoder
|              |              | • This module supports the "wire break" diagnostic function. To implement this function, make sure that a total current between 2.4 mA and 4.9 mA flows even at signal state "0" when you use an encoder that is evaluated at two inputs in parallel.
|              |              | You achieve this by connecting a resistor across the encoder. Its value depends on the type of switch and usually ranges between 6800 and 8200 ohms for contacts.
|              |              | For BEROS, calculate the resistance based on this formula: 
|              |              | $30 \text{ V}/(4.9 \text{ mA} – I_{R_{Bero}}) < R < (20 \text{ V}/(2.4 \text{ mA} – I_{R_{Bero}})$ |
| X            | X            | D1 16xDC 24 V | 6ES7 321–1BH02–0AA0          |
|              | X            | In some system states, it is possible that an incorrect value of the first module is read in briefly when the front connector of the second module is removed. This is prevented by using series diodes like those shown in figure F.1. |
| X            | X            | D1 32xDC 24 V | 6ES7 321–1BL00–0AA0          |
|              | X            | In some system states, it is possible that an incorrect value of the first module is read in briefly when the front connector of the second module is removed. This is prevented by using series diodes like those shown in figure F.2. |
### 13.4 Connecting redundant I/O to the PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DI 8xAC 120/230V</td>
<td>6ES7 321–1FF01–0AA0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DI 4xNamur [EEx ib]</td>
<td>6ES7 321–7RD00–0AB0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DI 16xNamur</td>
<td>6ES7321–7TH00–0AB0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DI 24xDC 24 V</td>
<td>6ES7326–1BK00–0AB0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DI 8xNAMUR [EEx ib]</td>
<td>6ES7326–1RF00–0AB0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 32xDC 24V/0.5A</td>
<td>6ES7422–7BL00–0AB0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 16xAC 120/230V/2A</td>
<td>6ES7422–1FH00–0AA0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 8xDC 24 V/0.5 A</td>
<td>6ES7322–8BF00–0AB0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 8xDC 24 V/2 A</td>
<td>6ES7322–1BF01–0AA0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 32xDC 24 V/0.5 A</td>
<td>6ES7322–1BL00–0AA0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 8xAC 120/230 V/2 A</td>
<td>6ES7322–1FF01–0AA0</td>
</tr>
</tbody>
</table>

---

You cannot use the module for applications in hazardous areas in redundant mode.

Use with non-redundant encoder
- You can only connect 2-wire NAMUR encoders or contact makers.
- Equipotential bonding of the encoder circuit should always be at one point only (preferably encoder negative).
- When selecting encoders, compare their properties with the specified input characteristics. Remember that this function must always be available, regardless of whether you are using one or two inputs. Example of valid values for NAMUR encoders: for "0" current > 0.2 mA; for "1" current > 4.2 mA.

Use with non-redundant encoder
- Equipotential bonding of the encoder circuit should always be at one point only (preferably encoder negative).
- Operate the two redundant modules on a common load power supply.
- When selecting encoders, compare their properties with the specified input characteristics. Remember that this function must always be available, regardless of whether you are using one or two inputs. Example of valid values for NAMUR encoders: for "0" current > 0.7 mA; for "1" current > 4.2 mA.

A clear evaluation of the diagnostics information "P short-circuit", "M short-circuit" and wire break is not possible. Deselect these individually in your configuration.

The minimum I/O retention time remains ineffective in the case of a plant change during operation. As a result, no bumpless switchover of this module is possible, with configured module redundancy, for example. There is always a gap of 3 to 50 ms.

A definite evaluation of the diagnostics information "P short-circuit" and "wire break" is not possible. Deselect these individually in your configuration.
### 13.4 Connecting redundant I/O to the PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 4x24 V/10 mA [EEEx ib]</td>
<td>6ES7322–5SD00–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>You cannot use the module for applications in hazardous areas in redundant mode.</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 4x24 V/10 mA [EEEx ib]</td>
<td>6ES7322–5RD00–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>You cannot use the module for applications in hazardous areas in redundant mode.</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 16xDC 24 V/0.5 A</td>
<td>6ES7322–8BH01–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The equipotential bonding of the load circuit should always take place from one point only (preferably load minus).</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Diagnostics of the channels is not possible.</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 16xDC 24 V/0.5 A</td>
<td>6ES7322–8BH10–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The equipotential bonding of the load circuit should always take place from one point only (preferably load minus).</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DO 10xDC 24 V/2 A, product version 3 or higher</td>
<td>6ES7326–2BF01–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F module in standard mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The inputs and outputs must have the same address.</td>
<td></td>
</tr>
</tbody>
</table>

#### Central: Redundant AI dual-channel

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>AI 16x16Bit</td>
<td>6ES7431–7QH00–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Use in voltage measurement</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The &quot;wire break&quot; diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Use in indirect current measurement</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Use a 50 ohm resistor (measuring range +/- 1 V) or 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage, see figure 10-9. The tolerance of the resistor must be added on to the module error.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Use in direct current measurement</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Suitable Zener diode: BZX85C6v2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Load capability of 4-wire transmitters: ( R_\text{fl} &gt; 325 \text{ ohms} ) (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to ( R_\text{fl} = (R_\text{fl} * I_{\text{max}} + U_{z_{\text{max}}})/I_{\text{max}} ))</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Input voltage in the circuit when operating with a 2-wire transmitter: ( U_{e-2w} &lt; 8 \text{V} ) (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to ( U_{e-2w} = R_\text{fl} * I_{\text{max}} + U_{z_{\text{max}}} ))</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The circuit shown in figure 10-10 works only with active (4-wire) transmitters or with passive (2-wire) transmitters with external power supply. Always parameterize the module channels for operation as &quot;4-wire transmitter&quot;, and set the measuring range cube to position &quot;C&quot;. It is not possible to power the transmitters via the module (2DMU).</td>
<td></td>
</tr>
</tbody>
</table>
Connecting redundant I/O to the PROFIBUS DP interface

### Use in voltage measurement
- The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected.

### Use for indirect current measurement
- When determining the measuring error, observe the following: The total input resistance in measuring ranges > 2.5 V is reduced from a nominal 100 kOhm to 50 kOhm when operating two inputs connected in parallel.
- The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected.
- Use a 50 ohm resistor (measuring range +/- 1 V) or 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage, see figure 10-9. The tolerance of the resistor must be added on to the module error.
- This module is not suitable for direct current measurement.

### Use of redundant encoders:
- You can use a redundant encoder with the following voltage settings:
  - +/- 80 mV (only without wire break monitoring)
  - +/- 250 mV (only without wire break monitoring)
  - +/- 500 mV (wire break monitoring not configurable)
  - +/- 1 V (wire break monitoring not configurable)
  - +/- 2.5 V (wire break monitoring not configurable)
  - +/- 5 V (wire break monitoring not configurable)
  - +/- 10 V (wire break monitoring not configurable)
  - 1...5 V (wire break monitoring not configurable)
### 13.4 Connecting redundant I/O to the PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>AI 8x16Bit</td>
<td>6ES7 331–7NF00–0AB0</td>
</tr>
</tbody>
</table>

#### Use in voltage measurement
- The "wire break" diagnostics function in HW Config must not be activated when operating the modules with transmitters.

#### Use in indirect current measurement
- When using indirect current measurement, ensure a reliable connection between the sensor resistances and the actual inputs, because a reliable wire break detection cannot be guaranteed in the case of a wire break of individual cables of this connection.
- Use a 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage; see figure 10-9.

#### Use in direct current measurement
- Suitable Zener diode: BZX85C8v2
- Circuit-specific additional error: If one module fails, the other may suddenly show an additional error of approx. 0.1%.
- Load capability of 4-wire transmitters: $R_B > 610 \text{ ohms}$
  (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to $R_B = \frac{(R_E \cdot I_{\text{max}} + U_{Z\text{max}})}{I_{\text{max}}}$)
- Input voltage in the circuit when operating with a 2-wire transmitter: $U_{e-2w} < 15 \text{ V}$
  (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to $U_{e-2w} = R_E \cdot I_{\text{max}} + U_{Z\text{max}}$)

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>AI 8x16Bit</td>
<td>6ES7 331–7NF10–0AB0</td>
</tr>
</tbody>
</table>

#### Use in voltage measurement
- The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected.

#### Use in indirect current measurement
- Use a 250 ohm resistor (measuring range 1 - 5 V) to map the current on a voltage; see figure 10-9.

#### Use in direct current measurement
- Suitable Zener diode: BZX85C8v2
- Load capability of 4-wire transmitters: $R_B > 610 \text{ ohms}$
  (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to $R_B = \frac{(R_E \cdot I_{\text{max}} + U_{Z\text{max}})}{I_{\text{max}}}$)
- Input voltage in the circuit when operating with a 2-wire transmitter: $U_{e-2w} < 15 \text{ V}$ (determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to $U_{e-2w} = R_E \cdot I_{\text{max}} + U_{Z\text{max}}$)
### 13.4 Connecting redundant I/O to the PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>AI 6xTC 16Bit iso, 6ES7331-7PE10-0AB0</td>
<td>6ES7331-7PE10-0AB0</td>
</tr>
</tbody>
</table>

**Notice:** These modules must only be used with redundant encoders.

You can use this module with Version 3.5 or higher of FB 450 "RED_IN" in the library "Redundant IO MGP" and Version 5.8 or higher of FB 450 "RED_IN" in the library "Redundant IO CGP" V50.

Observe the following when measuring temperatures by means of thermocouples and parameterized redundancy:

The value specified in "Redundancy" under "Tolerance window" is always based on 2764.8 °C. For example, a tolerance of 27 °C is checked if "1" is entered, or a tolerance of 138 °C is checked if "5" is entered.

A firmware update is not possible in redundant operation.

Online calibration is not possible in redundant operation.

Use in voltage measurement

- The "wire break" diagnostics function in HW Config must not be activated when operating the modules with thermocouples.

Use in indirect current measurement

- Due to the maximum voltage range +/- 1 V, the indirect current measurement can be carried out exclusively via a 50 ohm resistor. Mapping that conforms to the system is only possible for the area +/- 20 mA.

| X            | X            | AI 4x15Bit [EEx ib] | 6ES7331-7RD00-0AB0 |

You cannot use the module for applications in hazardous areas in redundant mode.

It is not suitable for indirect current measurement.

Use in direct current measurement

- Suitable Zener diode: BZX85C6v2
- Load capability of 4-wire transmitters: RB > 325 ohms determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to RB = \( \frac{RE \cdot I_{max} + U_{z \ max}}{I_{max}} \)
- Input voltage for 2-wire transmitters: \( U_{e-2w} < 8 \) V determined for worst case: 1 input + 1 Zener diode at an S7 overload value 24 mA to \( U_{e-2w} = RE \cdot I_{max} + U_{z \ max} \)

**Note:** You can only connect 2-wire transmitters with a 24 V external supply or 4-wire transmitters. The internal power supply for transmitters cannot be used in the circuit shown in figure 8-10, because this outputs only 13 V, and thus in the worst case it would supply only 5 V to the transmitter.

| X            | X            | AI 6x13Bit | 6ES7 336–1HE00–0AB0 |

F module in standard mode

| X            | X            | X            | AI 8x0/4...20mA HART | 6ES7 331–7TF01-0AB0 |

A firmware update is not possible in redundant operation.

Online calibration is not possible in redundant operation.

See *Distributed I/O Device ET 200M; HART Analog Modules* manual

**Distributed: Redundant AO dual-channel**

| X | X | AO4x12 Bit | 6ES7332–5HD01–0AB0 |
| X | X | AO8x12 Bit | 6ES7332–5HF00–0AB0 |
Using I/Os in S7–400H

13.4 Connecting redundant I/O to the PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Library V5.x</th>
<th>Library V4.x</th>
<th>Library V3.x</th>
<th>Module</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>AO4x0/4...20 mA [EEx ib]</td>
<td>6ES7332–5RD00–0AB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>You cannot use the module for applications in hazardous areas in redundant mode.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X</th>
<th>X</th>
<th>X</th>
<th>AO 8x0/4...20mA HART</th>
<th>6ES7332–8TF01–0AB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>A firmware update is not possible in redundant operation. Online calibration is not possible in redundant operation. See Manual ET 200M Distributed I/O Device; HART Analog Modules</td>
<td></td>
</tr>
</tbody>
</table>

Note

You need to install the F ConfigurationPack for F modules. The F ConfigurationPack can be downloaded free of charge from the Internet. You can get it from Customer Support at: http://www.siemens.com/automation/service&support.

Quality levels in the redundant configuration of signal modules

The availability of modules in the case of an error depends on their diagnostics possibilities and the fine granularity of the channels.

Using digital input modules as redundant I/O

The following parameters were set to configure digital input modules for redundant operation:

- Discrepancy time (maximum permitted time in which the redundant input signals may differ). The specified discrepancy time must be a multiple of the update time of the process image and therefore also the basic conversion time of the channels. When there is still a discrepancy in the input values after the configured discrepancy time has expired, an error has occurred.

- Response to a discrepancy in the input values

  First, the input signals of the paired redundant modules are checked for consistency. If the values match, the uniform value is written to the lower memory area of the process input image. If there is a discrepancy and it is the first, it is marked accordingly and the discrepancy time is started.

  During the discrepancy time, the most recent matching (non-discrepant) value is written to the process image of the module with the lower address. This procedure is repeated until the values once again match within the discrepancy time or until the discrepancy time of a bit has expired.

  If the discrepancy continues past the expiration of the configured discrepancy time, an error has occurred.
The defective side is localized according to the following strategy:

1. During the discrepancy time, the most recent matching value is retained as the result.

2. Once the discrepancy time has expired, the following error message is displayed:
   Error code 7960: "Redundant I/O: discrepancy time at digital input expired, error not yet localized". Passivation is not performed and no entry is made in the static error image. Until the next signal change occurs, the configured response is performed after the discrepancy time expires.

3. If another signal change occurs, the module/channel in which the signal change occurred is the intact module/channel and the other module/channel is passivated.

**Note**

The time that the system actually needs to determine a discrepancy depends on various factors: Bus delay times, cycle and call times in the user program, conversion times, etc. Redundant input signals can therefore be different for a longer period than the configured discrepancy time.

Modules with diagnostics capability are also passivated by calling OB 82.

**Using redundant digital input modules with non-redundant encoders**

With non-redundant encoders, you use digital input modules in a 1-out-of-2 configuration:

![Figure 13-7 Fault-tolerant digital input module in 1-out-of-2 configuration with one encoder](image)

The use of redundant digital input modules increases their availability.

Discrepancy analysis detects "Continuous 1" and "Continuous 0" errors of the digital input modules. A "Continuous 1" error means the value 1 is applied permanently at the input, a "Continuous 0" error means that the input is not energized. This can be caused, for example, by a short-circuit to L+ or M.

The current flow over the chassis ground connection between the modules and the encoder should be the minimum possible.

When connecting an encoder to several digital input modules, the redundant modules must operate at the same reference potential.

If you want to replace a module during operation and are not using redundant encoders, you will need to use decoupling diodes.
You will find interconnection examples in Appendix Connection examples for redundant I/Os (Page 433).

**Note**

Remember that the proximity switches (Beros) must provide the current for the channels of both digital input modules. The technical data of the respective modules, however, specify only the required current per input.

**Using redundant digital input modules with redundant encoders**

With redundant encoders you use digital input modules in a 1-out-of-2 configuration:

![Digital input modules](image_url)

Figure 13-8 Fault-tolerant digital input modules in 1-out-of-2 configuration with two encoders

The use of redundant encoders also increases their availability. A discrepancy analysis detects all errors, except for the failure of a non-redundant load voltage supply. You can enhance availability by installing redundant load power supplies.

You will find interconnection examples in Appendix Connection examples for redundant I/Os (Page 433).
13.4 Connecting redundant I/O to the PROFINET interface

Redundant digital output modules

Fault-tolerant control of a final controlling element can be achieved by connecting two outputs of two digital output modules or fail-safe digital output modules in parallel (1-out-of-2 configuration).

![Interconnection using external diodes](image1)

![Interconnection without external diodes](image2)

Figure 13-9 Fault-tolerant digital output modules in 1-out-of-2 configuration

The digital output modules must be connected to a common load voltage supply.

You will find interconnection examples in Appendix [Connection examples for redundant I/Os](Page 433).

Interconnection using external diodes <-> without external diodes

The table below lists the redundant digital output modules which in redundant mode you should interconnect using external diodes:

<table>
<thead>
<tr>
<th>Module</th>
<th>with diodes</th>
<th>without diodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>6ES7 422–7BL00–0AB0</td>
<td>X</td>
<td>-</td>
</tr>
<tr>
<td>6ES7 422–1FH00–0AA0</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 326–2BF01–0AB0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 322–1BL00–0AA0</td>
<td>X</td>
<td>-</td>
</tr>
<tr>
<td>6ES7 322–1BF01–0AA0</td>
<td>X</td>
<td>-</td>
</tr>
<tr>
<td>6ES7 322–8BF00–0AB0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 322–1FF01–0AA0</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 322–8BH01–0AB0</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 322–8BH10–0AB0</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 322–5RD00–0AB0</td>
<td>X</td>
<td>-</td>
</tr>
<tr>
<td>6ES7 322–5SD00–0AB0</td>
<td>X</td>
<td>-</td>
</tr>
</tbody>
</table>
Information on connecting with diodes

- Suitable diodes are diodes with $U_r \geq 200 \text{ V}$ and $I_F \geq 1 \text{ A}$ (e.g. types from the series 1N4003 ... 1N4007).
- It is advisable to separate the ground of the module and the ground of the load. There must be equipotential bonding between both.

Using analog input modules as redundant I/O

You specified the following parameters when you configured the analog input modules for redundant mode:

- Tolerance window (configured as a percentage of the end value of the measuring range)
  Two analog values are considered equal if they are within the tolerance window.
- Discrepancy time (maximum permitted time in which the redundant input signals can be outside the tolerance window).
  The specified discrepancy time must be a multiple of the update time of the process image and therefore also the basic conversion time of the channels.
  An error is generated when there is an input value discrepancy after the configured discrepancy time has expired.
  If you connect identical sensors to both analog input modules, the default value for the discrepancy time is usually sufficient. If you use different sensors, in particular temperature sensors, you will have to increase the discrepancy time.

- Applied value
  The applied value represents the value of the two analog input values that is applied to the user program.

The system verifies that the two read-in analog values are within the configured tolerance window. If they are, the applied value is written to the lower data memory area of the process input image. If there is a discrepancy and it is the first, it is marked accordingly and the discrepancy time is started.

When the discrepancy time is running, the most recent valid value is written to the process image of the module with the lower address and made available to the current process. If the discrepancy time expires, the module/channel with the configured standard value is declared as valid and the other module/channel is passivated. If the maximum value from both modules is parameterized as the standard value, this value is then taken for further program execution and the other module/channel is passivated. If the minimum value is configured, this module/channel supplies the data to the process and the module with the maximum value is passivated. In any case, the passivated modules/channels are entered in the diagnostic buffer.

If the discrepancy is eliminated within the discrepancy time, analysis of the redundant input signals is still carried out.

**Note**

The time that the system actually needs to determine a discrepancy depends on various factors: Bus delay times, cycle and call times in the user program, conversion times, etc. Redundant input signals can therefore be different for a longer period than the configured discrepancy time.
Note
There is no discrepancy analysis when a channel reports an overflow with 16#7FFF or an underflow with 16#8000. The relevant module/channel is passivated immediately.
You should therefore disable all unused inputs in HW Config using the "Measurement type" parameter.

Redundant analog input modules with non-redundant encoder
With non-redundant encoders, analog input modules are used in a 1-out-of-2 configuration:

- Connect the analog input modules in parallel for voltage sensors (left in figure).
- You can convert a current into voltage using an external load to be able to use voltage analog input modules connected in parallel (center in the figure).
- 2-wire transmitters are powered externally to allow you to repair the module online.

The redundancy of the fail-safe analog input modules enhances their availability.
You will find interconnection examples in Appendix Connection examples for redundant I/Os (Page 433).

Redundant analog input modules for indirect current measurement
The following applies to the wiring of analog input modules:
- Suitable encoders for this circuit are active transmitters with voltage output and thermocouples.
- The "wire break" diagnostics function in HW Config must not be activated, neither when operating the modules with transmitters nor when thermocouples are connected.
● Suitable encoder types are active 4-wire and passive 2-wire transmitters with output ranges +/-20 mA, 0...20 mA, and 4...20 mA. 2-wire transmitters are powered by an external auxiliary voltage.

● Criteria for the selection of resistance and input voltage range are the measurement accuracy, number format, maximum resolution and possible diagnostics.

● In addition to the options listed, other input resistance and voltage combinations according to Ohm’s law are also possible. Note, however, that such combinations may lead to loss of the number format, diagnostics function and resolution. The measurement error also depends largely on the size of the measure resistance of certain modules.

● Use a measure resistance with a tolerance of +/- 0.1% and TC 15 ppm.

Additional conditions for specific modules

AI 8x12bit 6ES7 331–7K..02–0AB0

- Use a 50 ohm or 250 ohm resistor to map the current on a voltage:

<table>
<thead>
<tr>
<th>Resistor</th>
<th>50 ohms</th>
<th>250 ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current measuring range</td>
<td>+/-20 mA</td>
<td>+/-20 mA *)</td>
</tr>
<tr>
<td>Input range to be parameterized</td>
<td>+/-1 V</td>
<td>+/-5 V</td>
</tr>
<tr>
<td>Measuring range cube position</td>
<td>&quot;A&quot;</td>
<td>&quot;B&quot;</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bits + sign</td>
<td>12 bits + sign</td>
</tr>
<tr>
<td>S7 number format</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Circuit-specific measuring error</td>
<td>-</td>
<td>0.5%</td>
</tr>
<tr>
<td>- 2 parallel inputs</td>
<td>-</td>
<td>0.25%</td>
</tr>
<tr>
<td>- 1 input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;Wire break&quot; diagnostics</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Load for 4-wire transmitters</td>
<td>50 ohms</td>
<td>250 ohms</td>
</tr>
<tr>
<td>Input voltage for 2-wire transmitters</td>
<td>&gt; 1.2 V</td>
<td>&gt; 6 V</td>
</tr>
<tr>
<td>(*) The AI 8x12bit outputs diagnostic interrupt and measured value &quot;7FFF&quot; in the event of wire break</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The listed measuring error results solely from the interconnection of one or two voltage inputs with a measure resistance. Allowance has neither been made here for the tolerance nor for the basic/operational limits of the modules.

The measuring error for one or two inputs shows the difference in the measurement result depending on whether two inputs or, in case of error, only one input acquires the current of the transmitter.

AI 8x16bit 6ES7 331–7NF00–0AB0

- Use a 250 ohm resistor to map the current on a voltage:

<table>
<thead>
<tr>
<th>Resistor</th>
<th>250 ohms *)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current measuring range</td>
<td>+/-20 mA</td>
</tr>
<tr>
<td>Input range to be parameterized</td>
<td>+/-5 V</td>
</tr>
<tr>
<td>Resolution</td>
<td>15 bits + sign</td>
</tr>
<tr>
<td>S7 number format</td>
<td>x</td>
</tr>
</tbody>
</table>
13.4 Connecting redundant I/O to the PROFIBUS DP interface

<table>
<thead>
<tr>
<th>Resistor</th>
<th>250 ohms *)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit-specific measuring error</td>
<td>-</td>
</tr>
<tr>
<td>- 2 parallel inputs</td>
<td>-</td>
</tr>
<tr>
<td>- 1 input</td>
<td>-</td>
</tr>
<tr>
<td>&quot;Wire break&quot; diagnostics</td>
<td>- x</td>
</tr>
<tr>
<td>Load for 4-wire transmitters</td>
<td>250 ohms</td>
</tr>
<tr>
<td>Input voltage for 2-wire transmitters</td>
<td>&gt; 6 V</td>
</tr>
</tbody>
</table>

*) It may be possible to use the freely connectable internal 250 ohm resistors of the module

AI 16x16bit 6ES7 431–7QH00–0AB0

- Use a 50 ohm or 250 ohm resistor to map the current on a voltage:

<table>
<thead>
<tr>
<th>Resistor</th>
<th>50 ohms</th>
<th>250 ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current measuring range</td>
<td>+/-20 mA</td>
<td>+/-20 mA</td>
</tr>
<tr>
<td>Input range to be configured</td>
<td>+/-1 V</td>
<td>+/-5 V</td>
</tr>
<tr>
<td>Measuring range cube position</td>
<td>&quot;A&quot;</td>
<td>&quot;A&quot;</td>
</tr>
<tr>
<td>Resolution</td>
<td>15 bits + sign</td>
<td>15 bits + sign</td>
</tr>
<tr>
<td>S7 number format</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Circuit-specific measuring error 1)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>- 2 parallel inputs</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>- 1 input</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>&quot;Wire break&quot; diagnostics</td>
<td>-</td>
<td>- x</td>
</tr>
<tr>
<td>Load for 4-wire transmitters</td>
<td>50 ohms</td>
<td>250 ohms</td>
</tr>
<tr>
<td>Input voltage for 2-wire transmitters</td>
<td>&gt; 1.2 V</td>
<td>&gt; 6 V</td>
</tr>
</tbody>
</table>

**Redundant analog input modules for direct current measurement**

Requirements for wiring analog input modules according to Figure 8-10:

- Suitable encoder types are active 4-wire and passive 2-wire transmitters with output ranges +/-20 mA, 0...20 mA, and 4...20 mA. 2-wire transmitters are powered by an external auxiliary voltage.
- The "wire break" diagnostics function supports only the 4...20 mA input range. All other unipolar or bipolar ranges are excluded in this case.
- Suitable diodes include the types of the BZX85 or 1N47..A series (Zener diodes 1.3 W) with the voltages specified for the modules. When selecting other elements, make sure that the reverse current is as low as possible.
- A fundamental measuring error of max. 1 µA results from this type of circuit and the specified diodes due to the reverse current. In the 20 mA range and at a resolution of 16 bits, this value leads to an error of < 2 bits. Individual analog inputs in the circuit above lead to an additional error, which may be listed in the constraints. The errors specified in the manual must be added to these errors for all modules.
The 4-wire transmitters used must be capable of driving the load resulting from the circuit above. You will find details in the technical specifications of the individual modules.

When connecting up 2-wire transmitters, note that the Zener diode circuit weighs heavily in the power budget of the transmitter. The required input voltages are therefore included in the technical specifications of the individual modules. Together with the inherent supply specified on the transmitter data sheet, the minimum supply voltage is calculated to:

\[ L^+ > U_{e-2w} + U_{IS-TR} \]

Redundant analog input modules with redundant encoders

With double-redundant encoders, it is better to use fail-safe analog input modules in a 1-out-of-2 configuration:

![Analog input module](image)

The use of redundant encoders also increases their availability.

A discrepancy analysis also detects external errors, except for the failure of a non-redundant load voltage supply.

You will find interconnection examples in Appendix Connection examples for redundant I/Os (Page 433).

The general comments made at the beginning of this documentation apply.

Redundant encoders <-> non-redundant encoders

The table below shows you which analog input modules you can operate in redundant mode with redundant or non-redundant encoders:

<table>
<thead>
<tr>
<th>Module</th>
<th>Redundant encoders</th>
<th>Non-redundant encoders</th>
</tr>
</thead>
<tbody>
<tr>
<td>6ES7 431–7QH00–0AB0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 336–1HE00–0AB0</td>
<td>X</td>
<td>-</td>
</tr>
<tr>
<td>6ES7 331–7KF02–0AB0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 331–7NF00–0AB0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6ES7 331–7RD00–0AB0</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
13.4 Connecting redundant I/O to the PROFIBUS DP interface

Redundant analog output modules

You implement fault-tolerant control of a final controlling element by wiring two outputs of two analog output modules in parallel (1-out-of-2 structure).

![Analog output modules diagram](image)

Figure 13-12 Fault-tolerant analog output modules in 1-out-of-2 configuration

The following applies to the wiring of analog output modules:

- Wire the ground connections in a star structure to avoid output errors (limited common-mode suppression of the analog output module).

Information on connecting with diodes

- Suitable diodes are diodes with $U_r >= 200$ V and $I_F >= 1$ A (e.g. types from the series 1N4003 ... 1N4007).
- A separate load supply is advisable. There must be equipotential bonding between both load supplies.

Analog output signals

Only analog output modules with current outputs (0 to 20 mA, 4 to 20 mA) can be operated redundantly.

The output value is divided by 2, and each of the two modules outputs half. If one of the modules fails, the failure is detected and the remaining module outputs the full value. As a result, the surge at the output module in the event of an error is not as high.

Note

The output value drops briefly to half, and after the reaction in the program it is returned to the proper value. The duration of the output value drop is determined by the following time intervals:

- Time interval between the initial occurrence of an interrupt and the interrupt report reaching the CPU.
- Time interval until the next FB 453 call.
- Time interval until the intact analog output module has doubled the output value.
In the case of passivation or a CPU STOP, redundant analog outputs output a parameterizable minimum current of approximately 120-1000 μA per module (or 240-1000 μA for HART analog output modules), i.e. a total of approximately 240-2000 μA (or 480-2000 μA for HART analog output modules). Considering the tolerance, this means that the output value is always positive.

A configured substitute value of 0 mA will produce at least these output values. In redundant mode, in the event of a CPU STOP, the response of the current outputs is automatically set to "zero current and zero voltage" in their configuration. You can also specify a configurable compensation current of 0-400 μA for an output range of 4-20 mA.

This means you have the option of matching the minimum/compensation current to the connected I/O.

To minimize the error of the total current at the summing point in case of one-sided passivation, the parameterized compensation current is subtracted in this case from the current of the depassivated (i.e. active) channel with a pre-set value of 4 mA (range ±20 μA).

**Note**

If both channels of a channel pair were passivated (e.g. by OB 85), the respective half of the current value is still output to both storage locations in the process image of outputs. If one channel is depassivated, then the full value is output on the available channel. If this is not required, a substitute value must be written to the lower channels of both modules prior to executing FB 451 "RED_OUT".

---

**Depassivation of modules**

Passivated modules are depassivated by the following events:

- When the fault-tolerant system starts up
- When the fault-tolerant system changes over to "redundant" mode
- After system modifications during operation
- If you call FC 451 "RED_DEPA" and at least one redundant channel or module is passivated.

The depassivation is executed in FB 450 "RED IN" after one of these events has occurred. Completion of the depassivation of all modules is logged in the diagnostic buffer.

**Note**

When a redundant module is assigned a process image partition and the corresponding OB is not available on the CPU, the complete passivation process may take approximately 1 minute.
13.4 Connecting redundant I/O to the PROFIBUS DP interface

13.4.2 Evaluating the passivation status

Procedure

First, determine the passivation status by evaluating the status byte in the status/control word "FB_RED_IN.STATUS_CONTROL_W". If you see that one or more modules have been passivated, determine the status of the respective module pairs in MODUL_STATUS_WORD.

Evaluating the passivation status using the status byte

The status word "FB_RED_IN.STATUS_CONTROL_W" is located in the instance DB of FB 450 "RED_IN". The status byte returns information on the status of the redundant I/Os. The assignment of the status byte is described in the online help for the respective block library.

Evaluating the passivation status of individual module pairs by means of MODUL_STATUS_WORD

MODUL_STATUS_WORD is an output parameter of FB 453 and can be interconnected accordingly. It returns information on the status of individual module pairs.

The assignment of the MODUL_STATUS_WORD status byte is described in the online help for the respective function block library.
13.5 Other options for connecting redundant I/Os

Redundant I/O at user level

If you cannot use the redundant I/O supported by your system (section Connecting redundant I/O to the PROFIBUS DP interface), for example because the relevant module may not be listed among the supported components, you can implement the use of redundant I/O at the user level.

Configurations

The following redundant I/O configurations are supported:

1. Redundant configuration with one-sided central and/or distributed I/O.
   For this purpose, one signal module each is inserted into the CPU 0 and CPU 1 subsystems.

2. Redundant configuration with switched I/O
   One signal module each is inserted into two ET 200M distributed I/O devices with active backplane bus.

Note

When using redundant I/O, you may need to add time to the calculated monitoring times; see section Determining the monitoring times (Page 152).
Hardware configuration and project engineering of the redundant I/O

Strategy recommended for use of redundant I/O:

1. Use the I/O as follows:
   - in a one-sided configuration, one signal module in each subsystem
   - in a switched configuration, one signal module each in two ET 200M distributed I/O devices.

2. Wire the I/O in such a way that it can be addressed by both subsystems.

3. Configure the signal modules so that they have different logical addresses.

Note

It is not advisable to configure the input and output modules with the same logical addresses. Otherwise, in addition to the logical address, you will also need to query the type (input or output) of the defective module in OB 122.

The user program also has to update the process image for redundant one-sided output modules when the system is in single mode (direct access, for example). If you use process image partitions, the user program must update them (SFC 27 "UPDAT_PO") in OB 72 (recovery of redundancy). The system would otherwise first output old values on the single-channel one-sided output modules of the reserve CPU when the system changes to redundant mode.

Redundant I/O in the user program

The sample program below shows the use of two redundant digital input modules:

- Module A in rack 0 with logical start address 8 and
- Module B in rack 1 with logical start address 12.

One of the two modules is read in OB 1 by direct access. For the following it is generally assumed that the module in question is A (value of variable MODA is TRUE). If no error occurred, processing continues with the value read.

If an I/O area access error has occurred, module B is read by direct access ("second try" in OB 1). If no error occurred, processing of module B continues with the value read. However, if an error has also occurred here, both modules are currently defective, and operation continues with a substitute value.

The sample program is based on the fact that following an access error on module A and its replacement, module B is always processed first in OB 1. Module A is not processed first again in OB 1 until an access error occurs on module B.

Note

The MODA and IOAE_BIT variables must also be valid outside OB 1 and OB 122. The ATTEMPT2 variable, however, is used only in OB 1.
13.5 Other options for connecting redundant I/Os

Figure 13-14 Flow chart for OB 1
Example in STL

The required elements of the user program (OB 1, OB 122) are listed below.

Table 13- 6  Example of redundant I/O, OB 1 part

<table>
<thead>
<tr>
<th>STL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP 0;</td>
<td></td>
</tr>
<tr>
<td>SET;</td>
<td></td>
</tr>
<tr>
<td>R ATTEMPT2;</td>
<td>//Initialization</td>
</tr>
<tr>
<td>A MODA;</td>
<td>//Read module A first?</td>
</tr>
<tr>
<td>JCN CMOB;</td>
<td>//If not, continue with module B</td>
</tr>
<tr>
<td>CMOA: SET;</td>
<td></td>
</tr>
<tr>
<td>R IOAE_BIT;</td>
<td>//Delete IOAE bit</td>
</tr>
<tr>
<td>L PID 8;</td>
<td>//Read from CPU 0</td>
</tr>
<tr>
<td>A IOAE_BIT;</td>
<td>//Was IOAE detected in OB 122?</td>
</tr>
<tr>
<td>JCN IOOK;</td>
<td>//If not, process access OK</td>
</tr>
<tr>
<td>A ATTEMPT2;</td>
<td>//Was this access the second attempt?</td>
</tr>
<tr>
<td>JC CMO0;</td>
<td>//If yes, use substitute value</td>
</tr>
<tr>
<td>SET;</td>
<td></td>
</tr>
<tr>
<td>R MODA;</td>
<td>//Do not read module A first any more</td>
</tr>
<tr>
<td></td>
<td>//in future</td>
</tr>
<tr>
<td>S ATTEMPT2;</td>
<td></td>
</tr>
<tr>
<td>CMOB: SET;</td>
<td></td>
</tr>
<tr>
<td>R IOAE_BIT;</td>
<td>//Delete IOAE bit</td>
</tr>
<tr>
<td>L PID 12;</td>
<td>//Read from CPU 1</td>
</tr>
<tr>
<td>A IOAE_BIT;</td>
<td>//Was IOAE detected in OB 122?</td>
</tr>
<tr>
<td>JCN IOOK;</td>
<td>//If not, process access OK</td>
</tr>
<tr>
<td>A ATTEMPT2;</td>
<td>//Was this access the second attempt?</td>
</tr>
<tr>
<td>JC CMO0;</td>
<td>//If yes, use substitute value</td>
</tr>
<tr>
<td>SET;</td>
<td></td>
</tr>
<tr>
<td>S MODA;</td>
<td>//Read module A first again in future</td>
</tr>
<tr>
<td>S ATTEMPT2;</td>
<td></td>
</tr>
<tr>
<td>JU CMOA;</td>
<td></td>
</tr>
<tr>
<td>CMOO: L SUBS;</td>
<td>//Substitute value</td>
</tr>
<tr>
<td>IOOK:</td>
<td>//The value to be used is in ACCU1</td>
</tr>
</tbody>
</table>
### Other options for connecting redundant I/Os

#### Example of redundant I/O, OB 122 part

<table>
<thead>
<tr>
<th>STL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L OB122_MEM_ADDR;</td>
<td>// Does module A cause IOAE?</td>
</tr>
<tr>
<td>L W#16#8;</td>
<td>// Relevant logical base address</td>
</tr>
<tr>
<td>== I;</td>
<td>// Module A?</td>
</tr>
<tr>
<td>JCN M01;</td>
<td>// If not, continue with M01</td>
</tr>
<tr>
<td>SET;</td>
<td>// IOAE during access to module A</td>
</tr>
<tr>
<td>= IOAE_BIT;</td>
<td>// Set IOAE bit</td>
</tr>
<tr>
<td>JU CONT;</td>
<td>// Does module B cause an IOAE?</td>
</tr>
<tr>
<td>M01: NOP 0;</td>
<td></td>
</tr>
<tr>
<td>L OB122_MEM_ADDR;</td>
<td>// Relevant logical start address</td>
</tr>
<tr>
<td>L W#16#C;</td>
<td>// Module B?</td>
</tr>
<tr>
<td>== I;</td>
<td>// If not, continue with CONT</td>
</tr>
<tr>
<td>JCN CONT;</td>
<td>// IOAE during access to module B</td>
</tr>
<tr>
<td>SET;</td>
<td></td>
</tr>
<tr>
<td>= IOAE_BIT;</td>
<td>// Set IOAE bit</td>
</tr>
<tr>
<td>CONT: NOP 0;</td>
<td></td>
</tr>
</tbody>
</table>

#### Monitoring times during link-up and update

**Note**

If you have made I/O modules redundant and have taken account of this in your program, you may need to add an overhead to the calculated monitoring times so that no bumps occur at output modules (in HW Config -> Properties CPU -> H Parameter).

An overhead is only required if you operate modules from the following table as redundant modules.

#### For the monitoring times with redundant I/O

<table>
<thead>
<tr>
<th>Module type</th>
<th>Overhead in ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>ET200M: Standard output modules</td>
<td>2</td>
</tr>
<tr>
<td>ET200M: HART output modules</td>
<td>10</td>
</tr>
<tr>
<td>ET200M: F output modules</td>
<td>50</td>
</tr>
<tr>
<td>ET200L–SC with analog outputs</td>
<td>≤ 80</td>
</tr>
<tr>
<td>ET200S with analog outputs or technology modules</td>
<td>≤ 20</td>
</tr>
</tbody>
</table>
Follow the steps below:

- Calculate the overhead from the table. If you use several module types from the table redundantly, apply the largest overhead.
- Add this to all of the monitoring times calculated so far.
13.5 Other options for connecting redundant I/Os
14.1 Communication services

14.1.1 Overview of communication services

Overview

<table>
<thead>
<tr>
<th>Communication service</th>
<th>Functionality</th>
<th>Allocation of S7 connection resources</th>
<th>via MPI</th>
<th>via DP</th>
<th>via PN/IE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG communication</td>
<td>Commissioning, testing, diagnostics</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>OP communication</td>
<td>Operator control and monitoring</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Data exchange via configured connections</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing of PG functions</td>
<td>e.g. testing, diagnostics beyond network boundaries</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PROFIBUS DP</td>
<td>Data exchange between master and slave</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>PROFINET IO</td>
<td>Data exchange between I/O controllers and I/O devices</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>SNMP (Simple Network Management Protocol)</td>
<td>Standard protocol for network diagnostics and parameterization</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Open communication over TCP/IP</td>
<td>Data exchange over Industrial Ethernet with TCP/IP protocol (with loadable FBs)</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Open communication over ISO on TCP</td>
<td>Data exchange over Industrial Ethernet with ISO on TCP protocol (with loadable FBs)</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Open communication over UDP</td>
<td>Data exchange over Industrial Ethernet with UDP protocol (with loadable FBs)</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Data set routing</td>
<td>for example, parameter assignment and diagnostics of field devices on PROFIBUS DP with PDM.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Communication

14.1 Communication services

Note

Communication via the PNIO interface

If you want to use the PNIO interface of the module for communication in plant operation, you must also network this in Step 7 / HW Config / Netpro.

Connection resources in the S7-400 H

S7-400 H components provide a module-specific number of connection resources.

Availability of connection resources

Table 14-2 Availability of connection resources

<table>
<thead>
<tr>
<th>CPU</th>
<th>Total number of connection resources</th>
<th>Can be used for S7-H connections</th>
<th>Reserved from the total number for</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>PG communication</td>
</tr>
<tr>
<td>412-5H PN/DP</td>
<td>48</td>
<td>46</td>
<td>1</td>
</tr>
<tr>
<td>414-5H PN/DP</td>
<td>64</td>
<td>62</td>
<td>1</td>
</tr>
<tr>
<td>416-5H PN/DP</td>
<td>96</td>
<td>62</td>
<td>1</td>
</tr>
<tr>
<td>417-5H PN/DP</td>
<td>120</td>
<td>62</td>
<td>1</td>
</tr>
</tbody>
</table>

Free S7 connections can be used for any of the above communication services.

Note

Communication service via the PROFIBUS DP interface

A fixed default timeout of 40 s is specified for communication services using S7 connection resources. Reliable operation of those communication services at a low baud rate via PROFIBUS DP interface can be ensured in configurations with a Ttr (Target Rotation Time) < 20 s.
14.1.2 PG communication

Properties

Programming device communication is used to exchange data between engineering stations (PG, PC, for example) and SIMATIC modules which are capable of communication. This service is available for MPI, PROFIBUS and Industrial Ethernet subnets. Routing between subnets is also supported.

You can use the programming device communication for the following actions:

- Loading programs and configuration data
- Performing tests
- Evaluating diagnostic information

These functions are integrated in the operating system of SIMATIC S7 modules.

A CPU can maintain several simultaneous online connections to one or multiple programming devices.

14.1.3 OP communication

Properties

OP communication is used to exchange data between HMI stations, such as WinCC, OP, TP and SIMATIC modules which are capable of communication. This service is available for MPI, PROFIBUS and Industrial Ethernet subnets.

You can use the OP communication for operator control, monitoring and alarms. These functions are integrated in the operating system of SIMATIC S7 modules. A CPU can maintain several simultaneous connections to one or several OPs.

14.1.4 S7 communication

Properties

A CPU can always act as a server or client in S7 Communication. A connection is configured permanently. The following connections are possible:

- One-sided configured connections (for PUT/GET only)
- Two-side configured connections (for USEND, URCV, BSEND, BRCV, PUT, GET)

You can use S7 communication via integral interfaces (MPI/DP, PROFIBUS-DP, PROFINET) and, if necessary, via additional communication processors (CP443-1 for Industrial Ethernet, CP443-5 for PROFIBUS).

The S7-400 features integrated S7 communication services that allow the user program in the controller to initiate reading and writing of data. The S7 communication functions are
14.1 Communication services

called via SFBs in the user program. These functions are independent of the specific
network, allowing you to program S7 communication over PROFINET, Industrial Ethernet,
PROFIBUS, or MPI.

S7 communication services provide the following options:

- During system configuration, you configure the connections used by the
  S7 communication. These connections remain configured until you download a new
  configuration.
- You can establish several connections to the same partner. The number of
  communication partners accessible at any time is restricted to the number of connection
  resources available.
- You can configure fault-tolerant S7 connections using the integrated PROFINET
  interface.

---

**Note**

**Downloading the connection configuration in RUN**

When you load a modified connection configuration during operation, connections which
have been set up which are not affected by changes in the connection configuration may
also be aborted.

S7 communication allows you to transfer a block of up to 64 KB per call to the SFB. An S7-
400 transfers a maximum of 4 tags per block call.

---

**SFBs for S7 Communication**

The following SFBs are integrated in the operating system of the S7-400 CPUs:

<table>
<thead>
<tr>
<th>Block</th>
<th>Block name</th>
<th>Brief description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFB 8</td>
<td>USEND</td>
<td>Send data to a remote partner SFB with the type &quot;URCV&quot;</td>
</tr>
<tr>
<td>SFB 9</td>
<td>URCV</td>
<td>Receive asynchronous data from a remote partner SFB with the type &quot;USEND&quot;</td>
</tr>
<tr>
<td>SFB 12</td>
<td>BSEND</td>
<td>Send data to a remote partner SFB with the type &quot;BRCV&quot;</td>
</tr>
<tr>
<td>SFB 13</td>
<td>BRCV</td>
<td>Receive asynchronous data from a remote partner SFB with the type &quot;BSEND&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>With this data transfer, a larger amount of data can be transported between the communication partners than is possible with all other communications SFBs for the configured S7 connections.</td>
</tr>
<tr>
<td>SFB 14</td>
<td>GET</td>
<td>Read data from a remote CPU</td>
</tr>
<tr>
<td>SFB 15</td>
<td>PUT</td>
<td>Write data to a remote CPU</td>
</tr>
<tr>
<td>SFB 16</td>
<td>PRINT</td>
<td>Send data via a CP 441 to a printer</td>
</tr>
<tr>
<td>SFB 19</td>
<td>START</td>
<td>Carry out a reboot (warm restart) or cold restart in a remote station</td>
</tr>
<tr>
<td>SFB 20</td>
<td>STOP</td>
<td>Set a remote station to STOP state</td>
</tr>
<tr>
<td>SFB 21</td>
<td>RESUME</td>
<td>Carry out a hot restart in a remote station</td>
</tr>
<tr>
<td>SFB 22</td>
<td>STATUS</td>
<td>Query the device status of a remote partner</td>
</tr>
<tr>
<td>SFB 23</td>
<td>USSTATUS</td>
<td>Uncoordinated receiving of a remote device status</td>
</tr>
</tbody>
</table>
Integration into STEP 7

S7 communication offers communication functions through configured S7 connections. You use STEP 7 to configure the connections.

S7 connections with an S7-400 are established when the connection data is downloaded.

14.1.5 S7 routing

Properties

You can access your S7 stations beyond subnet boundaries using the programming device / PC. You can use them for the following actions:

- Downloading user programs
- Downloading a hardware configurations
- Performing tests and diagnostics functions

Note

On a CPU used as intelligent slave the S7 routing function is only available if the DP interface is activated. In STEP 7, check the Test, Commissioning, Routing check box in the properties dialog of the DP interface. For more information, refer to the Programming with STEP 7 manual, or directly to the STEP 7 Online Help

Requirements

- The network configuration does not exceed project limits.
- The modules have loaded the configuration data containing the latest "knowledge" of the entire network configuration of the project.

  Reason: All modules connected to the network gateway must receive routing information which defines the paths to other subnets.

- In your network configuration, the PG/PC you want to use to set up a connection via gateway must be assigned to the network to which it is physically connected.
- The CPU must set to master mode, or
- if the CPU is configured as a slave, the "Programming, status/modify or other PG functions" check box must be activated in the properties of the DP interface for the DP slave in STEP 7.
S7 routing gateways: MPI to DP

Gateways between subnets are routed in a SIMATIC station that is equipped with interfaces to the respective subnets. The following figure shows CPU 1 (DP master) acting as router for subnets 1 and 2.

Figure 14-1 S7 routing
S7 routing gateways: MPI - DP - PROFINET

The following figure shows access from MPI to PROFINET via PROFIBUS. CPU 1, for example 416-3, is the router for subnet 1 and 2; CPU 2 is the router for subnet 2 and 3.

![S7 routing gateways: MPI - DP - PROFINET](image)

**Figure 14-2  S7 routing gateways: MPI - DP - PROFINET**

S7 routing: TeleService application example

The following figure shows an application example of the remote maintenance of an S7 station using a PG. The connection to other subnets is set up via modem.

The bottom of the figure shows how this can be configured in STEP 7.
14.1 Communication services

Reference

- You can find additional information on configuring in STEP 7 in the Configuring Hardware and Connections with STEP 7 manual.
- More basic information is available in the Communication with SIMATIC manual.
- For more information about the TeleService adapter, refer to the manual TS-Adapter.
- For additional information about SFCs, refer to the Instructions list.
- For more information, refer to the STEP 7 Online Help, or to the System and Standard Functions manual.
14.1.6 Time synchronization

Introduction

The S7-400 has a powerful timer system. You can synchronize this timer system using a higher-level time generator, which will allow you to synchronize, trace, record, and archive sequences.

Interfaces

Time synchronization is possible via every interface of the S7-400:

- **MPI**
  You can configure the CPU as a time master or a time slave.
- **PROFIBUS DP interface**
  You can configure the CPU as a time master or a time slave.
- **PROFINET interface via Industrial Ethernet**
  Time synchronization using the NTP method; the CPU is the client.
  Time synchronization using the SIMATIC method as master or slave
- **Via the S7-400 backplane bus**
  You can configure the CPU as a time master or a time slave.

CPU as a time master

If you configure the CPU as a time master, you must specify a synchronization interval. You can select any interval between 1 second and 24 hours.

If the CPU time master is on the S7-400 backplane bus, you should select a synchronization interval of 10 seconds.

The time master sends its first message frame once the time has been set for the first time (via SFC 0 "SET_CLK" or PG function). If another interface was configured as a time slave or as an NTP client, the time starts once the first time message frame has been received.

CPU as a time slave

If the CPU is a time slave on the S7-400 backplane bus, then the synchronization is carried out by a central clock connected to the LAN or by another CPU.

You can use a CP to forward the time to the S7-400. To do this, the CP (if it supports direction filtering) must be configured with the "from LAN to station" option in order to forward the time.
**14.1 Communication services**

**Time synchronization via the PROFINET interface**

At the PROFINET interface, time synchronization is possible using the NTP method. The PROFINET CPU is client.

You may configure up to four NTP servers. You can set the update interval between 10 seconds and 1 day. If times exceed an interval of 90 minutes, the PROFINET CPU requests an NTP at cyclic intervals of 90 minutes.

If synchronizing the PROFINET CPU based on the NTP method, you should configure the PROFINET CPU as the time master for the synchronization method in the S7-400. Select a synchronization interval of 10 seconds.

Use FB "LT_BT" or FB "BT_LT" from the STEP 7 standard library to make allowances for a time zone or daylight saving/standard time.

Time synchronization is also possible via Ethernet MMS as master or slave. The combination NTP with SIMATIC method is allowed in this case.

**14.1.7 Data set routing**

**Availability**

S7-400H CPUs as of firmware version 6.0 support data set routing. The CPUs must also be configured in this or a higher firmware version for this.

**Routing and data set routing**

Routing is the transfer of data beyond network boundaries. You can send information from a transmitter to a receiver across several networks.

Data set routing is an expansion of S7 routing and is used, for example, in SIMATIC PDM. The data sent through data record routing include the parameter assignments of the participating communication devices and device-specific information (for example, setpoint values, limit values, etc.). The structure of the destination address for data set routing depends on the data content, in other words, it is determined by the device for which the data is intended.

The field device itself does not need to support data set routing, since these devices do not forward the included information.
Data set routing

The following figure shows the engineering station accessing a variety of field devices. The engineering station is connected to the CPU via Industrial Ethernet in this scenario. The CPU communicates with the field devices via the PROFIBUS.

![Diagram of Data set routing](image)

Figure 14-4 Data set routing

See also

For more information on SIMATIC PDM, refer to the *The Process Device Manager* manual.
14.1.8 SNMP network protocol

Availability

S7-400H CPUs as of firmware version 6.0 support the SNMP network protocol. The CPUs must also be configured in this or a higher firmware version for this.

Properties

SNMP (Simple Network Management Protocol) is the standardized protocol for diagnostics of the Ethernet network infrastructure. In the office setting and in automation engineering, devices from many different manufacturers support SNMP on the Ethernet. SNMP-based applications can be operated on the same network in parallel to applications with PROFINET.

Configuration of the SNMP OPC server is integrated in the STEP 7 Hardware Configuration application. Already configured S7 modules from the STEP 7 project can be transferred directly. As an alternative to STEP 7, you can also perform the configuration with the NCM PC (included on the SIMATIC NET CD). All Ethernet devices can be detected by means of their IP address and/or the SNMP protocol (SNMP V1) and transferred to the configuration.

Use the profile MIB_II_V10.

Applications based on SNMP can be operated on the same network at the same time as applications with PROFINET.

Note

MAC addresses

During SNMP diagnostics, the following MAC addresses are shown for the ifPhysAddress parameter as of FW V5.1:

- Interface 1 (PN interface) = MAC address (specified on the front panel of the CPU)
- Interface 2 (port 1) = MAC address + 1
- Interface 3 (port 2) = MAC address + 2

Diagnostics with SNMP OPC Server in SIMATIC NET

The SNMP OPC server software provides diagnostics and configuration functions for all SNMP devices. The OPC server uses the SNMP protocol to perform data exchange with SNMP devices.

All information can be integrated in OPC-compatible systems, such as the WinCC HMI system. This enables process and network diagnostics to be combined in the HMI system.

Reference

For further information on the SNMP communication service and diagnostics with SNMP, refer to the PROFINET System Description.
14.1.9 Open Communication Via Industrial Ethernet

Availability

S7-400H CPUs with firmware version 6.0 support "open communication over Industrial Ethernet" (in short: open IE communication). The CPUs must also be configured accordingly with this or a higher firmware version.

Functionality

The following services are available for open IE communication:

• Connection-oriented protocols:

  Prior to data transmission connection-oriented protocols establish a logical connection to the communication partner and close this again, if necessary, after transmission is completed. Connection-oriented protocols are used when security is especially important in data transmission. A physical cable can generally accommodate several logical connections. The maximum job length is 32 KB.

  The following connection-oriented protocols are supported for the FBs for open IE communication:
  – TCP to RFC 793
  – ISO on TCP according to RFC 1006

  **Note**

  **ISOonTCP**

  For data communication with third-party systems via RFC1006, the connection partner must adhere to the maximum TPDU size (TPDU = Transfer Protocol Data Unit) negotiated in the ISOonTCP connection establishment.

• Connectionless protocols:

  Connectionless protocols operate without a logical connection. There is also no establishing or terminating a connection to remote partner. Connectionless protocols transfer the data unacknowledged and thus unsecured to the remote partner. The maximum message frame length is 1472 bytes.

  The following connectionless protocols are supported for the FBs for open communication by means of Industrial Ethernet:
  – UDP according to RFC 768

    The single-cast and broadcast modes are supported.
How to use open IE communication

STEP 7 provides the following FBs and UDTs under "Communication Blocks" in the "Standard Library" to allow data to be exchanged with other communication partners:

- **Connection-oriented protocols: TCP/ISO-on-TCP**
  - FB 63 "TSEND" for sending data
  - FB 64 "TRCV" for receiving data
  - FB 65 "TCON", for connection setup
  - FB 66 "TDISCON", for disconnecting
  - UDT 65 "TCON_PAR" with the data structure for the configuration of the connection

- **Connectionless protocol: UDP**
  - FB 67 "TUSEND" for sending data
  - FB 68 "TURCV" for receiving data
  - FB 65 "TCON" for setting up the local communication access point
  - FB 66 "TDISCON" for resolving the local communication access point
  - UDT 65 "TCON_PAR" with the data structure for configuring the local communication access point
  - UDT 66 "TCON_ADR" with the data structure of the addressing parameters of the remote partner

Data blocks for parameterization

- **Data blocks for parameterizing TCP and ISO-on-TCP connections**

  To be able to parameterize your connection at TCP and ISO-on-TCP, you must create a DB that contains the data structure of UDT 65 "TCON_PAR". This data structure contains all parameters you need to set up the connection. Such a data structure which you can group within a global data range is required for every connection.

  Connection parameter CONNECT of FB 65 "TCON" reports the address of the corresponding connection description to the user program (for example, P#DB100.DBX0.0 byte 64).

- **Data blocks for the configuration the local UDP communication access point**

  To assign parameters to the local communication access point, create a DB containing the data structure from the UDT 65 "TCON_PAR". This data structure contains the necessary parameters you need to set up the connection between the user program and the communication layer of the operating system. You also need UDT 66 "TCON_ADDR" for UDP. You can also store this UDT in the DB.

  The CONNECT parameter of the FB 65 "TCON" contains a reference to the address of the corresponding connection description (for example, P#DB100.DBX0.0 Byte 64).
Job lengths and parameters for the different types of connection

Table 14- 4  Job lengths and "local_device_id" parameter

<table>
<thead>
<tr>
<th>Message frame</th>
<th>CPU 41x-5H PN/DP</th>
<th>CPU 41x-5H PN/DP with CP 443-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCP</td>
<td>32 KB</td>
<td>-</td>
</tr>
<tr>
<td>ISO-on-TCP</td>
<td>32 KB</td>
<td>1452 bytes</td>
</tr>
<tr>
<td>UDP</td>
<td>1472 bytes</td>
<td>-</td>
</tr>
</tbody>
</table>

"local_device_id" parameter for the connection description

Dev. ID 16#5 for CPU 0 16#10 for CPU1

Establishing a communication connection

- Use with TCP and ISO-on-TCP
  Both communication partners call FB 65 "TCON" to establish the connection. In the configuration, you specify which communication partner activates the connection, and which one responds to the request with a passive connection. To determine the number of possible connections, refer to your CPU's technical specifications.

  The CPU automatically monitors and holds the active connection.

  If the connection is broken, for example by line interruption or by the remote communication partner, the active partner tries to reestablish the connection. You do not have to call FB 65 "TCON" again.

  FB 66 "TDISCON" disconnects the CPU from a communication partner, as does STOP mode. To reestablish the connection to have to call FB65 "TCON" again.

- Use with UDP
  Both communication partners call FB 65 "TCON" to set up their local communication access point. This establishes a connection between the user program and operating system's communication layer. No connection is established to the remote partner.

  The local access point is used to send and receive UDP message frames.

Disconnecting a communication connection

- Use with TCP and ISO-on-TCP
  FB 66 "TDISCON" disconnects the communication connection between the CPU and a communication partner.

- Use with UDP
  FB 66 "TDISCON" disconnects the local communication access point, i.e., the interconnection between the user program and the communication layer of the operating system is terminated.
### 14.2 Basics and terminology of fault-tolerant communication

#### Options for closing the communication connection

The following events cause the communication connection to be closed:

- Program cancellation of the communication connection with FB 66 "TDISCON".
- The CPU state changes from RUN to STOP.
- At POWER OFF / POWER ON

#### Connection diagnostics

In Step7, you can read detailed information on the configured connections by selecting "Module state -> Communication -> Open communication over Industrial Ethernet".

#### Reference

For detailed information on the blocks described above, refer to the *STEP 7 Online Help*.

#### 14.2 Basics and terminology of fault-tolerant communication

**Overview**

Increased demands on the availability of an overall system require increased reliability of the communication systems, which means implementing redundant communication.

Below you will find an overview of the fundamentals and basic concepts which you ought to know with regard to using fault-tolerant communications.

**Redundant communication system**

The availability of the communication system can be enhanced by duplicating component units and all bus components, or by using a fiber-optic ring.

On failure of a component, the various monitoring and synchronization mechanisms ensure that the communication functions are taken over by the reserve components during operation.

A redundant communication system is essential if you want to use fault-tolerant S7 connections.

**Fault-tolerant communication**

Fault-tolerant communication is the deployment of S7 communication SFBs over fault-tolerant S7 connections.

Fault-tolerant S7 connections need a redundant communication system.
Redundancy nodes

Redundancy nodes represent extreme reliability of communication between two fault-tolerant systems. A system with multi-channel components is represented by redundancy nodes. Redundancy nodes are independent when the failure of a component within the node does not result in any reliability impairment in other nodes.

Even with fault-tolerant communication, only single errors/faults can be tolerated. If more than one error occurs between communication endpoints, communication can no longer be guaranteed.

Connection (S7 connection)

A connection represents the logical assignment of two communication peers for executing a communication service. Every connection has two end points containing the information required for addressing the communication peer as well as other attributes for establishing the connection.

An S7 connection is the communication link between two standard CPUs or from a standard CPU to a CPU in a fault-tolerant system.

In contrast to a fault-tolerant S7 connection, which contains at least two partial connections, an S7 connection actually consists of just one connection. If that connection fails, communication is terminated.

![S7 connection diagram](image)

Figure 14-5 Example of an S7 connection

Note

Generally speaking, "connection" in this manual means a "configured S7 connection". For other types of connection, please refer to the SIMATIC NET NCM S7 for PROFIBUS and SIMATIC NET NCM S7 for Industrial Ethernet manuals.

Fault-tolerant S7 connections

The requirement for higher availability with communication components (for example CPs and buses) means that redundant communication connections are necessary between the systems involved.

Unlike an S7 connection, a fault-tolerant S7 connection consists of at least two underlying subconnections. From the user program, configuration and connection diagnostics perspective, the fault-tolerant S7 connection with its underlying subconnections is represented by exactly one ID (just like a standard S7 connection). Depending on the configuration, it can consist of up to four subconnections, of which two are always established (active) to maintain communication in the event of an error. The number of subconnections depends on the possible alternative paths (see figure below) and is
determined automatically. Within an S7-H connection, only subconnections over CP or over the integrated CPU interface are used in the configuration.

The following examples and the possible configurations in STEP 7 are based on a maximum of two subnets and a maximum of 4 CPs in the redundant fault-tolerant system. Configurations with a higher number of CPs or networks are not supported in STEP 7.

**Figure 14-6**  Example that shows that the number of resulting partial connections depends on the configuration
If the active subconnection fails, the already established second subconnection automatically takes over communication.

**Resource requirements of fault-tolerant S7 connections**

The fault-tolerant CPU supports operation of 62/46 (see the technical specifications) fault-tolerant S7 connections. Each connection needs a connection resource on the CPU; subconnections do not need any additional connection resources. On the CP, on the other hand, each subconnection needs a connection resource.

**Note**

If you have configured several fault-tolerant S7 connections for a fault-tolerant station, establishing them may take a considerable time. If the configured maximum communication delay is set too short, link-up and updating is canceled and the redundant system mode is no longer reached (see section [Time monitoring](Page 149)).

Each CPU provides the connection resources according to its configuration, which means that a CPU 417-5H that was configured as CPU 412-5H only provides the connection resources of a CPU 412-5H.

### 14.3 Usable networks

Your choice of the physical transmission medium depends on the required expansion, targeted fault tolerance, and transfer rate. The following bus systems are used for communication with fault-tolerant systems:

- Industrial Ethernet
- PROFIBUS

Additional information on the networks that can be used is available in the relevant SIMATIC NET documentation on PROFIBUS and Ethernet.
14.4 Usable communication services

The following services can be used:

- S7 communication via fault-tolerant S7 connections:
  - via PROFIBUS
  - Industrial Ethernet (ISO)
    S7 fault-tolerant connections are only possible between SIMATIC-S7-400H stations, or SIMATIC S7-400 stations with CPU41x-5H.
    Fault-tolerant communication with PC stations is only possible over Industrial Ethernet with ISO protocol and with ISO-on-TCP as of version 8.1.2.
  - Via integrated PROFINET interface (ISOonTCP).

- Open communication via Industrial Ethernet
- S7 communication using S7 connections via MPI, PROFIBUS, and Industrial Ethernet
- Standard communication (e.g. FMS) via PROFIBUS
- S5-compatible communication (e.g. SEND and RECEIVE blocks) via PROFIBUS and Industrial Ethernet

The following are not supported:

- S7 basic communication
- Global data communication
- PROFINET CBA

14.5 Communication via S7 connections

Communication with standard systems

Fault-tolerant communication between fault-tolerant and standard systems is not supported. The following examples illustrate the actual availability of the communicating systems.

Configuration

S7 connections are configured in STEP 7.

Programming

All communication functions are supported for S7 communication on a fault-tolerant system. The communication SFBs are used in STEP 7 to program communication.
Note

The START and STOP communication functions act on exactly one CPU or on all CPUs of the fault-tolerant system (for more details refer to the System Software for S7-300/400, System and Standard Functions Reference Manual).

Note

Downloading the connection configuration in RUN
If you download a connection configuration during operation, any established connections could be canceled.
14.5 Communication via S7 connections

14.5.1 Communication via S7 connections - one-sided mode

Availability

Availability is also enhanced by using a redundant plant bus instead of a simple bus (see image below) for communication between a fault-tolerant system and a standard system.

![Diagram showing communication between fault-tolerant and standard systems via S7 connections.](image)

Figure 14-7 Example of linking standard and fault-tolerant systems in a simple bus system

With this configuration and redundant operation, the fault-tolerant system is connected via bus1 with the standard system. This applies no matter which CPU is the master CPU.

For linked fault-tolerant and standard systems, the availability of communication cannot be improved by means of a dual electrical bus system. To be able to use the second bus system as redundancy, a second S7 connection must be used and managed accordingly in the user program (see next figure).
On a plant bus configured as duplex fiber-optic ring, communication between the partner systems is maintained if the duplex fiber-optic cable breaks. The systems then communicate as if they were connected to a bus system (linear structure); see following figure.

Figure 14-9 Example of linking of standard and fault-tolerant systems in a redundant ring
Response to failure

Duplex fiber-optic ring and bus system

Because S7 connections are used here (the connection ends at the CPU of the subsystem, in this case CPUa1), an error in the fault-tolerant system (e.g. CPUa1 or CPa1) or in system b (e.g. CP b) results in total failure of communication between the participating systems (see previous figures).

There are no bus system-specific differences in the response to failure.

Linking standard and fault-tolerant systems

Driver block "S7H4_BSR": You can link a fault-tolerant system to an S7-400 / S7-300 using the "S7H4_BSR" driver block. For more information, contact Siemens by e-mail: function.blocks.industry @siemens.com

Alternative: SFB 15 "PUT" and SFB 14 "GET" in the fault-tolerant system: As an alternative, use two SFB 15 "PUT" blocks over two standard connections. First call the first block. If there was no error message when the block executed, the transfer is assumed to have been successful. If there was an error message, the data transfer is repeated via the second block. If a connection cancelation is detected later, the data is also transferred again to exclude possible information losses. You can use the same method with an SFB 14 "GET".

If possible, use the mechanisms of S7 communication for communication.
14.5.2 Communication via redundant S7 connections

**Availability**

Availability can be enhanced by using a redundant plant bus and two separate CPs in a standard system.

Redundant communication can also be operated with standard connections. For this two separate S7 connections must be configured in the program in order to implement connection redundancy. In the user program, both connections require the implementation of monitoring functions in order to allow the detection of failures and to change over to the standby connection.

The following figure shows such a configuration.

![Fault-tolerant and Standard System Diagram](image)

**Response to failure**

Double errors in the fault-tolerant system (i.e. CPUa1 and CPa2) or in the standard system (CPb1 and CPb2), and single errors in the standard system (CPUb1) lead to a total failure of communication between the systems involved (see previous figure).
14.5 Communication via S7 connections

14.5.3 Communication via point-to-point CP on the ET 200M

Connection via ET 200M

Links from fault-tolerant systems to single-channel systems are often possible only by way of point-to-point connections, as many systems offer no other connection options.

In order to make the data of a single-channel system available to CPUs of the fault-tolerant system as well, the point-to-point CP (CP 341) must be installed in a distributed rack along with two IM 153-2 modules.

Configuring connections

Redundant connections between the point-to-point CP and the fault-tolerant system are not necessary.

Figure 14-11 Example of connecting a fault-tolerant system to a single-channel third-party system using switched PROFIBUS DP
Response to failure

Double errors in the fault-tolerant system (i.e. CPUa1 and IM153) and single errors in the third-party system lead to a total failure of communication between the systems involved (see previous figure).

The point-to-point CP can also be inserted centrally in "Fault-tolerant system a". However, in this configuration even the failure of the CPU, for example, will cause a total failure of communication.

14.5.4 Custom connection to single-channel systems

Connection via PC as gateway

Fault-tolerant systems and single-channel systems can also be via a gateway (no connection redundancy). The gateway is connected to the system bus by one or two CPs, depending on availability requirements. Fault-tolerant connections can be configured between the gateway and the fault-tolerant systems. The gateway allows you to link any kinds of single-channel system (e.g. TCP/IP with a manufacturer-specific protocol).

A user-programmed software instance in the gateway implements the single-channel transition to the fault-tolerant systems, and so allows any single-channel systems to be linked to a fault-tolerant system.

Configuring connections

Redundant connections between the gateway CP and the single-channel system are not required.
The gateway CP is located on a PC system which has fault-tolerant connections to the fault-tolerant system.

To configure fault-tolerant S7 connections between fault-tolerant system A and the gateway, you first need to install S7-REDCONNECT on the gateway. The functions for preparing data for their transfer via the single-channel link must be implemented in the user program.

For additional information, refer to the “Industrial Communications IK10” Catalog.

Availability of communicating systems

Fault-tolerant communication expands the overall SIMATIC system by additional, redundant communication components such as CPs and bus cables. To illustrate the actual availability of communicating systems when using an optical or electrical network, a description is given below of the possibilities for communication redundancy.

Requirement

The essential requirement for the configuration of fault-tolerant connections with STEP 7 is a configured hardware installation.

The hardware configuration in both subsystems of a fault-tolerant system must be identical. This applies in particular to the slots.

Depending on the network used, CPs can be used for fault-tolerant and fail-safe communication, see Appendix Function modules and communication processors supported by the S7-400H (Page 429).
Only Industrial Ethernet with the ISO protocol or PROFIBUS without distributed I/O and ISO-on-TCP as of version 6.0 is supported. Fault-tolerant S7 connections via Industrial Ethernet with ISO-on-TCP are supported by the integrated PN interface and corresponding CPs. You require a suitable CP for fault-tolerant S7 connections via Industrial Ethernet with ISO protocol or via PROFIBUS. These connections are not possible via the internal PROFIBUS-DP interface.

Only Industrial Ethernet is supported for connecting to PC stations using fault-tolerant S7 connections. To be able to use fault-tolerant S7 connections between a fault-tolerant system and a PC, you must install the "S7-REDCONNECT" software package on the PC. The software is part of the SIMATIC Net CD. Communication via ISO-on-TCP is also supported as of version 8.1.2. Please refer to the product information on the SIMATIC NET PC software to learn more about the CPs you can use at the PC end.

**Communication combinations**

The following table shows the possible combinations of fault-tolerant connections via Industrial Ethernet.

<table>
<thead>
<tr>
<th>Local connectio n end point</th>
<th>Local network connection</th>
<th>Used network protocol</th>
<th>Remote network connection</th>
<th>Remote connection end point</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU 41xH V6</td>
<td>CPU-PN interface CP443-1 (EX11/20)</td>
<td>TCP</td>
<td>CPU-PN interface CP443-1 (EX11/20)</td>
<td>TCP CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td>CP443-1 (X11/20)</td>
<td>TCP</td>
<td>CPU-PN interface CP443-1 (X11/20)</td>
<td>TCP CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCP</td>
<td>CPU-PN interface CP443-1 (X11/20)</td>
<td>TCP CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCP</td>
<td>CPU-PN interface CP443-1 (X11/20)</td>
<td>TCP CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td>PC1623 as of V8.1.2</td>
<td>TCP</td>
<td>CPU-PN interface CP443-1 (EX11/20)</td>
<td>TCP CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCP</td>
<td>CPU-PN interface CP443-1 (EX11/20)</td>
<td>TCP CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td>PC station with Simatic Net CD</td>
<td>PC1623 as of V8.1.2</td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td>PC station with Simatic Net CD</td>
<td>PC1623 up to V7.x</td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISO</td>
<td>CP443-1 (EX11/20)</td>
<td>ISO CPU 41xH V6 S7 fault tolerant connection via ISO-onTCP</td>
</tr>
</tbody>
</table>
**Configuration**

The availability of the system, including the communication, is set during configuration. Refer to the STEP 7 documentation to find out how to configure connections.

Only S7 communication is used for fault-tolerant S7 connections. To set this up, open the "New Connection" dialog box, then select "S7 Connection Fault-Tolerant" as the type.

The number of required redundant subconnections is determined by STEP 7 as a function of the redundancy nodes. Up to four redundant connections can be generated, if supported by the network. Higher redundancy cannot be achieved even by using more CPs.

In the "Properties - Connection" dialog box you can also modify specific properties of a fault-tolerant connection if necessary. When using more than one CP, you can also route the connections in this dialog box. This may be practical, because by default all connections are routed initially through the first CP. If all the connections are busy there, any further connections are routed via the second CP, etc.

You have to extend the monitoring time of the connection when you use long synchronization cables.

Example: If you are operating 5 fault-tolerant S7 connections with a monitoring time of 500 ms and short synchronization cables (up to 10m) and want to convert to long synchronization cables (10km), you must increase the monitoring time to 1000 ms.

To ensure CIR capability of the fault tolerant system, activate the option "Save connections prior to loading" in Step7 Netpro.

**Programming**

Fault-tolerant communication can be implemented on the fault-tolerant CPU and is implemented by means of S7 communication.

This is possible only within an S7 project/multiproject.

Fault-tolerant communication is programmed in STEP 7 by means of communication SFBs. Those blocks can be used to transfer data on subnets (Industrial Ethernet, PROFIBUS). The standard communication SFBs integrated into the operating system offer you the option of acknowledged data transfer. In addition to data transfer, you can also use other communication functions for controlling and monitoring the communication peer.

User programs written for S7 connections can also be run for fault-tolerant S7 connections without program modification. Cable and connection redundancy has no effect on the user program.
14.6 Communication via fault-tolerant S7 connections

Note

For information on programming the communication, refer to the STEP 7 documentation (e.g. Programming with STEP 7).

The START and STOP communication functions act on exactly one CPU or on all CPUs of the fault-tolerant system (for more details refer to the System Software for S7-300/400, System and Standard Functions Reference Manual).

Any disruption of subconnections while communication jobs are active over fault-tolerant S7 connections leads to extended delay times.

Note

Downloading the connection configuration in RUN

If you download a connection configuration during operation, any established connections could be canceled.

14.6.1 Communication between fault-tolerant systems

Availability

The easiest way to enhance availability between linked systems is to implement a redundant plant bus, using a duplex fiber-optic ring or a dual electrical bus system. The connected nodes may consist of simple standard components.

Availability can best be enhanced using a duplex fiber-optic ring. If the one of the multimode fiber-optic cables breaks, communication between the systems involved is maintained. The systems then communicate as if they were connected to a bus system (line). A ring topology basically contains two redundant components and automatically forms a 1-out-of-2 redundancy node. A fiber-optic network can be set up as a line or star topology. However, the line topology does not permit cable redundancy.

If one electrical cable segment fails, communication between the participating systems is also upheld (1-out-of-2 redundancy).

The examples below illustrate the differences between the two variants.

Note

The number of connection resources required on the CPs depends on the network used.

If you implement a duplex fiber-optic ring (see figure below), two connection resources are required per CP. In contrast, only one connection resource is required per CP if a double electrical network (see figure after next) is used.
14.6 Communication via fault-tolerant S7 connections

Figure 14-14 Example of redundancy with fault-tolerant system and redundant ring

Configuration view ≠ Physical view

Figure 14-15 Example of redundancy with fault-tolerant system and redundant bus system

Configuration view = Physical view
14.6 Communication via fault-tolerant S7 connections

You decide during configuration if the additional CPs are used to increase resources or availability. This configuration is typically used to increase availability.

Note

**Internal and external interface**

Communication between fault-tolerant systems may only take place between internal interfaces or external interfaces (CP). Communication between internal interface and CP is not possible.

**Response to failure**

If a duplex fiber-optic ring is used, only a double error within a fault-tolerant system (e.g. CPUa1 and CPA2 in one system) leads to total failure of communication between the systems involved (see first figure).

If a double error (e.g. CPUa1 and CPb2) occurs in the first case of a redundant electrical bus system (see second figure), this results in a total failure of communication between the systems involved.

In the case of a redundant electrical bus system with CP redundancy (see third figure), only a double error within a fault-tolerant system (e.g. CPUa1 and CPUa2) or a triple error (e.g. CPUa1, CPA22, and bus2) will result in a total failure of communication between the systems involved.
Fault-tolerant S7 connections

Any disruption of subconnections while communication jobs are active over fault-tolerant S7 connections leads to extended delay times.

14.6.2 Communication between fault-tolerant systems and a fault-tolerant CPU

Availability

Availability can be enhanced by using a redundant plant bus and by using a fault-tolerant CPU in a standard system.

If the communication peer is a fault-tolerant CPU, redundant connections can also be configured, in contrast to systems with a standard CPU.

Note

Fault-tolerant connections use two connection resources on CP b1 for the redundant connections. One connection resource each is occupied on CP a1 and CP a2 respectively. In this case, the use of further CPs in the standard system only serves to increase the resources.

Response to failure

Double errors in the fault-tolerant system (i.e. CPUa1 and CPa2) or single errors in a standard system (CPUb1) lead to a total failure of communication between the systems involved; see previous figure.
14.6 Communication via fault-tolerant S7 connections

14.6.3 Communication between fault-tolerant systems and PCs

Availability

PCs are not fault-tolerant due to their hardware and software characteristics. They can be arranged redundantly within a system, however. The availability of such a PC (OS) system and its data management is ensured by means of suitable software such as WinCC Redundancy.

Communication takes place via fault-tolerant S7 connections.

The "S7-REDCONNECT" software package is required for fault-tolerant communication on a PC. S7-REDCONNECT is used to connect a PC to a redundant bus system using one or two CPs. The second CP is merely used to redundantly connect the PC to the bus system and does not increase the availability of the PC. Always use the latest version of this software.

Only Industrial Ethernet is supported for connecting PC systems. The SIMATIC Net software V 8.1.2 is required for connection via ISOonTCP. This corresponds to the configuration TCP/RFC1006 at the PC end.

Note

The PROFINET MRP (Media Redundancy Protocol) for PROFINET ring topologies is not supported by SIMATIC NET PC modules. System buses as optical two-fiber ring cannot be operated with MRP.

Configuring connections

The PC must be engineered and configured as a SIMATIC PC station. Additional configuration of fault-tolerant communication is not necessary at the PC end. The connection configuration is uploaded from the STEP 7 project to the PC station.

You can find out how to use STEP 7 to integrate fault-tolerant S7 communication for a PC into your OS system in the WinCC documentation.
14.6 Communication via fault-tolerant S7 connections

Response to failure

Double errors in the fault-tolerant system, e.g., CPUa1 and CPA2, or failure of the PC result in a total failure of communication between the systems involved; see previous figures.
PC/PG as Engineering System (ES)

To be able to use a PC as Engineering System, you need to configure it under its name as a PC station in HW Config. The ES is assigned to a CPU and is capable of executing STEP 7 functions on that CPU.

If this CPU fails, communication between the ES and the fault-tolerant system is no longer possible.

14.7 Communication performance

Compared to a fault-tolerant CPU in stand-alone mode or standard CPU, the communication performance (response time or data throughput) of a fault-tolerant system operating in redundant mode is significantly lower.

The aim of this description is to provide you with criteria which allow you to assess the effects of the various communication mechanisms on communication performance.

You get information on the latest connection statistics of all CPU connections in the "Connection statistics" tab of the "Module state" tab dialog.

Definition of communication load

Communication load is the sum of requests per second issued to the CPU by the communication mechanisms, plus the requests and messages issued by the CPU.

Higher communication load increases the response time of the CPU, meaning the CPU takes more time to respond to a request (such as a read job) or to output requests and messages.

Operating range

In every automation system there is a linear operating range in which an increase in communication load will also lead to an increase in data throughput. This then results in reasonable response times which are acceptable for the automation task at hand.

A further increase in communication load will push data throughput into the saturation range. Under certain conditions, the automation system therefore may no longer be capable of processing the request volume within the response time demanded. Data throughput reaches its maximum, and the reaction time rises exponentially; see the figures below.

Data throughput may even be reduced somewhat due to additional internal loads inside the device.
14.7 Communication performance

**Standard and fault-tolerant systems**

The information above applies to standard and fault-tolerant systems. Since communication performance in standard systems is clearly higher than that of redundant, fault-tolerant systems, the saturation point is rarely reached in today's plants.

In contrast, fault-tolerant systems require synchronization to maintain synchronous operation. This increases block execution times and reduces communication performance. This means that performance limits are reached earlier. If the redundant, fault-tolerant system is not operating at its performance limits, the performance benchmark compared to the single mode will be lower by the factor 2 to 3.

**Communication statistics**

You can determine the distribution of the communication load across all connections of a CPU or the redundant fault tolerant system via STEP 7 "Module state -> Communication statistics".
Which variables influence communication load?

The communication load is affected by the following variables:

- Number of connections/connected HMI systems
- Number of tags, or number of tags in screens displayed on OPs or using WinCC.
- Communication type (HMI, S7 communication, S7 message functions, S5-compatible communication, open communication via Industrial Ethernet...)
- The configured maximum cycle time extension as a result of communication load
- The length of the fiber-optic cables of the synchronization connection.

Data throughput drops by about 5% for each kilometer of cable length.
14.8 General issues regarding communication

Reduce the rate of communication jobs per second as far as possible. Utilize the maximum user data length for communication jobs, for example by grouping several tags or data areas in one read job.

Each request requires a certain processing time, and its status should therefore not be checked before this process is completed.

You can download a tool for the assessment of processing times free of charge from the Internet at:


Your calls of communication jobs should allow the event-driven transfer of data. Check the data transfer event only until the job is completed.

Call the communication blocks sequentially and stepped down within the cycle in order to obtain a balanced distribution of communication load.

You can by-pass the block call command by means of a conditional jump if you do not want to transfer any user data.

A significant increase in communication performance between S7 components is achieved by using S7 communication functions, rather than S5-compatible communication functions.

As S5-compatible communication functions (FB "AG_SEND", FB "AG_RECV", AP_RED) generate a significantly higher communication load, you should only deploy these for the communication of S7 components with non-S7 components.

AP_RED software package

When using the "AP_RED" software package, limit the user data length to 240 bytes. If larger data volumes are necessary, transfer those by means of sequential block calls.

The "AP_RED" software package uses the mechanisms of FB "AG_SEND" and FB "AG_RECV". Use AP_RED only to link SIMATIC S5/S5-H controllers or third-party devices which only support S5-compatible communication.

S7 communication (SFB 12 "BSEND" and SFB 13 "BRCV")

Do not call SFB 12 "BSEND" in the user program more often than the associated SFB 13 "BRCV" at the communication peer.

S7 communication (SFB 8 "USEND" and SFB 9 "URCV")

SFB 8 "USEND" should always be event-driven, because this block may generate a high communication load.

Do not call SFB 8 "USEND" in the user program more often than the associated SFB 9 "URCV" at the communication peer.
**SIMATIC OPs, SIMATIC MPs**

Do not install more than 4 OPs or 4 MPs in a fault-tolerant system. If you do need more OPs/MPs, your automation task may have to be revised. Contact your SIMATIC sales partner for support.

Do not select a screen refresh cycle time of less than 1 s, and increase it to 2 s as required.

Verify that all screen tags are requested within the same cycle time in order to form an optimized group for read jobs.

**OPC servers**

When OPC is used to connect several HMI devices for your visualization tasks to a fault-tolerant system, you should keep the number of OPC servers accessing the fault-tolerant system as low as possible. OPC clients should address a shared OPC server, which then fetches the data from the fault-tolerant system.

You can optimize data exchange by using WinCC and its client/server concept.

Various HMI devices of third-party vendors support the S7 communication protocol. You should utilize this option.
This section provides an overview of fundamental issues you must observe when you configure a fault-tolerant system.

The second section covers the PG functions in STEP 7.

For detailed information, refer to Configuring fault-tolerant systems in the basic help.

15.1 Configuring with STEP 7

The basic approach to configuring the S7-400H is no different from that used to configure the S7-400.

- Creating projects and stations
- Configuring hardware and networking
- Loading system data onto the target system

Even the individual steps that are required for this are identical for the most part to those familiar from the S7-400.

Note

OBs required

Always download these error OBs to the S7-400H CPU: OB 70, OB 72, OB 80, OB 82, OB 83, OB 85, OB 86, OB 87, OB 88, OB 121 and OB 122. If you do not download these OBs, the fault-tolerant system goes into STOP when an error occurs.

Creating a fault-tolerant station

The SIMATIC fault-tolerant station represents a separate station type in SIMATIC Manager. It allows the configuration of two central units, each having a CPU and therefore a redundant station configuration.

15.1.1 Rules for arranging fault-tolerant station components

The following rules have to be complied with for a fault-tolerant station, in addition to the rules that generally apply to the arrangement of modules in the S7-400:

- Insert the CPUs into the same slots.
- Redundantly used external DP master interfaces or communication modules must be inserted in the same slots in each case.
- Insert an external DP master interface for redundant DP master systems only into the CPUs and not into the expansion devices.
- Redundantly used CPUs (e.g. CPU 41x-5H PN/DP) must be identical, i.e. they must have the same order number, the same product version and firmware version. It is not the marking on the front side is decisive for the product version, but the revision of the "Hardware" component ("Module status" dialog mask) to be read using step 7.
- Redundantly used modules (e.g. DP slave interface module IM 153-2) must be identical, i.e. they must have the same order number, the same product version and - if available - the same firmware version.

**Layout rules**

- A fault-tolerant station may contain up to 20 expansion devices.
- Assign module racks with even numbers only to central rack 0, and racks with odd numbers only to central rack 1.
- Modules with communication bus interface can be operated only in racks 0 through 6.
- Communication-bus capable modules are not permissible in switched I/O.
- Pay attention to the rack numbers for operation of CPs for fault-tolerant communication in expansion devices:
  - The numbers must be directly sequential and begin with the even number, e.g. rack numbers 2 and 3, but not rack numbers 3 and 4.
- A rack number is also assigned for DP master no. 9 onwards if the central rack contains DP master modules. The number of possible expansion racks is reduced as a result.

Compliance with the rules is monitored automatically by STEP 7 and considered accordingly during configuration.

### 15.1.2 Configuring hardware

The simplest way of achieving a redundant hardware configuration consists in initially equipping one rack with all the redundant components, assigning parameters to them and then copying them.

You can then specify the various addresses (for one-sided I/O only!) and arrange other, non-redundant modules in individual racks.

**Special features in presenting the hardware configuration**

In order to enable quick recognition of a redundant DP master system, it is represented by two parallel DP cables.
15.1.3 Assigning parameters to modules in a fault-tolerant station

Introduction
Assigning parameters to modules in a fault-tolerant station is no different from assigning parameters to modules in S7-400 standard stations.

Procedure
All parameters of the redundant components (with the exception of MPI and communication addresses) must be identical.

The special case of CPUs
You can only set the CPU0 parameters (CPU on rack 0). Any values that you specify are automatically allocated to CPU1 (CPU on rack 1). You can set the following values for CPU1:

- Parameters of the MPI/DP interface (X1)
- Parameters of the DP interface (X2)
- Addresses of sync modules
- Parameters of the PROFINET interface

Configuring modules addressed in the I/O address space
Always configure a module that is addressed in the I/O address space so that it is located either entirely in the process image or entirely outside. Otherwise, consistency cannot be guaranteed, and the data may be corrupted.

I/O access using word or double word operations
The system loads the values to accumulator "0" if the word or double word for I/O access contains only the first or the first three bytes, but not the remaining bytes of the addressed space.

Example: The I/O with address 8 and 9 is available in the S7-400H; addresses 10 and 11 are not used. Access L ID 8 causes the system to load the value DW#16#00000000 into the accumulator.
15.1.4 Recommendations for setting the CPU parameters

CPU parameters that determine cyclic behavior

You specify the CPU parameters that determine the cyclic behavior of the system on the "Cycle/Clock memory" tab.

Recommended settings:
- As long a scan cycle monitoring time as possible (e.g. 6000 ms)
- OB 85 call when there is an I/O area access error: only with incoming and outgoing errors

Number of messages in the diagnostic buffer

You specify the number of messages in the diagnostic buffer on the "Diagnostics/Clock" tab. We recommend that you set a large number (3200, for example).

Monitoring time for transferring parameters to modules

You specify this monitoring time on the "Startup" tab. It depends on the configuration of the fault-tolerant station. If the monitoring time is too short, the CPU enters the W#16#6547 event in the diagnostic buffer.

For some slaves (e.g. IM 157) these parameters are packed in system data blocks. The transmission time of the parameters depends on the following factors:
- Baud rate of the bus system (high baud rate => short transmission time)
- Size of the parameters and the system data blocks (long parameter => long transmission time)
- Load on the bus system (many slaves => long transmission time);
  **Note:** The bus load is at its peak during restart of the DP master, for example, following Power OFF/ON

Recommended setting: 600 corresponds to 60 s.

**Note**

The specific fault-tolerant CPU parameters, and thus also the monitoring times, are calculated automatically. The work memory allocation of all data blocks is based on a CPU-specific default value. If your fault-tolerant system does not link up, check the data memory allocation (HW Config > CPU Properties > H Parameters > Work memory used for all data blocks).

**Note**

A CP 443-5 Extended (order number 6GK7443–5DX03) may only be used for transfer rates of up to 1.5 Mbaud in an S7–400H or S7–400FH when a DP/PA or Y link is connected (IM157, order number 6ES7157-0AA00-0XA0, 6ES7157-0AA80-0XA0, 6ES7157-0AA81-0XA0). Remedy: see FAQ 11168943 in Service & Support [http://www.siemens.com/automation/service&support]
15.1.5 Networking configuration

The fault-tolerant S7 connection is a separate connection type of the "Configure Networks" application. It permits that the following communication peers can communicate with each other:

- S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)->S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)
- S7–400 station (with 1 fault-tolerant CPU)->S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)
- S7–400 station (with 1 fault-tolerant CPU)->S7–400 station (with 1 fault-tolerant CPU)
- SIMATIC PC stations > S7–400 fault-tolerant station (with 2 fault-tolerant CPUs)

When this connection type is configured, the application automatically determines the number of possible connecting paths:

- If two independent but identical subnets are available and they are suitable for an S7 connection (DP master systems), two connecting paths are used. In practice, they are usually electrical power systems, one CP in each subnet:

- If only one DP master system is available (in practice usually fiber-optic cables), four connecting paths are used for a connection between two fault-tolerant stations. All CPs are in this subnet:

Downloading the network configuration into a fault-tolerant station

The complete network configuration can be downloaded into the fault-tolerant station in one operation. The same requirements that apply for downloads into standard stations must be met.
15.2 Programming device functions in STEP 7

Display in SIMATIC Manager

In order to do justice to the special features of a fault-tolerant station, the way in which the system is visualized and edited in SIMATIC Manager differs from that of a S7-400 standard station as follows:

- In the offline view, the S7 program appears only under CPU0 of the fault-tolerant station. No S7 program is visible under CPU1.
- In the online view, the S7 program appears under both CPUs and can be selected in both locations.

Communication functions

For programming device (PG) functions that establish online connections (e.g. downloading and deleting blocks), one of the two CPUs has to be selected even if the function affects the entire system over the redundant link.

- Data which is modified in one of the central processing units in redundant operation affect the other CPUs over the redundant link.
- Data which is modified when there is no redundant link (i.e. in single mode) initially affects only the processed CPU. The blocks are applied by the master CPU to the reserve CPU during the next link-up and update. Exception: No new blocks are applied after changing the configuration. Loading the blocks is then the responsibility of the user.
16.1 Failure and replacement of components during operation

One factor that is crucial to the uninterrupted operation of the fault-tolerant controller is the replacement of failed components during operation. Quick repairs will recover fault-tolerant redundancy.

We will show you in the following sections how simple and fast it can be to repair and replace components in the S7-400H. Also refer to the tips in the corresponding sections of the manual *S7-400 Automation Systems, Installation*.

16.2 Failure and replacement of components during operation

Which components can be replaced?

The following components can be replaced during operation:

- Central processing units (e.g. CPU 417–5H)
- Power supply modules (e.g. PS 405, PS 407)
- Signal and function modules
- Communication processors
- Synchronization modules and fiber-optic cables
- Interface modules (e.g. IM 460, IM 461)

16.2.1 Failure and replacement of a CPU

Complete replacement of the CPU is not always necessary. If only the load memory fails, it is enough to replace the corresponding memory card. Both cases are described below.

**Starting situation for replacement of the CPU**

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
</table>
| The S7-400H is in redundant system mode and a CPU fails. | • The partner CPU switches to single mode.  
• The partner CPU reports the event in the diagnostic buffer and in OB 72. |
Requirements for replacement

The module replacement described below is possible only if the "new" CPU

- has the same operating system version as the failed CPU and
- if it is equipped with the same load memory as the failed CPU.

Note

New CPUs are always shipped with the latest operating system version. If this differs from the version of the operating system of the remaining CPU, you will have to equip the new CPU with the same version of the operating system. Either create an operating system update card for the new CPU and use this to load the operating system on the CPU or load the required operating system in HW Config with "PLC -> Update Firmware", see section Updating the firmware without a memory card (Page 77).

Procedure

Follow the steps below to replace a CPU:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Turn off the power supply module.</td>
<td>• The entire subsystem is switched off (system operates in single mode).</td>
</tr>
<tr>
<td>2</td>
<td>Replace the CPU. Make sure the rack number is set correctly on the CPU.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Insert the synchronization modules.</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>Plug in the fiber-optic cable connections of the synchronization modules.</td>
<td>–</td>
</tr>
<tr>
<td>5</td>
<td>Switch the power supply module on again.</td>
<td>• CPU runs the self-tests and changes to STOP.</td>
</tr>
<tr>
<td>6</td>
<td>Perform a CPU memory reset on the replaced CPU.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 7    | Start the replaced CPU (for example, STOP-RUN or Start using the PG). | • The CPU performs an automatic LINK-UP and UPDATE.  
  • The CPU changes to RUN and operates as the reserve CPU. |

Starting situation for replacement of the load memory

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
</table>
| The S7-400H is in redundant system mode and a load memory access error occurs. | • The relevant CPU changes to STOP and requests a memory reset.  
  • The partner CPU switches to single mode. |
Procedure

Follow the steps below to replace the load memory:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Replace the memory card on the stopped CPU.</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>Perform a memory reset on the CPU with the replaced memory card.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 3    | Start the CPU. | • The CPU performs an automatic LINK-UP and UPDATE.  
• The CPU changes to RUN and operates as the reserve CPU. |

16.2.2 Failure and replacement of a power supply module

Starting situation

Both CPUs are in RUN.

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
</table>
| The S7-400H is in redundant system mode and a power supply module fails. | • The partner CPU switches to single mode.  
• The partner CPU reports the event in the diagnostic buffer and in OB 72. |

Procedure

Proceed as follows to replace a power supply module in the central rack:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Turn off the power supply (24 V DC for PS 405 or 120/230 V AC for PS 407).</td>
<td>• The entire subsystem is switched off (system operates in single mode).</td>
</tr>
<tr>
<td>2</td>
<td>Replace the module.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 3    | Switch the power supply module on again. | • The CPU executes the self-tests.  
• The CPU performs an automatic LINK-UP and UPDATE.  
• The CPU changes to RUN (redundant system mode) and operates as reserve CPU. |
Note

Redundant power supply

If you use a redundant power supply (PS 407 10A R), two power supply modules are assigned to one fault-tolerant CPU. If a part of the redundant PS 407 10A R power supply module fails, the associated CPU keeps on running. The defective part can be replaced during operation.

Other power supply modules

If the failure concerns a power supply module outside the central rack (e.g. in the expansion rack or in the I/O device), the failure is reported as a rack failure (central) or station failure (remote). In this case, simply switch off the power supply to the power supply module concerned.

16.2.3 Failure and replacement of an input/output or function module

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>The S7-400H is in redundant system mode and an input/output or function module fails.</td>
<td>• Both CPUs report the event in the diagnostic buffer and via appropriate OBs.</td>
</tr>
</tbody>
</table>

Procedure

⚠️ CAUTION

Note the different procedures.

Minor injury or damage to equipment is possible.

The procedure for replacing an input/output or function module differs for modules of the S7-300 and S7-400.

Use the correct procedure when replacing a module. The correct procedure is described below for the S7-300 and the S7-400.
To replace signal and function modules of an S7-300, perform the following steps:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Disconnect the module from its peripheral power supply, if necessary.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Remove the failed module (in RUN mode).</td>
<td>Both CPUs process the swapping interrupt OB 83 synchronized with each other.</td>
</tr>
<tr>
<td>3</td>
<td>Disconnect the front connector and wiring.</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>Plug the front connector into the new module.</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>Insert the new module.</td>
<td>Both CPUs process the swapping interrupt OB 83 synchronized with each other. Parameters are assigned automatically to the module by the CPU concerned and the module is addressed again.</td>
</tr>
</tbody>
</table>

To replace signal and function modules of an S7-400, perform the following steps:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Disconnect the module from its peripheral power supply, if necessary.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Disconnect the front connector and wiring.</td>
<td>Call OB 82 if the module concerned is capable of diagnostic interrupts and diagnostic interrupts are enabled in the configuration. Call OB 122 if you are accessing the module by direct access Call OB 85 if you are accessing the module using the process image</td>
</tr>
<tr>
<td>3</td>
<td>Remove the failed module (in RUN mode).</td>
<td>Both CPUs process the swapping interrupt OB 83 synchronized with each other.</td>
</tr>
<tr>
<td>4</td>
<td>Insert the new module.</td>
<td>Both CPUs process the swapping interrupt OB 83 synchronized with each other. Parameters are assigned automatically to the module by the CPU concerned and the module is addressed again.</td>
</tr>
<tr>
<td>5</td>
<td>Plug the front connector into the new module.</td>
<td>Call OB 82 if the module concerned is capable of diagnostic interrupts and diagnostic interrupts are enabled in the configuration.</td>
</tr>
</tbody>
</table>
16.2.4 Failure and replacement of a communication module

This section describes the failure and replacement of communication modules for PROFIBUS and Industrial Ethernet.

The failure and replacement of communication modules for PROFIBUS DP are described in section Failure and replacement of a PROFIBUS DP master (Page 263).

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
</table>
| The S7-400H is in redundant system mode and a communication module fails. | • Both CPUs report the event in the diagnostic buffer and via appropriate OBs.  
• In communication via standard connections:  
  Connection failed  
• In communication via redundant connections:  
  Communication is maintained without interruption over an alternate channel. |

Procedure

If you want to use a communication module that is already being used by another system, you have to ensure that there are no parameter data saved in the module's integrated FLASH-EPROM before you swap it.

Proceed as follows to replace a communication module for PROFIBUS or Industrial Ethernet:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Remove the module.</td>
<td>• Both CPUs process the swapping interrupt OB 83 synchronized with each other.</td>
</tr>
</tbody>
</table>
| 2    | Insert the new module. | • Both CPUs process the swapping interrupt OB 83 synchronized with each other.  
• The module is automatically configured by the appropriate CPU. |
| 3    | Turn the module back on. | • The module resumes communication (system establishes communication connection automatically). |
16.2.5 Failure and replacement of a synchronization module or fiber-optic cable

In this section, you will see three different error scenarios:

- Failure of a synchronization module or fiber-optic cable
- Successive failure of both synchronization modules or fiber-optic cables
- Simultaneous failure of both synchronization modules or fiber-optic cables

The CPU indicates by means of LEDs and diagnostics whether the lower or upper redundant link has failed. After the defective parts (fiber-optic cable or synchronization module) have been replaced, LEDs IFM1F and IFM2F must go out.

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure of a fiber-optic cable or synchronization module: The S7-400H is in redundant system mode and a fiber-optic cable or synchronization module fails. See also chapter Synchronization modules for S7-400H (Page 323).</td>
<td>- The master CPU reports the event in the diagnostic buffer and with OB 72 of OB 82. - The reserve CPU changes to ERROR-SEARCH mode for some minutes. If the error is eliminated during this time, the reserve CPU switches to redundant system mode, otherwise it switches to STOP. - The LED Link1 OK or Link2 OK on the synchronization module is lit.</td>
</tr>
</tbody>
</table>

Procedure

Follow the steps below to replace a synchronization module or fiber-optic cable:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>First, check the fiber-optic cable.</td>
<td>~</td>
</tr>
<tr>
<td>2</td>
<td>Start the reserve CPU (for example, STOP-RUN or Start using the programming device).</td>
<td>The following responses are possible: 1. CPU changes to RUN mode. 2. CPU changes to STOP mode. In this case continue at step 3.</td>
</tr>
<tr>
<td>3</td>
<td>Remove the faulty synchronization module from the reserve CPU.</td>
<td>~</td>
</tr>
<tr>
<td>4</td>
<td>Insert the new synchronization module in the reserve CPU.</td>
<td>~</td>
</tr>
<tr>
<td>5</td>
<td>Plug in the fiber-optic cable connections of the synchronization modules.</td>
<td>- The LED Link1 OK or Link2 OK on the synchronization module goes out. - Both CPUs report the event in the diagnostic buffer</td>
</tr>
</tbody>
</table>
### Failure and replacement of components during operation

#### 16.2 Failure and replacement of components during operation

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Start the reserve CPU (for example, STOP-RUN or Start using the programming device).</td>
<td>The following responses are possible:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. CPU changes to RUN mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. CPU changes to STOP mode. In this case continue at step 7.</td>
</tr>
<tr>
<td>7</td>
<td>If the reserve CPU changed to STOP in step 6: Remove the synchronization module from the master CPU.</td>
<td>• The master CPU processes swapping interrupt OB 83 and redundancy error OB 72 (entering state).</td>
</tr>
<tr>
<td>8</td>
<td>Insert the new synchronization module into the master CPU.</td>
<td>• The master CPU processes swapping interrupt OB 83 and redundancy error OB 72 (exiting state).</td>
</tr>
<tr>
<td>9</td>
<td>Plug in the fiber-optic cable connections of the synchronization modules.</td>
<td>–</td>
</tr>
<tr>
<td>10</td>
<td>Start the reserve CPU (for example, STOP-RUN or Start using the programming device).</td>
<td>• The CPU performs an automatic LINK-UP and UPDATE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The CPU changes to RUN (redundant system mode) and operates as reserve CPU.</td>
</tr>
</tbody>
</table>

### Note

If both fiber-optic cables or synchronization modules are damaged or replaced one after the other, the system responses are the same as described above.

The only exception is that the reserve CPU does not change to STOP but instead requests a memory reset.

### Starting situation

#### Failure

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure of both fiber-optic cables or synchronization modules:</td>
<td>• Both CPUs report the event in the diagnostic buffer and via OB 72.</td>
</tr>
<tr>
<td>The S7-400H is in redundant system mode and both fiber-optic cables or synchronization modules fail.</td>
<td>• Both CPUs become the master CPU and remain in RUN mode.</td>
</tr>
<tr>
<td></td>
<td>• The LED Link1 OK or Link2 OK on the synchronization module is lit.</td>
</tr>
</tbody>
</table>
**Procedure**

The double error described results in loss of redundancy. In this event proceed as follows:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Switch off one subsystem.</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>Replace the faulty components.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Turn the subsystem back on.</td>
<td>• LEDs IFM1F and IFM2F go off. The LED MSTR of the switched on subsystem goes out.</td>
</tr>
<tr>
<td>4</td>
<td>Start the CPU (for example Start from programming device or STOP - RUN).</td>
<td>• The CPU performs an automatic LINK-UP and UPDATE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The CPU changes to RUN (redundant system mode) and operates as reserve CPU.</td>
</tr>
</tbody>
</table>
16.2.6 Failure and replacement of an IM 460 and IM 461 interface module

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>The S7-400H is in redundant system mode and an interface module fails.</td>
<td>• The connected expansion unit is turned off.</td>
</tr>
<tr>
<td></td>
<td>• Both CPUs report the event in the diagnostic buffer and via OB 86.</td>
</tr>
</tbody>
</table>

Procedure

Follow the steps below to replace an interface module:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Turn off the power supply of the central rack.</td>
<td>• The partner CPU switches to single mode.</td>
</tr>
<tr>
<td>2</td>
<td>Turn off the power supply of the expansion unit in which you want to replace the interface module.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Remove the interface module.</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>Insert the new interface module and turn the power supply of the expansion unit back on.</td>
<td>–</td>
</tr>
<tr>
<td>5</td>
<td>Switch the power supply of the central unit back on and start the CPU.</td>
<td>• The CPU performs an automatic LINK-UP and UPDATE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The CPU changes to RUN and operates as the reserve CPU.</td>
</tr>
</tbody>
</table>
16.3 Failure and replacement of components of the distributed I/Os

Which components can be replaced?

The following components of the distributed I/Os can be replaced during operation:

- PROFIBUS DP master
- PROFIBUS DP interface module (IM 153-2 or IM 157)
- PROFIBUS DP slave
- PROFIBUS DP cable

Note

Replacing I/O and function modules located in a distributed station is described in section Failure and replacement of an input/output or function module (Page 256).

16.3.1 Failure and replacement of a PROFIBUS DP master

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>The S7-400H is in redundant system mode and a DP master module fails.</td>
<td>• With single-channel one-sided I/O: The DP master can no longer process connected DP slaves. • With switched I/O: DP slaves are addressed via the DP master of the partner.</td>
</tr>
</tbody>
</table>

Procedure

Proceed as follows to replace a PROFIBUS DP master:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Turn off the power supply of the central rack.</td>
<td>The fault-tolerant system switches to single mode.</td>
</tr>
<tr>
<td>2</td>
<td>Unplug the Profibus DP cable of the affected DP master module.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Replace the module.</td>
<td>–</td>
</tr>
</tbody>
</table>
### Failure and replacement of components during operation

#### 16.3 Failure and replacement of components of the distributed I/Os

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Plug the Profibus DP back in.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 5    | Turn on the power supply of the central rack. | • The CPU performs an automatic LINK-UP and UPDATE.  
• The CPU changes to RUN and operates as the reserve CPU. |

#### Exchanging a CP 443-5 in case of spare part requirement

If a CP 443-5 is replaced by a successor module with a new article number, always both modules must be replaced in the case of redundantly used components.

Redundantly used modules must be identical, i.e. they must have the same article number, product version and firmware version.

Proceed as follows:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Stop the standby CPU</td>
<td>The fault-tolerant system switches to single mode, see chapter PCS 7, step 3: Stopping the reserve CPU (Page 276) or STEP 7, step 4: Stopping the reserve CPU (Page 294)</td>
</tr>
<tr>
<td>2</td>
<td>Turn off the power supply of the central rack.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Unplug the Profibus DP cable of the affected DP master module.</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>Replace the module.</td>
<td>–</td>
</tr>
<tr>
<td>5</td>
<td>Plug the Profibus DP back in.</td>
<td>–</td>
</tr>
<tr>
<td>6</td>
<td>Turn on the power supply of the central rack.</td>
<td>–</td>
</tr>
<tr>
<td>7</td>
<td>Switch to the CPU with the modified configuration.</td>
<td>The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single modePCS 7, step 5: Switch to CPU with modified configuration (Page 277) or chapter STEP 7, step 6: Switch to CPU with modified configuration (Page 295)</td>
</tr>
<tr>
<td>8</td>
<td>Turn off the power supply of the second central rack.</td>
<td>–</td>
</tr>
<tr>
<td>9</td>
<td>Unplug the Profibus DP cable of the second DP master module.</td>
<td>–</td>
</tr>
<tr>
<td>10</td>
<td>Replace the module.</td>
<td>–</td>
</tr>
<tr>
<td>11</td>
<td>Plug the Profibus DP back in.</td>
<td>–</td>
</tr>
</tbody>
</table>
16.3 Failure and replacement of components of the distributed I/Os

### 16.3.2 Failure and replacement of a redundant PROFIBUS DP interface module

**Starting situation**

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>The S7-400H is in redundant system mode and a PROFIBUS DP interface module (IM 153–2, IM 157) fails.</td>
<td>Both CPUs report the event in the diagnostic buffer and via OB 70.</td>
</tr>
</tbody>
</table>

**Replacement procedure**

Proceed as follows to replace the PROFIBUS DP interface module:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Turn off the supply for the affected DP interface module.</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>Remove the bus connector.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Insert the new PROFIBUS DP interface module and turn the power supply back on.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 4    | Plug the bus connector back in. | • The CPUs process the I/O redundancy error OB 70 (outgoing event) synchronized with each other.  
• Redundant access to the station by the system is now possible again. |
16.3.3 Failure and replacement of a PROFIBUS DP slave

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>The S7-400H is in redundant system mode and a DP slave fails.</td>
<td>Both CPUs report the event in the diagnostic buffer and via the appropriate OB.</td>
</tr>
</tbody>
</table>

Procedure

Proceed as follows to replace a DP slave:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Turn off the supply for the DP slave.</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>Remove the bus connector.</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Replace the DP slave.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 4    | Plug the bus connector back in and turn the power supply back on. | • The CPUs process the rack failure OB 86 synchronized with each other (outgoing event)  
• The associated DP master can address the DP slave. |

16.3.4 Failure and replacement of PROFIBUS DP cables

Starting situation

<table>
<thead>
<tr>
<th>Failure</th>
<th>How does the system react?</th>
</tr>
</thead>
</table>
| The S7-400H is in redundant system mode and the PROFIBUS DP cable is defective. | • With single-channel one-sided I/O:  
Rack failure OB (OB 86) is started (incoming event). The DP master can no longer process connected DP slaves (station failure).  
• With switched I/O:  
I/O redundancy error OB (OB 70) is started (incoming event). DP slaves are addressed via the DP master of the partner. |
Replacement procedure

Proceed as follows to replace PROFINET DP cables:

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Check the cabling and localize the interrupted PROFIBUS DP cable.</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>Replace the defective cable.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 3    | Switch the failed modules to RUN mode. | The CPUs process the error OBs synchronized with each other  
• With one-sided I/O:  
  Rack failure OB 86 (outgoing event)  
  The DP slaves can be addressed via the DP master system.  
• With switched I/O:  
  I/O redundancy error OB 70 (outgoing event).  
  The DP slaves can be addressed via both DP master systems. |
Failure and replacement of components during operation

16.3 Failure and replacement of components of the distributed I/Os
17.1 System modifications during operation

In addition to the options described in chapter Failure and replacement of components during operation [Page 253] for replacing failed components during operation, you can also make changes to the system in a fault-tolerant system without interrupting the running program.

The procedure partially depends on whether you are working with your user software in PCS 7 or STEP 7.

The procedures described below for changes during operation are designed so that you start with the redundant system mode (see chapter The system states of the S7-400H [Page 117]) with the aim of returning to this mode when the procedures are completed.

Note

Keep strictly to the rules described in this section with regard to modifications of the system in runtime. If you contravene one or more rules, the response of the fault-tolerant system can result in its availability being restricted or even failure of the entire automation system.

Only perform a system change in runtime when there is no redundancy error, i.e. when the REDF LED is not lit. The automation system may otherwise fail.

The cause of a redundancy error is listed in the diagnostic buffer.

Safety-related components are not taken into account in this description. For more information on dealing with fail-safe systems refer to the S7-400F and S7-400FH Automation Systems manual.
17.2 Possible hardware modifications

How is a hardware modification made?

If the hardware components concerned are suitable for unplugging or plugging in live, the hardware modification can be carried out in redundant system mode. However, the fault-tolerant system must be operated temporarily in single mode, because any download of new hardware configuration data in redundant system mode would inevitably cause it to stop. In single mode the process is then controlled only by one CPU while you can carry out the relevant configuration changes at the partner CPU.

**WARNING**

During a hardware modification, you can either remove or add modules. If you want to alter your fault-tolerant system such that you remove modules and add others, you have to make two hardware changes.

**Note**

Always download configuration changes to the CPU using the "Configure hardware" function.

Load memory data of both CPUs must be updated several times in the process. It is therefore advisable to expand the integrated load memory with a RAM card (at least temporarily).

You may only change the FLASH card to a RAM card as required for this if the FLASH card has as much maximum storage space as the largest RAM card available. If you cannot obtain a RAM card with a capacity to match the FLASH card memory space, split the relevant configuration and program modifications into several smaller steps in order to provide sufficient space in the integrated load memory.

**Synchronization link**

Whenever you make hardware modifications, make sure that the synchronization link between the two CPUs is established before you start or turn on the reserve CPU. If the power supply to the CPUs is on, the LEDs IFM1F and IFM2F that indicate errors on the module interfaces on the two CPUs should go off.

If one of the IFM LEDs continues to be lit even after you have replaced the relevant synchronization modules, the synchronization cables and even the reserve CPU, there is an error in the master CPU. In this case, you can, however, switch to the reserve CPU by selecting the "via only one intact redundancy link" option in the "Switch" STEP 7 dialog box.
Which components can be modified?

The following modifications can be made to the hardware configuration during operation:

- Adding or removing modules in the central or expansion units (e.g. one-sided I/O module).

**Note**

Always switch off power before you add or remove IM460 and IM461 interface modules, external CP443-5 Extended DP master interface modules, and their connecting cables.

- Adding or removing components of the distributed I/Os such as
  - DP slaves with a redundant interface module (e.g. ET 200M, DP/PA link, or Y link)
  - One-sided DP slaves (in any DP master system)
  - Modules in modular DP slaves
  - DP/PA links
  - PA devices
- Changing specific CPU parameters
- Changing the CPU memory configuration
- Re-parameterization of a module
- Assigning a module to another process image partition
- Upgrading the CPU version
- Changing the master with only one available redundant link

**Note**

No changes to the PROFINET interface at runtime

I/O components that are connected to a PROFINET interface as well as parameters of the PROFINET interface cannot be modified during operation.

When you make any modifications, keep to the rules for the configuration of a fault-tolerant station (see section Rules for the assembly of fault-tolerant stations (Page 31)).

What should I consider during system planning?

For switched I/O to be expanded during operation, the following points must be taken into account already at the system planning stage:

- In both cables of a redundant DP master system, sufficient numbers of branching points are to be provided for spur lines or isolating points (spur lines are not permitted for transmission rates of 12 Mbit/s). These branching points can be spaced or implemented at any points that can be accessed easily.

- Both cables must be uniquely identified so that the line which is currently active is not accidentally cut off. This identification should be visible not only at the end points of a line, but also at each possible new connection point. Different colored cables are especially suitable for this.
System modifications during operation

17.2 Possible hardware modifications

- Modular DP slave stations (ET 200M), DP/PA links and Y links must always be installed with an active backplane bus and fitted with all the bus modules required wherever possible, because the bus modules cannot be installed and removed during operation.

- Always terminate both ends of PROFIBUS DP and PROFIBUS PA bus cables using active bus terminating elements in order to ensure proper termination of the cables while you are reconfiguring the system.

- PROFIBUS PA bus systems should be built up using components from the SpliITConnect product range (see interactive catalog CA01) so that separation of the lines is not required.

- Loaded data blocks must not be deleted and created again. In other words, SFC 22 (CREATE_DB) and SFC 23 (DEL_DB) may not be applied to DB numbers occupied by loaded DBs.

- Always ensure that the current status of the user program is available as STEP 7 project in block format at the PG/ES when you modify the system configuration. It is not enough to upload the user program back from one of the CPUs to the PG/ES or to compile it again from an STL source.

Modification of the hardware configuration

With a few exceptions, all elements of the configuration can be modified during operation. Usually configuration changes will also affect the user program.

The following must not be changed by means of system modifications during operation:

- Certain CPU parameters (for details refer to the relevant subsections)
- The transmission rate (baud rate) of redundant DP master systems
- S7 and S7 H connections

Modifications to the user program and the connection configuration

The modifications to the user program and connection configuration are loaded into the target system in redundant system mode. The procedure depends on the software used. For more details refer to the Programming with STEP 7 manual and the PCS 7, Configuration Manual.

Note

After reloading connections/gateways, it is no longer possible to change from a RAM card to a FLASH card.
Special features

- Keep changes to a manageable extent. We recommend that you modify only one DP master and/or a few DP slaves (e.g. no more than 5) per reconfiguration run.

- When using an IM 153-2, active bus modules can only be plugged in if the power supply is off.

---

**Note**

Remember the following when using redundant I/O that you have implemented as one-sided I/O at the user level (see section Other options for connecting redundant I/Os (Page 198)):

Due to the link-up and update process carried out after a system modification, the I/O data of the previous master CPU may be temporarily deleted from the process image until all (changed) I/Os of the "new" master CPU are written to the process image.

During the first update of the process image after a system modification, you may (incorrectly) have the impression that the redundant I/O has failed completely or that a redundant I/O exists. So correct evaluation of the redundancy status is not possible until the process image has been fully updated.

This does not apply for modules that have been enabled for redundant operation (see section Connecting redundant I/O to the PROFIBUS DP interface (Page 171)).

---

**Preparations**

To minimize the time during which the fault-tolerant system has to run in single mode, perform the following steps before making the hardware change:

- Check whether the CPUs provide sufficient memory capacity for the new configuration data and user program. If necessary, first expand the memory configuration (see section Changing the CPU memory configuration (Page 313)).

- Always ensure that plugged modules which are not configured yet do not have any unwanted influence on the process.

---

**17.3 Adding components in PCS 7**

**Starting situation**

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 308)).

The fault-tolerant system is operating in redundant system mode.
System modifications during operation

17.3 Adding components in PCS 7

Procedure

Carry out the steps listed below to add hardware components to a fault-tolerant system in PCS 7. Details of each step are described in a subsection.

<table>
<thead>
<tr>
<th>Step</th>
<th>What has to be done?</th>
<th>See section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modification of hardware</td>
<td>PCS 7, step 1: Modification of hardware (Page 275)</td>
</tr>
<tr>
<td>2</td>
<td>Offline modification of the hardware configuration</td>
<td>PCS 7, step 2: Offline modification of the hardware configuration (Page 275)</td>
</tr>
<tr>
<td>3</td>
<td>Stopping the reserve CPU</td>
<td>PCS 7, step 3: Stopping the reserve CPU (Page 276)</td>
</tr>
<tr>
<td>4</td>
<td>Loading a new hardware configuration in the reserve CPU</td>
<td>PCS 7, step 4: Loading a new hardware configuration in the reserve CPU (Page 277)</td>
</tr>
<tr>
<td>5</td>
<td>Switching to CPU with modified configuration</td>
<td>PCS 7, step 5: Switch to CPU with modified configuration (Page 277)</td>
</tr>
<tr>
<td>6</td>
<td>Transition to redundant system mode</td>
<td>PCS 7, step 6: Transition to redundant system mode (Page 278)</td>
</tr>
<tr>
<td>7</td>
<td>Editing and downloading the user program</td>
<td>PCS 7, step 7: Editing and downloading the user program (Page 279)</td>
</tr>
</tbody>
</table>

Exceptions

This procedure for system modification does not apply in the following cases:

- To use free channels on an existing module
- For adding interface modules (see section Adding interface modules in PCS 7 (Page 282))

Note

After changing the hardware configuration, it is downloaded practically automatically. This means that you no longer need to perform the steps described in sections PCS 7, step 3: Stopping the reserve CPU (Page 276) to PCS 7, step 6: Transition to redundant system mode (Page 278). The system behavior remains unchanged as already described.

You will find more information in the HW Config online help, "Download to module -> Download station configuration in RUN mode".
17.3.1 PCS 7, step 1: Modification of hardware

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure

1. Add the new components to the system.
   - Plug new central modules into the racks.
   - Plug new module into existing modular DP stations
   - Add new DP stations to existing DP master systems.

   **Note**
   With switched I/O: Always complete all changes on **one** segment of the redundant DP master system before you modify the next segment.

2. Connect the required sensors and actuators to the new components.

Result
The insertion of non-configured modules will have no effect on the user program. The same applies to adding DP stations.
The fault-tolerant system continues to operate in redundant system mode.
New components are not yet addressed.

17.3.2 PCS 7, step 2: Offline modification of the hardware configuration

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure

1. Perform all the modifications to the hardware configuration relating to the added hardware offline. Assign appropriate icons to the new channels to be used.

2. Compile the new hardware configuration, but do **not** load it into the target system just yet.

Result
The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.
Configuring connections

The interconnections with added CPs must be configured on both connection partners after you complete the HW modification.

17.3.3 PCS 7, step 3: Stopping the reserve CPU

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

Although I/O access errors of the one-sided I/O will result in OB 85 being called, due to the higher-priority CPU redundancy loss (OB 72) they will not be reported. OB 70 (I/O redundancy loss) is not called.
17.3.4 PCS 7, step 4: Loading a new hardware configuration in the reserve CPU

**Starting situation**

The fault-tolerant system is operating in single mode.

**Procedure**

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

**Note**

The user program and connection configuration cannot be downloaded in single mode.

**Result**

The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.

17.3.5 PCS 7, step 5: Switch to CPU with modified configuration

**Starting situation**

The modified hardware configuration is downloaded to the reserve CPU.

**Procedure**

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
   In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
3. Acknowledge the prompt for confirmation with "OK".

**Result**

The reserve CPU links up, is updated (see chapter Link-up and update [Page 135]) and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single mode.
System modifications during operation

17.3 Adding components in PCS 7

Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of previous master CPU</th>
<th>One-sided I/O of new master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added I/O modules</td>
<td>are not addressed by the CPU.</td>
<td>are given new parameter settings and updated by the CPU. Driver blocks are not yet present. Process or diagnostic interrupts are detected, but are not reported.</td>
<td></td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are no longer addressed by the CPU. Output modules output the configured substitute or holding values.</td>
<td>are given new parameter settings and updated by the CPU.</td>
<td>continue operation without interruption.</td>
</tr>
<tr>
<td>Added DP stations</td>
<td>are not addressed by the CPU.</td>
<td>as for added I/O modules (see above)</td>
<td>continue operation without interruption.</td>
</tr>
</tbody>
</table>

1) The central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or holding values).

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to chapter Time monitoring (Page 149).

17.3.6 PCS 7, step 6: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU links up and is updated. The fault-tolerant system is operating with the new hardware configuration in redundant system mode.
Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of reserve CPU</th>
<th>One-sided I/O of master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added I/O modules</td>
<td>are given new parameter settings and updated by the CPU. Driver blocks are not yet present. Any interrupts occurring are not reported.</td>
<td>are updated by the CPU. Driver blocks are not yet present. Process or diagnostic interrupts are detected, but are not reported.</td>
<td></td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are given new parameter settings(^1) and updated by the CPU.</td>
<td>continue operation without interruption.</td>
<td></td>
</tr>
<tr>
<td>Added DP stations</td>
<td>as for added I/O modules (see above)</td>
<td>Driver blocks are not yet present. Any interrupts occurring are not reported.</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the link-up and update later. For additional information, refer to section Time monitoring (Page 149).

17.3.7 PCS 7, step 7: Editing and downloading the user program

Starting situation

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

**CAUTION**

The following program modifications are not possible in redundant system mode and result in the system mode Stop (both CPUs in STOP mode):
- Structural modifications to an FB interface or the FB instance data.
- Structural modifications to global DBs.
- Compression of the CFC user program.

Before the entire program is recompiled and reloaded due to such modifications the parameter values must be read back into the CFC, otherwise the modifications to the block parameters could be lost. You will find more detailed information on this topic in the CFC for S7, Continuous Function Chart manual.
**System modifications during operation**

### 17.3 Adding components in PCS 7

**Procedure**

1. Adapt the program to the new hardware configuration. You can add the following components:
   - CFCs and SFCs
   - Blocks in existing charts
   - Connections and parameter settings

2. Assign parameters for the added channel drivers and interconnect them with the newly assigned icons (see section PCS 7, step 2: Offline modification of the hardware configuration (Page 275)).

3. In SIMATIC Manager, select the charts folder and choose the "Options > Charts > Generate Module Drivers" menu command.

4. Compile only the modifications in the charts and download them to the target system.

5. Configure the interconnections for the new CPs on both communication partners and download them to the target system.

**Result**

The fault-tolerant system processes the entire system hardware with the new user program in redundant system mode.

### 17.3.8 PCS7, Using free channels on an existing module

The use of previously free channels of an I/O module depends mainly on the fact if the module can be configured or not.

**Non-configurable modules**

Free channels can be switched and used in the user program at any time in case of non-configurable modules.

**Configurable modules**

The hardware configuration first has to be matched to the used sensors or actuators for configurable modules. This step usually requires a new configuration of the entire module in most cases.

This means an uninterrupted operation of the respective modules is no longer possible:

- One-sided output modules briefly output 0 during this time (instead of the configured substitute or hold values).
- Modules in switched DP stations are not reconfigured when you switch over to the CPU with the modified configuration.
Proceed as follows to change the channel use:

- In steps 1 to 5, you completely remove the respective module from the hardware configuration and the user program. But it can remain inserted in the DP station. The module drivers must not be removed.
- In steps 2 to 7, you add the module with the modified use once again to the hardware configuration and the user program.

---

**Note**

The respective modules are not addressed between the two changeover steps (steps V and 5); respective output modules output the value 0. The existing channel drivers in the user program hold their signals.

If this behavior is unacceptable for the process to be controlled, there is no other way to use previously free channels. In this case you must install additional modules to expand the system.
17.3.9 Adding interface modules in PCS 7

Always switch off power before you install the IM460 and IM461 interface modules, external CP443-5 Extended DP master interface module and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure

1. Change the hardware configuration offline (see section PCS 7, step 2: Offline modification of the hardware configuration (Page 275))
2. Stop the reserve CPU (see section PCS 7, step 3: Stopping the reserve CPU (Page 276))
3. Download the new hardware configuration to the reserve CPU (see section PCS 7, step 4: Loading a new hardware configuration in the reserve CPU (Page 277))
4. Proceed as follows to expand the subsystem of the present reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.
   - or
   - Add a new expansion unit to an existing chain.
   - or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.
5. Switch to CPU with altered configuration (see section PCS 7, step 5: Switch to CPU with modified configuration (Page 277))
6. Proceed as follows to expand the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.
   - or
   - Add a new expansion unit to an existing chain.
   - or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.
7. Change to redundant system mode (see section PCS 7, step 6: Transition to redundant system mode (Page 278))
8. Modify and download the user program (see section PCS 7, step 7: Editing and downloading the user program (Page 279))
17.4 Removing components in PCS 7

Starting situation

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 308)).

The modules to be removed and their connected sensors and actuators are no longer of any significance to the process being controlled. The fault-tolerant system is operating in redundant system mode.

Procedure

Carry out the steps listed below to remove hardware components from a fault-tolerant system in PCS 7. Details of each step are described in a subsection.

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>See section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Offline modification of the hardware configuration</td>
<td>PCS 7, step 1: Editing the hardware configuration offline (Page 284)</td>
</tr>
<tr>
<td>2</td>
<td>Editing and downloading the user program</td>
<td>PCS 7, step 2: Editing and downloading the user program (Page 285)</td>
</tr>
<tr>
<td>3</td>
<td>Stopping the reserve CPU</td>
<td>PCS 7, step 3: Stopping the reserve CPU (Page 286)</td>
</tr>
<tr>
<td>4</td>
<td>Loading a new hardware configuration in the reserve CPU</td>
<td>PCS 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 288)</td>
</tr>
<tr>
<td>5</td>
<td>Switch to CPU with modified configuration</td>
<td>PCS 7, step 5: Switching to CPU with modified configuration (Page 287)</td>
</tr>
<tr>
<td>6</td>
<td>Transition to redundant system mode</td>
<td>PCS 7, step 6: Transition to redundant system mode (Page 288)</td>
</tr>
<tr>
<td>7</td>
<td>Modification of hardware</td>
<td>PCS 7, step 7: Modification of hardware (Page 289)</td>
</tr>
</tbody>
</table>

Exceptions

This general procedure for system modifications does not apply to removing interface modules (see section Removing interface modules in PCS 7 (Page 290)).

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections PCS 7, step 3: Stopping the reserve CPU (Page 286) to PCS 7, step 6: Transition to redundant system mode (Page 288). The system behavior remains as described.

You will find more information in the HW Config online help, "Download to module -> Download station configuration in RUN mode".
17.4 Removing components in PCS 7

17.4.1 PCS 7, step 1: Editing the hardware configuration offline

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure
1. Perform offline only the configuration modifications relating to the hardware being removed. As you do, delete the icons to the channels that are no longer used.
2. Compile the new hardware configuration, but do not load it into the target system just yet.

Result
The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.
17.4 Removing components in PCS 7

17.4.2 PCS 7, step 2: Editing and downloading the user program

Starting situation

The fault-tolerant system is operating in redundant system mode.

<table>
<thead>
<tr>
<th>CAUTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>The following program modifications are not possible in redundant system mode and result in the system mode Stop (both CPUs in STOP mode):</td>
</tr>
<tr>
<td>• Structural modifications to an FB interface or the FB instance data.</td>
</tr>
<tr>
<td>• Structural modifications to global DBs.</td>
</tr>
<tr>
<td>• Compression of the CFC user program.</td>
</tr>
<tr>
<td>Before the entire program is recompiled and reloaded due to such modifications the parameter values must be read back into the CFC, otherwise the modifications to the block parameters could be lost. You will find more detailed information on this topic in the CFC for S7, Continuous Function Chart manual.</td>
</tr>
</tbody>
</table>

Procedure

1. Edit only the program elements related to the hardware removal. You can delete the following components:
   - CFCs and SFCs
   - Blocks in existing charts
   - Channel drivers, interconnections and parameter settings
2. In SIMATIC Manager, select the charts folder and choose the "Options > Charts > Generate Module Drivers" menu command.
   This removes the driver blocks that are no longer required.
3. Compile only the modifications in the charts and download them to the target system.

Note

Until an FC is called the first time, the value of its output is undefined. This must be taken into account in the interconnection of the FC outputs.

Result

The fault-tolerant system continues to operate in redundant system mode. The modified user program will no longer attempt to access the hardware being removed.
17.4 Removing components in PCS 7

17.4.3 PCS 7, step 3: Stopping the reserve CPU

Starting situation
The fault-tolerant system is operating in redundant system mode. The user program will no longer attempt to access the hardware being removed.

Procedure
1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result
The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

17.4.4 PCS 7, step 4: Downloading a new hardware configuration to the reserve CPU

Starting situation
The fault-tolerant system is operating in single mode.

Procedure
Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

Note
The user program and connection configuration cannot be downloaded in single mode.

Result
The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.
17.4 Removing components in PCS 7

17.4.5 PCS 7, step 5: Switching to CPU with modified configuration

Starting situation
The modified hardware configuration is downloaded to the reserve CPU.

Procedure
1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result
The reserve CPU links up, is updated (see section Link-up and update (Page 135)) and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single mode.

Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of previous master CPU</th>
<th>One-sided I/O of new master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules to be removed ¹)</td>
<td>are no longer addressed by the CPU. Driver blocks are no longer present.</td>
<td></td>
<td>continue operation without interruption.</td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are no longer addressed by the CPU. Output modules output the configured substitute or holding values.</td>
<td>are given new parameter settings ²) and updated by the CPU.</td>
<td></td>
</tr>
<tr>
<td>DP stations to be removed</td>
<td>as for I/O modules to be removed (see above)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹) No longer included in the hardware configuration, but still plugged in
²) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

Reaction to monitoring timeout
The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 149).
17.4.6 PCS 7, step 6: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU links up and is updated. The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of reserve CPU</th>
<th>One-sided I/O of master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules to be removed(^1)</td>
<td>are no longer addressed by the CPU.</td>
<td></td>
<td>continue operation without interruption.</td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are given new parameter settings(^2) and updated by the CPU.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP stations to be removed</td>
<td>as for I/O modules to be removed (see above)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) No longer included in the hardware configuration, but still plugged in
\(^2\) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the link-up and update later. For additional information, refer to section Time monitoring (Page 149).
17.4 Removing components in PCS 7

17.4.7 PCS 7, step 7: Modification of hardware

Starting situation
The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Procedure
1. Disconnect all the sensors and actuators from the components you want to remove.
2. Unplug modules of the one-sided I/Os that are no longer required from the racks.
3. Unplug components that are no longer required from the modular DP stations.
4. Remove DP stations that are no longer required from the DP master systems.

Note
With switched I/O: Always complete all changes on one segment of the redundant DP master system before you modify the next segment.

Result
The removal of non-configured modules does not influence the user program. The same applies to removing DP stations.

The fault-tolerant system continues to operate in redundant system mode.
17.4.8 Removing interface modules in PCS 7

Always switch off the power before you remove the IM460 and IM461 interface modules, external CP 443-5 Extended DP master interface module, and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure

1. Change the hardware configuration offline (see section PCS 7, step 1: Editing the hardware configuration offline (Page 284))
2. Modify and download the user program (see section PCS 7, step 2: Editing and downloading the user program (Page 285))
3. Stop the reserve CPU (see section PCS 7, step 3: Stopping the reserve CPU (Page 286))
4. Download the new hardware configuration to the reserve CPU (see section PCS 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 286))
5. Follow the steps below to remove an interface module from the subsystem of the reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Remove an IM460 from the central unit.
     or
   - Remove an expansion unit from an existing chain.
     or
   - Remove an external DP master interface module.
   - Switch on the power supply of the reserve subsystem again.
6. Switch to CPU with altered configuration (see section PCS 7, step 5: Switching to CPU with modified configuration (Page 287))
7. Proceed as follows to remove an interface module from the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Remove an IM460 from the central unit.
     or
   - Remove an expansion unit from an existing chain.
     or
   - Remove an external DP master interface module.
   - Switch on the power supply of the reserve subsystem again.
8. Change to redundant system mode (see section PCS 7, step 6: Transition to redundant system mode (Page 288))
17.5 Adding components in STEP 7

Starting situation
You have verified that the CPU parameters (e.g. monitoring times) match the planned new
program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters
(Page 308)).

The fault-tolerant system is operating in redundant system mode.

Procedure
Carry out the steps listed below to add hardware components to a fault-tolerant system in
STEP 7. Details of each step are described in a subsection.

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>See section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modification of hardware</td>
<td>STEP 7, step 1: Adding hardware (Page 292)</td>
</tr>
<tr>
<td>2</td>
<td>Editing the hardware configuration offline</td>
<td>STEP 7, step 2: Offline modification of the hardware configuration (Page 293)</td>
</tr>
<tr>
<td>3</td>
<td>Expanding and downloading OBs</td>
<td>STEP 7, step 3: Expanding and downloading OBs (Page 293)</td>
</tr>
<tr>
<td>4</td>
<td>Stopping the reserve CPU</td>
<td>STEP 7, step 4: Stopping the reserve CPU (Page 294)</td>
</tr>
<tr>
<td>5</td>
<td>Downloading a new hardware configuration to the reserve CPU</td>
<td>STEP 7, step 5: Loading a new hardware configuration in the reserve CPU (Page 294)</td>
</tr>
<tr>
<td>6</td>
<td>Switching to CPU with modified configuration</td>
<td>STEP 7, step 6: Switch to CPU with modified configuration (Page 295)</td>
</tr>
<tr>
<td>7</td>
<td>Transition to redundant system mode</td>
<td>STEP 7, step 7: Transition to redundant system mode (Page 296)</td>
</tr>
<tr>
<td>8</td>
<td>Editing and downloading the user program</td>
<td>STEP 7, step 8: Editing and downloading the user program (Page 297)</td>
</tr>
</tbody>
</table>
System modifications during operation

17.5 Adding components in STEP 7

Exceptions

This procedure for system modification does not apply in the following cases:

- To use free channels on an existing module
- For adding interface modules (see section "Adding interface modules in STEP 7" on page 299)

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections STEP 7, step 4: Stopping the reserve CPU (Page 294) to STEP 7, step 8: Editing and downloading the user program (Page 297). The system behavior remains as described.

You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode".

17.5.1 STEP 7, step 1: Adding hardware

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Add the new components to the system.
   - Plug new central modules into the racks.
   - Plug new module into existing modular DP stations
   - Add new DP stations to existing DP master systems.

   Note
   With switched I/O: Always complete all changes on one segment of the redundant DP master system before you modify the next segment.

2. Connect the required sensors and actuators to the new components.

Result

The insertion of non-configured modules will have no effect on the user program. The same applies to adding DP stations.

The fault-tolerant system continues to operate in redundant system mode.

New components are not yet addressed.
17.5.2 STEP 7, step 2: Offline modification of the hardware configuration

Starting situation
The fault-tolerant system is operating in redundant system mode. The modules added are not yet addressed.

Procedure
1. Perform all the modifications to the hardware configuration relating to the added hardware offline.
2. Compile the new hardware configuration, but do not load it into the target system just yet.

Result
The modified hardware configuration is in the PG. The target system continues operation with the old configuration in redundant system mode.

Configuring connections
The interconnections with added CPs must be configured on both connection partners after you complete the HW modification.

17.5.3 STEP 7, step 3: Expanding and downloading OBs

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure
1. Verify that the interrupt OBs 4x, 82, 83, 85, 86, OB 88 and 122 react to any interrupts of the new components as intended.
2. Download the modified OBs and the corresponding program elements to the target system.

Result
The fault-tolerant system is operating in redundant system mode.
17.5.4  **STEP 7, step 4: Stopping the reserve CPU**

**Starting situation**

The fault-tolerant system is operating in redundant system mode.

**Procedure**

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

**Result**

The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed. OB 70 (I/O redundancy loss) is not called due to the higher-priority CPU redundancy loss (OB72).

17.5.5  **STEP 7, step 5: Loading a new hardware configuration in the reserve CPU**

**Starting situation**

The fault-tolerant system is operating in single mode.

**Procedure**

Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

**Note**

The user program and connection configuration cannot be downloaded in single mode.

**Result**

The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.
17.5.6  **STEP 7, step 6: Switch to CPU with modified configuration**

**Starting situation**

The modified hardware configuration is downloaded to the reserve CPU.

**Procedure**

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

**Result**

The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system operates with the new hardware configuration in single mode.

**Reaction of the I/O**

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of previous master CPU</th>
<th>One-sided I/O of new master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added I/O modules</td>
<td>are not addressed by the CPU.</td>
<td>are given new parameter settings and updated by the CPU.</td>
<td>The output modules temporarily output the configured substitution values.</td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are no longer addressed by the CPU. Output modules output the configured substitute or holding values.</td>
<td>are given new parameter settings(^1) and updated by the CPU.</td>
<td>continue operation without interruption.</td>
</tr>
<tr>
<td>Added DP stations</td>
<td>are not addressed by the CPU.</td>
<td>as for added I/O modules (see above)</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

**Reaction to monitoring timeout**

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section **Time monitoring** (Page 149).
17.5.7  
STEP 7, step 7: Transition to redundant system mode

Starting situation

The fault-tolerant system is operating with the new hardware configuration in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU links up and is updated. The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of reserve CPU</th>
<th>One-sided I/O of master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added I/O modules</td>
<td>are given new parameter settings and updated by the CPU. The output modules temporarily output the configured substitution values.</td>
<td>are updated by the CPU.</td>
<td>are updated by the CPU. Generate insertion interrupt; must be ignored in OB 83.</td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are given new parameter settings(^1) and updated by the CPU.</td>
<td>continue operation without interruption.</td>
<td></td>
</tr>
<tr>
<td>Added DP stations</td>
<td>as for added I/O modules (see above)</td>
<td>are updated by the CPU.</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the link-up and update later. For additional information, refer to section Time monitoring (Page 149).
17.5.8 **STEP 7, step 8: Editing and downloading the user program**

**Starting situation**

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

**Restrictions**

<table>
<thead>
<tr>
<th><strong>CAUTION</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Any attempts to modify the structure of an FB interface or the instance data of an FB in redundant system mode will lead to stop system mode (both CPUs in STOP mode).</td>
</tr>
</tbody>
</table>

**Procedure**

1. Adapt the program to the new hardware configuration.
   
   You can add, edit or remove OBs, FBs, FCs and DBs.

2. Download only the program changes to the target system.

3. Configure the interconnections for the new CPs on both communication partners and download them to the target system.

**Note**

Until an FC is called the first time, the value of its output is undefined. This must be taken into account in the interconnection of the FC outputs.

**Result**

The fault-tolerant system processes the entire system hardware with the new user program in redundant system mode.

17.5.9 **STEP7, Using free channels on an existing module**

The use of previously free channels of an I/O module depends mainly on the fact if the module can be configured or not.

**Non-configurable modules**

Free channels can be switched and used in the user program at any time in case of non-configurable modules.
**System modifications during operation**

17.5 Adding components in STEP 7

---

**Configurable modules**

The hardware configuration first has to be matched to the used sensors or actuators for configurable modules. This step usually requires a new configuration of the entire module in most cases.

This means an uninterrupted operation of the respective modules is no longer possible:

- One-sided output modules briefly output 0 during this time (instead of the configured substitute or hold values).
- Modules in switched DP stations are not reconfigured when you switch over to the CPU with the modified configuration.

Proceed as follows to change the channel use:

- In steps 1 to 5, you completely remove the respective module from the hardware configuration and the user program. But it can remain inserted in the DP station.
- In steps 3 to 8, you add the module with the modified use once again to the hardware configuration and the user program.

---

**Note**

The respective modules are not addressed between the two changeover steps (steps V and 6); respective output modules output the value 0.

If this behavior is unacceptable for the process to be controlled, there is no other way to use previously free channels. In this case you must install additional modules to expand the system.
### 17.5.10 Adding interface modules in STEP 7

Always switch off power before you install the IM460 and IM461 interface modules, external CP443-5 Extended DP master interface module and their connecting cables.

Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

#### Procedure

1. Change the hardware configuration offline (see section [STEP 7, step 2: Offline modification of the hardware configuration](Page 293)).

2. Expand and download the organization blocks (see section [STEP 7, step 3: Expanding and downloading OBs](Page 293)).

3. Stop the reserve CPU (see section [STEP 7, step 4: Stopping the reserve CPU](Page 294)).

4. Download the new hardware configuration to the reserve CPU (see section [STEP 7, step 5: Loading a new hardware configuration in the reserve CPU](Page 294)).

5. Proceed as follows to expand the subsystem of the present reserve CPU:
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.
     - or
   - Add a new expansion unit to an existing chain.
     - or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.

6. Switch to CPU with altered configuration (see section [STEP 7, step 6: Switch to CPU with modified configuration](Page 295)).

7. Proceed as follows to expand the subsystem of the original master CPU (currently in STOP mode):
   - Switch off the power supply of the reserve subsystem.
   - Insert the new IM460 into the central unit, then establish the link to a new expansion unit.
     - or
   - Add a new expansion unit to an existing chain.
     - or
   - Plug in the new external DP master interface, and set up a new DP master system.
   - Switch on the power supply of the reserve subsystem again.
8. Change to redundant system mode (see section STEP 7, step 7: Transition to redundant system mode (Page 296))

9. Modify and download the user program (see section STEP 7, step 8: Editing and downloading the user program (Page 297))

17.6 Removing components in STEP 7

Starting situation

You have verified that the CPU parameters (e.g. monitoring times) match the planned new program. Adapt the CPU parameters first, if necessary (see section Editing CPU parameters (Page 308)).

The modules to be removed and their connected sensors and actuators are no longer of any significance to the process being controlled. The fault-tolerant system is operating in redundant system mode.

Procedure

Carry out the steps listed below to remove hardware components from a fault-tolerant system in STEP 7. Details of each step are described in a subsection.

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>See section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Editing the hardware configuration offline</td>
<td>STEP 7, step 1: Editing the hardware configuration offline (Page 301)</td>
</tr>
<tr>
<td>2</td>
<td>Editing and downloading the user program</td>
<td>STEP 7, step 2: Editing and downloading the user program (Page 302)</td>
</tr>
<tr>
<td>3</td>
<td>Stopping the reserve CPU</td>
<td>STEP 7, step 3: Stopping the reserve CPU (Page 302)</td>
</tr>
<tr>
<td>4</td>
<td>Downloading a new hardware configuration to the reserve CPU</td>
<td>STEP 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 303)</td>
</tr>
<tr>
<td>5</td>
<td>Switching to CPU with modified configuration</td>
<td>STEP 7, step 5: Switching to CPU with modified configuration (Page 303)</td>
</tr>
<tr>
<td>6</td>
<td>Transition to redundant system mode</td>
<td>STEP 7, step 6: Transition to redundant system mode (Page 304)</td>
</tr>
<tr>
<td>7</td>
<td>Modification of hardware</td>
<td>STEP 7, step 7: Modification of hardware (Page 305)</td>
</tr>
<tr>
<td>8</td>
<td>Editing and downloading organization blocks</td>
<td>STEP 7, step 8: Editing and downloading organization blocks (Page 306)</td>
</tr>
</tbody>
</table>
Exceptions

This general procedure for system modifications does not apply to removing interface modules (see section Removing interface modules in STEP 7 (Page 306)).

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections STEP 7, step 3: Stopping the reserve CPU (Page 302) to STEP 7, step 6: Transition to redundant system mode (Page 304). The system behavior remains as described.

You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode".

17.6.1 STEP 7, step 1: Editing the hardware configuration offline

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Perform all the modifications to the hardware configuration relating to the hardware being removed offline.
2. Compile the new hardware configuration, but do not load it into the target system just yet.

Result

The modified hardware configuration is in the PG. The target system continues operation with the old configuration in redundant system mode.
17.6 Removing components in STEP 7

17.6.2   STEP 7, step 2: Editing and downloading the user program

Starting situation
The fault-tolerant system is operating in redundant system mode.

Restrictions

<table>
<thead>
<tr>
<th>CAUTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Any attempts to modify the structure of an FB interface or the instance data of an FB in redundant system mode will lead to stop system mode (both CPUs in STOP mode).</td>
</tr>
</tbody>
</table>

Procedure

1. Edit only the program elements related to the hardware removal.
   You can add, edit or remove OBs, FBs, FCs and DBs.
2. Download only the program changes to the target system.

Result
The fault-tolerant system continues to operate in redundant system mode. The modified user program will no longer attempt to access the hardware being removed.

17.6.3   STEP 7, step 3: Stopping the reserve CPU

Starting situation
The fault-tolerant system is operating in redundant system mode. The user program will no longer attempt to access the hardware being removed.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result
The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.
17.6 Removing components in STEP 7

17.6.4 STEP 7, step 4: Downloading a new hardware configuration to the reserve CPU

Starting situation
The fault-tolerant system is operating in single mode.

Procedure
Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

Note
The user program and connection configuration cannot be downloaded in single mode.

Result
The new hardware configuration of the reserve CPU does not yet have an effect on ongoing operation.

17.6.5 STEP 7, step 5: Switching to CPU with modified configuration

Starting situation
The modified hardware configuration is downloaded to the reserve CPU.

Procedure
1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result
The reserve CPU links up, is updated (see section Link-up and update (Page 135)) and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system continues operating in single mode.
### System modifications during operation

#### 17.6 Removing components in STEP 7

### Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of previous master CPU</th>
<th>One-sided I/O of new master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules to be removed¹</td>
<td>are no longer addressed by the CPU.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are no longer addressed by the CPU.</td>
<td>are given new parameter settings² and updated by the CPU.</td>
<td>continue operation without interruption.</td>
</tr>
<tr>
<td>DP stations to be removed</td>
<td>as for I/O modules to be removed (see above)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹) No longer included in the hardware configuration, but still plugged in  
²) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

### Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 149).

### 17.6.6 STEP 7, step 6: Transition to redundant system mode

#### Starting situation

The fault-tolerant system is operating with the new (restricted) hardware configuration in single mode.

#### Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

#### Result

The reserve CPU links up and is updated. The fault-tolerant system is operating in redundant system mode.
Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of reserve CPU</th>
<th>One-sided I/O of master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules to be removed(^1)</td>
<td>are no longer addressed by the CPU.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O modules still present</td>
<td>are given new parameter settings(^2) and updated by the CPU.</td>
<td>continue operation without interruption.</td>
<td></td>
</tr>
<tr>
<td>DP stations to be removed</td>
<td>as for I/O modules to be removed (see above)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1) No longer included in the hardware configuration, but still plugged in
2) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

Reaction to monitoring timeout

If one of the monitored times exceeds the configured maximum, the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the link-up and update later. For additional information, refer to section Time monitoring (Page 149).

17.6.7 STEP 7, step 7: Modification of hardware

Starting situation

The fault-tolerant system is operating with the new hardware configuration in redundant system mode.

Procedure

1. Disconnect all the sensors and actuators from the components you want to remove.
2. Remove the relevant components from the system.
   - Remove the central modules from the rack.
   - Remove the modules from modular DP stations
   - Remove DP stations from DP master systems.

Note

With switched I/O: Always complete all changes on one segment of the redundant DP master system before you modify the next segment.
17.6 Removing components in STEP 7

Result
The removal of non-configured modules does not influence the user program. The same applies to removing DP stations.
The fault-tolerant system continues to operate in redundant system mode.

17.6.8 STEP 7, step 8: Editing and downloading organization blocks

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure
1. Make sure that the interrupt OBs 4x and 82 no longer contain any interrupts of the removed components.
2. Download the modified OBs and the corresponding program elements to the target system.

Result
The fault-tolerant system is operating in redundant system mode.

17.6.9 Removing interface modules in STEP 7

Always switch off the power before you remove the IM460 and IM461 interface modules, external CP 443-5 Extended DP master interface module, and their connecting cables.
Always switch off power to an entire subsystem. To ensure that this does not influence the process, always set the subsystem to STOP before you do so.

Procedure
1. Change the hardware configuration offline (see section STEP 7, step 1: Editing the hardware configuration offline (Page 301))
2. Modify and download the user program (see section STEP 7, step 2: Editing and downloading the user program (Page 302))
3. Stop the reserve CPU (see section STEP 7, step 3: Stopping the reserve CPU (Page 302))
4. Download the new hardware configuration to the reserve CPU (see section STEP 7, step 4: Downloading a new hardware configuration to the reserve CPU (Page 303))
5. Follow the steps below to remove an interface module from the subsystem of the reserve CPU:
   – Switch off the power supply of the reserve subsystem.
   – Remove an IM460 from the central unit.
   or
   – Remove an expansion unit from an existing chain.
   or
   – Remove an external DP master interface module.
   – Switch on the power supply of the reserve subsystem again.

6. Switch to CPU with altered configuration (see section STEP 7, step 5: Switching to CPU with modified configuration (Page 303))

7. Proceed as follows to remove an interface module from the subsystem of the original master CPU (currently in STOP mode):
   – Switch off the power supply of the reserve subsystem.
   – Remove an IM460 from the central unit.
   or
   – Remove an expansion unit from an existing chain.
   or
   – Remove an external DP master interface module.
   – Switch on the power supply of the reserve subsystem again.

8. Change to redundant system mode (see section STEP 7, step 6: Transition to redundant system mode (Page 304))

9. Modify and download the user organization blocks (see section STEP 7, step 8: Editing and downloading organization blocks (Page 306))
17.7  Editing CPU parameters

17.7.1  Editing CPU parameters

Only certain CPU parameters (object properties) can be edited in operation. These are highlighted in the screen forms by blue text. If you have set blue as the color for dialog box text on the Windows Control Panel, the editable parameters are indicated in black characters.

---

**Note**

If you edit any protected parameters, the system will reject any attempt to changeover to the CPU containing those modified parameters. The event W#16#5966 is written to the diagnostic buffer, and you will then have to restore the wrongly changed parameters in the parameter configuration to their last valid values.

---

**Table 17- 1  Modifiable CPU parameters**

<table>
<thead>
<tr>
<th>Tab</th>
<th>Editable parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start-up</td>
<td>Monitoring time for signaling readiness by modules</td>
</tr>
<tr>
<td></td>
<td>Monitoring time for transferring parameters to modules</td>
</tr>
<tr>
<td>Cycle/clock memory</td>
<td>Scan cycle monitoring time</td>
</tr>
<tr>
<td></td>
<td>Cycle load due to communication</td>
</tr>
<tr>
<td></td>
<td>Size of the process image of inputs *)</td>
</tr>
<tr>
<td></td>
<td>Size of the process image of outputs *)</td>
</tr>
<tr>
<td>Memory</td>
<td>Local data for the various priority classes *)</td>
</tr>
<tr>
<td></td>
<td>Communication resources: Maximum number of communication jobs. You may only increase</td>
</tr>
<tr>
<td></td>
<td>the configured value of this parameter *)</td>
</tr>
<tr>
<td>Time-of-day interrupts</td>
<td>&quot;Active&quot; checkbox</td>
</tr>
<tr>
<td>(for each time-of-day</td>
<td>&quot;Execution&quot; list box</td>
</tr>
<tr>
<td>interrupt OB)</td>
<td>Starting date</td>
</tr>
<tr>
<td></td>
<td>Time</td>
</tr>
<tr>
<td>Watchdog interrupt</td>
<td>Execution</td>
</tr>
<tr>
<td>(for each watchdog</td>
<td>Phase offset</td>
</tr>
<tr>
<td>interrupt OB)</td>
<td>Diagnostics/clock</td>
</tr>
<tr>
<td></td>
<td>Security</td>
</tr>
<tr>
<td></td>
<td>Security level and password</td>
</tr>
</tbody>
</table>
System modifications during operation

17.7 Editing CPU parameters

<table>
<thead>
<tr>
<th>Tab</th>
<th>Editable parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>H parameter</td>
<td>Test cycle time</td>
</tr>
<tr>
<td></td>
<td>Maximum cycle time extension</td>
</tr>
<tr>
<td></td>
<td>Maximum communication delay</td>
</tr>
<tr>
<td></td>
<td>Maximum inhibit time for priority classes &gt; 15</td>
</tr>
<tr>
<td></td>
<td>Minimum I/O retention time</td>
</tr>
</tbody>
</table>

*) Modifying these parameters also modifies the memory content.

The selected new values should match both the currently loaded and the planned new user program.

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

To edit the CPU parameters of a fault-tolerant system, follow the steps outlined below. Details of each step are described in a subsection.

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>See section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Editing CPU parameters offline</td>
<td>Step 1: Editing CPU parameters offline (Page 310)</td>
</tr>
<tr>
<td>2</td>
<td>Stopping the reserve CPU</td>
<td>Step 2: Stopping the reserve CPU (Page 310)</td>
</tr>
<tr>
<td>3</td>
<td>Downloading modified CPU parameters to the reserve CPU</td>
<td>Step 3: Downloading a new hardware configuration to the reserve CPU (Page 311)</td>
</tr>
<tr>
<td>4</td>
<td>Switching to CPU with modified configuration</td>
<td>Step 4: Switching to CPU with modified configuration (Page 311)</td>
</tr>
<tr>
<td>5</td>
<td>Transition to redundant system mode</td>
<td>Step 5: Transition to redundant system mode (Page 312)</td>
</tr>
</tbody>
</table>

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections Step 2: Stopping the reserve CPU (Page 310) to Step 5: Transition to redundant system mode (Page 312). The system behavior remains as described.

You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode". You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode".
17.7 Editing CPU parameters

17.7.2 Step 1: Editing CPU parameters offline

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure
1. Edit the relevant CPU properties offline in HW Config.
2. Compile the new hardware configuration, but do not load it into the target system just yet.

Result
The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.

17.7.3 Step 2: Stopping the reserve CPU

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure
1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result
The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.
17.7.4 Step 3: Downloading a new hardware configuration to the reserve CPU

Starting situation
The fault-tolerant system is operating in single mode.

Procedure
Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

Note
The user program and connection configuration cannot be downloaded in single mode.

Result
The modified CPU parameters in the new hardware configuration of the standby CPU do not yet have an effect on ongoing operation.

17.7.5 Step 4: Switching to CPU with modified configuration

Starting situation
The modified hardware configuration is downloaded to the reserve CPU.

Procedure
1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result
The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system continues operating in single mode.
17.7 Editing CPU parameters

**Reaction of the I/O**

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of previous master CPU</th>
<th>One-sided I/O of new master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules</td>
<td>are no longer addressed by the CPU. Output modules output the configured substitute or holding values.</td>
<td>are given new parameter settings¹ and updated by the CPU.</td>
<td>continue operation without interruption.</td>
</tr>
</tbody>
</table>

¹) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).

**Reaction to monitoring timeout**

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 149).

Where the values for the monitoring times in the CPUs differ, the higher values always apply.

**17.7.6 Step 5: Transition to redundant system mode**

**Starting situation**

The fault-tolerant system operates with the modified CPU parameters in single mode.

**Procedure**

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

**Result**

The reserve CPU links up and is updated. The fault-tolerant system is operating in redundant system mode.
17.8 Changing the CPU memory configuration

17.8.1 Changing the CPU memory configuration

The redundant system state is only possible if both CPUs have the same memory configuration. For this the following condition must be met:

- The size and type of load memory (RAM or FLASH) on both CPUs must match.

The memory configuration of the CPUs can be modified in operation. Possible modifications of S7-400H memory:

- Expanding load memory
- Changing the type of load memory

17.8.2 Expanding load memory

The following methods of memory expansion are possible:

- Upgrade the load memory by inserting a memory card with more memory space
- Upgrade the load memory by inserting a RAM card, if no memory card was previously inserted

If you change memory in this way, the entire user program is copied from the master CPU to the reserve CPU during the link-up process (see section Update sequence (Page 143)).
17.8 Changing the CPU memory configuration

Restrictions

Memory should preferably be expanded using RAM cards, because this will ensure that the user program is copied to load memory of the reserve CPU in the link-up process.

In principle, it is also possible to use FLASH Cards to expand load memory. However, it is then your responsibility to download the entire user program and the hardware configuration to the new FLASH Card (see procedure in section Changing the type of load memory (Page 314)).

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

Proceed as follows in the specified sequence:

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Switch the reserve CPU to STOP using the</td>
<td>The system is now operating in single mode.</td>
</tr>
<tr>
<td></td>
<td>programming device.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Replace the memory card in the CPU with a card</td>
<td>Reserve CPU requests memory reset.</td>
</tr>
<tr>
<td></td>
<td>which has the required (higher) capacity.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reset the reserve CPU using the programming</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>device.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Start the reserve CPU with the menu command &quot;PLC</td>
<td>• The reserve CPU links up, is updated and becomes the master.</td>
</tr>
<tr>
<td></td>
<td>&gt; Mode &gt; Switch to CPU ... with expanded memory</td>
<td>• Previous master CPU changes to STOP.</td>
</tr>
<tr>
<td></td>
<td>configuration&quot;.</td>
<td>• System operates in single mode.</td>
</tr>
<tr>
<td>5</td>
<td>Turn off power to the second CPU.</td>
<td>The subsystem is disabled.</td>
</tr>
<tr>
<td>6</td>
<td>Modify the memory configuration of the second</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CPU as you did in steps 2 to 3 for the first CPU.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Start the second CPU with the menu command &quot;PLC</td>
<td>• The second CPU is linked up and updated.</td>
</tr>
<tr>
<td></td>
<td>&gt; Mode &gt; Switch to CPU ... with expanded memory</td>
<td>• The system is now operating again in redundant system mode.</td>
</tr>
<tr>
<td></td>
<td>configuration&quot;.</td>
<td></td>
</tr>
</tbody>
</table>

17.8.3 Changing the type of load memory

The following types of memory cards are available for load memory:

- RAM card for the test and commissioning phase
- FLASH Card for permanent storage of the completed user program

The size of the new memory card is irrelevant here.

If you change your memory configuration in this way, the system does not transfer any program parts from the master CPU to the reserve CPU. Instead, it transfers only the
System modifications during operation

17.8 Changing the CPU memory configuration

Contents of the unchanged blocks of the user program (see section Switch to CPU with modified configuration or expanded memory configuration [Page 146]).

It is your responsibility to download the entire user program to the new load memory.

Note

After reloading connections/gateways, it is no longer possible to change from a RAM card to a FLASH card.

Starting situation

The fault-tolerant system is operating in redundant system mode.

The current status of the user program is available on the PG/ES as a STEP 7 project in block format.

⚠️ CAUTION

You cannot deploy a user program you uploaded from the target system here.

It is not permissible to recompile the user program from an STL source file, because this action would set a new time stamp at all blocks and so prevent the block contents from being copied when there is a master-reserve changeover.

Procedure

Proceed as follows in the specified sequence:

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Switch the reserve CPU to STOP using the programming device.</td>
<td>The system is now operating in single mode.</td>
</tr>
<tr>
<td>2</td>
<td>Replace the existing memory card in the reserve CPU with a new one of the required type.</td>
<td>Reserve CPU requests memory reset.</td>
</tr>
<tr>
<td>3</td>
<td>Reset the reserve CPU using the programming device.</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>Download the program data to the reserve CPU in STEP 7 by selecting the &quot;Download User Program to Memory Card&quot; command. Notice: Select the correct CPU from the selection dialog.</td>
<td>–</td>
</tr>
<tr>
<td>5</td>
<td>Start the reserve CPU with the menu command &quot;PLC &gt; Mode &gt; Switching to CPU with modified configuration&quot;.</td>
<td>• The reserve CPU links up, is updated and becomes the master. • Previous master CPU changes to STOP. • System operates in single mode.</td>
</tr>
<tr>
<td>6</td>
<td>Modify the memory configuration of the second CPU as you did for the first CPU in step 2.</td>
<td>–</td>
</tr>
</tbody>
</table>
### System modifications during operation

#### 17.8 Changing the CPU memory configuration

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>How does the system react?</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Download the user program and the hardware configuration to the second CPU.</td>
<td>–</td>
</tr>
</tbody>
</table>
| 8    | Start the second CPU from the PG. | • The second CPU is linked up and updated.  
• The system is now operating again in redundant system mode. |

**Note**

If you want to change to FLASH Cards, you can load them with the user program and hardware configuration in advance without inserting them in the CPU. Steps 4 and 7 can then be omitted. However, the memory cards in both CPUs must be loaded in the same sequence. Changing the order of blocks in the load memories will lead to termination of the link-up process.

**Writing to a FLASH Card in the fault-tolerant system**

You can always write to a FLASH Card while the fault-tolerant system is in RUN, without having to stop the fault-tolerant system. This is, however, only possible if the online data of the hardware configuration and the user program in both CPUs and the corresponding offline data in your engineering station match.

**Inserting the Flash card**

Proceed as follows:

1. Set the reserve CPU to STOP and insert the FLASH Card into the CPU.
2. Reset the CPU using STEP 7.
3. Download the program data with the STEP 7 "Download User Program to Memory Card" command. Note: Select the correct CPU from the selection dialog.
4. Switch to the CPU with the changed configuration using the "Operating Mode" dialog. This changes over the master/reserve roles; the CPU with the Flash Card is now the master CPU. The reserve CPU is now in STOP.
5. Next, insert the Flash Card in the CPU that is in STOP. Reset the CPU using STEP 7.
6. Carry out step 4: Download the program data with the STEP 7 "Download User Program to Memory Card" command. Note: Select the correct CPU from the selection dialog.
7. Execute a warm restart of the reserve CPU using the "Operating Mode" dialog. The system status now changes to "Redundant" mode.
Removing the FLASH card

The online and offline data consistency described earlier also applies when you remove FLASH Cards from a fault-tolerant system. In addition, the available RAM size must not be less than the actual size of the STEP 7 program (STEP 7 Program > Block Container > "Blocks" Properties).

1. Set the reserve CPU to STOP and remove the FLASH Card. Adapt the memory configuration as required.
2. Reset the CPU using STEP 7.
3. Download the block container using STEP 7.
4. Switch to the CPU with the changed configuration using the "Operating Mode" dialog.
5. Remove the FLASH Card from the CPU which is now in STOP. Adapt the RAM configuration as required, and then perform a CPU memory reset.
6. Execute a warm restart of the reserve CPU using the "Operating Mode" dialog. The system status now changes to "Redundant" mode.

17.9 Re-parameterization of a module

17.9.1 Re-parameterization of a module

Refer to the information text in the "Hardware Catalog" window to determine which modules (signal modules and function modules) can be reconfigured during ongoing operation. The specific reactions of individual modules are described in the respective technical documentation.

---

**Note**

If you edit any protected parameters, the system will reject any attempt to changeover to the CPU containing those modified parameters. The event W#16#5966 is written to the diagnostic buffer, and you will then have to restore the wrongly changed parameters in the parameter configuration to their last valid values.

---

The selected new values must match the current and the planned user program.

**Starting situation**

The fault-tolerant system is operating in redundant system mode.
17.9 Re-parameterization of a module

Procedure

To edit the parameters of modules in a fault-tolerant system, perform the steps outlined below. Details of each step are described in a subsection.

<table>
<thead>
<tr>
<th>Step</th>
<th>What to do?</th>
<th>See section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Editing parameters offline</td>
<td>Step 1: Editing parameters offline (Page 318)</td>
</tr>
<tr>
<td>2</td>
<td>Stopping the reserve CPU</td>
<td>Step 2: Stopping the reserve CPU (Page 319)</td>
</tr>
<tr>
<td>3</td>
<td>Downloading modified CPU parameters to the reserve CPU</td>
<td>Step 3: Downloading a new hardware configuration to the reserve CPU (Page 319)</td>
</tr>
<tr>
<td>4</td>
<td>Switching to CPU with modified configuration</td>
<td>Step 4: Switching to CPU with modified configuration (Page 320)</td>
</tr>
<tr>
<td>5</td>
<td>Transition to redundant system mode</td>
<td>Step 5: Transition to redundant system mode (Page 321)</td>
</tr>
</tbody>
</table>

Note

After changing the hardware configuration, download takes place practically automatically. This means that you no longer need to perform the steps described in sections Step 2: Stopping the reserve CPU (Page 319) to Step 5: Transition to redundant system mode (Page 321). The system behavior remains as described.

You will find more information in the HW Config online help "Download to module -> Download station configuration in RUN mode".

17.9.2 Step 1: Editing parameters offline

Starting situation

The fault-tolerant system is operating in redundant system mode.

Procedure

1. Edit the module parameters offline in HW Config.
2. Compile the new hardware configuration, but do not load it into the target system just yet.

Result

The modified hardware configuration is in the PG/ES. The target system continues operation with the old configuration in redundant system mode.
17.9.3 Step 2: Stopping the reserve CPU

Starting situation
The fault-tolerant system is operating in redundant system mode.

Procedure
1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, select the reserve CPU, then click "Stop".

Result
The reserve CPU switches to STOP mode, the master CPU remains in RUN mode, the fault-tolerant system works in single mode. The one-sided I/O of the reserve CPU is no longer addressed.

17.9.4 Step 3: Downloading a new hardware configuration to the reserve CPU

Starting situation
The fault-tolerant system is operating in single mode.

Procedure
Load the compiled hardware configuration in the reserve CPU that is in STOP mode.

Note
The user program and connection configuration cannot be downloaded in single mode.

Result
The modified parameters in the new hardware configuration of the reserve CPU do not yet have an effect on ongoing operation.
17.9.5 Step 4: Switching to CPU with modified configuration

Starting situation

The modified hardware configuration is downloaded to the reserve CPU.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.
2. In the "Operating Mode" dialog box, click the "Switch to..." button.
3. In the "Switch" dialog box, select the "with altered configuration" option and click the "Switch" button.
4. Acknowledge the prompt for confirmation with "OK".

Result

The reserve CPU links up, is updated and becomes the master. The previous master CPU switches to STOP mode, the fault-tolerant system continues operating in single mode.

Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of previous master CPU</th>
<th>One-sided I/O of new master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules</td>
<td>are no longer addressed by the CPU. Output modules output the configured substitute or holding values.</td>
<td>are given new parameter settings and updated by the CPU.</td>
<td>continue operation without interruption.</td>
</tr>
<tr>
<td>1) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reaction to monitoring timeout

The update is canceled and no change of master takes place if one of the monitored times exceeds the configured maximum. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the master changeover later. For additional information, refer to section Time monitoring (Page 149).

Where the values for the monitoring times in the CPUs differ, the higher values always apply.
17.9 Re-parameterization of a module

Calling OB 83

After transferring the parameter data records to the desired modules, OB 83 is called. The sequence is as follows:

1. After you have made the parameter changes to a module in STEP 7 and loaded them in RUN in the CPU, the OB 83 is started (trigger event W#16#3367). Relevant in the OB start information are the logical start address (OB83_MDL_ADDR) and the module type (OB83_MDL_TYPE). From now on, the input and/or output data of the module might no longer be correct, and no SFCs that send data records to this module may be active.

2. After termination of OB 83, the parameters of the module are reset.

3. After termination of the parameter reset operation, the OB 83 is started again (trigger event W#16#3267 if the parameterization was successful, or W#16#3968 if it was unsuccessful). The input and output data of the module is the same as after an insertion interrupt, meaning that under certain circumstances may not yet be correct. With immediate effect, you can again call SFCs that send data records to the module.

17.9.6 Step 5: Transition to redundant system mode

Starting situation

The fault-tolerant system operates with the modified parameters in single mode.

Procedure

1. In SIMATIC Manager, select a CPU of the fault-tolerant system, then choose "PLC > Operating Mode" from the menu.

2. From the "Operating Mode" dialog box, select the reserve CPU, then click "Warm Restart".

Result

The reserve CPU links up and is updated. The fault-tolerant system is operating in redundant system mode.

Reaction of the I/O

<table>
<thead>
<tr>
<th>Type of I/O</th>
<th>One-sided I/O of reserve CPU</th>
<th>One-sided I/O of master CPU</th>
<th>Switched I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O modules</td>
<td>are given new parameter settings and updated by the CPU.</td>
<td>continue operation without interruption.</td>
<td></td>
</tr>
</tbody>
</table>

1) Central modules are first reset. Output modules briefly output 0 during this time (instead of the configured substitute or hold values).
17.9 Re-parameterization of a module

**Reaction to monitoring timeout**

If one of the monitored times exceeds the configured maximum the update is canceled. The fault-tolerant system remains in single mode with the previous master CPU and, assuming certain conditions are met, attempts the link-up and update later. For additional information, refer to section [Time monitoring](Page 149).

If the values for the monitoring times in the CPUs differ, the higher values apply.
18.1 Synchronization modules for S7–400H

Function of the synchronization modules

Synchronization modules are used for communication between two redundant S7-400H CPUs. You require two synchronization modules per CPU, connected in pairs by fiber-optic cable.

The system supports hot-swapping of synchronization modules, and so allows you to influence the repair response of the fault-tolerant systems and to control the failure of the redundant connection without stopping the plant.

The diagnostics process for synchronization modules is based in parts on the maintenance concept familiar from PROFINET. As of firmware version 6.0.4 of CPU, maintenance required is no longer reported.

If you remove a synchronization module in redundant system mode, there is a loss of synchronization. The reserve CPU changes to ERROR-SEARCH mode for some minutes. If the new synchronization module is inserted and the redundant link is reestablished during this time, the reserve CPU switches to redundant system mode, otherwise it switches to STOP.

Once you have inserted the new synchronization module and reestablished the redundant link, you must restart the reserve CPU.

Distance between the S7–400H CPUs

Two types of synchronization module are available:

<table>
<thead>
<tr>
<th>Order number</th>
<th>Maximum distance between the CPUs</th>
</tr>
</thead>
<tbody>
<tr>
<td>6ES7 960–1AA06–0X0A0</td>
<td>10 m</td>
</tr>
<tr>
<td>6ES7 960–1AB06–0X0A0</td>
<td>10 km</td>
</tr>
</tbody>
</table>

Long synchronization cables may increase cycle times. This extension can have the factor 2 - 5 with a cable length of 10 km.

Note

A fault-tolerant system requires 4 synchronization modules of the same type.
Synchronization modules

18.1 Synchronization modules for S7–400H

Mechanical configuration

![Diagram of Synchronization Module]

① Dummy plugs

Figure 18-1  Synchronization module

**CAUTION**

**Class 1 laser product**

Risk of injury.

The synchronization module is equipped with a laser system and is classified as a "CLASS 1 LASER PRODUCT" according to IEC 60825–1.

Avoid direct contact with the laser beam. Do not open the housing. Always observe the information provided in this manual, and keep the manual to hand as a reference.
OB 84

If the CPU was configured as V 4.5: In case of a reduced performance in the redundant link between the two CPUs in redundant system mode, the CPU's operating system calls OB 84.

The event "Reduced performance of the redundancy link" in the configuration as V4.5 corresponds to the event "Functional error of network component" in case of a configuration as V6.0. OB 82 is called in case of a configuration as V6.0.

You can determine the detail diagnostics by means of SFB52 or SFB54 in case of a configuration as V6.0.

In solo mode and in stand-alone operation the error identifier 0x3592 points to an error in a synchronization component. This error has no effect on the functionality of the CPU in Solo mode or in stand-alone operation. However, redundant mode is no longer possible. To exchange the CPU in Solo mode, perform a master change with the function "Switch over to CPU in rack .. via only one intact redundant link".

OB 82

When operating in redundant system mode, the CPU's operating system calls OB 82 if it detects a reduced performance in the redundant link between the two CPUs.

If OB 82 was called, you can only determine the cause later if the data were read out with SFB 52 or SFB 54.

The cause for this reduced performance can be found in the "Sync module diagnostics" tab in HW Config -> PLC -> Module state. For the selected synchronization module, you can display here the following channel-specific diagnostics data:

- Overtemperature
  The synchronization module is too hot.

- Fiber-optic error
  The sender of the electro-optical component has reached the end of its service life.

- Violation of lower limit
  The sent or received optical performance is low or too low.

- Violation of upper limit
  The sent or received optical performance is high or too high.

- Functional error of the network component
  The quality of the redundancy link between the CPUs (transmission distance including synchronization modules and fiber-optic cables) is reduced so that transmission errors are occurring frequently.

In redundant mode the OB82 is also called at Power Off/On or at a firmware update of the partner CPU. This does not indicate any problem with the synchronization link but is instead due to the fact that the synchronization modules are not emitting any light at this moment.
Fiber-optic interfaces of unused modules

Fiber-optic interfaces of unused modules must be blanked off during storage to protect the optical equipment. The plugs are in the synchronization module when shipped.

<table>
<thead>
<tr>
<th>NOTICE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Reduced optical performance due to soiling</strong></td>
</tr>
<tr>
<td>Even small amounts of dirt in a fiber-optic interface adversely affect the quality of the signal transmission. This can lead to synchronization losses during operation. Protect the fiber-optic interfaces against dirt during storage and installation of the synchronization modules.</td>
</tr>
</tbody>
</table>

Wiring and inserting the synchronization module

1. Remove the dummy plug of the synchronization module.
2. Fold back the clip completely against the synchronization module.
3. Insert the synchronization module into the IF1 interface of the first fault-tolerant CPU until it snaps into place.
4. Insert the end of the fiber-optic cable into the synchronization module until it snaps into place.
5. Repeat steps 1 to 4 for the second synchronization module.
6. Repeat the process for the second fault-tolerant CPU.

   Connect the IF1 interface of the first CPU with the IF1 interface of the second CPU and the IF2 interface of the first CPU with the IF2 interface of the second CPU.

**Note**

**Wiring synchronization modules crosswise**

If you wire synchronization modules crosswise, i.e. the IF1 interface of the first CPU with the IF2 interface of the second CPU and vice versa, the two CPUs take over the master role and the system will now function properly. The LEDs IFM 1 and IFM 2 are lit on both CPUs.

Make sure that you connect the IF1 interface of the first CPU with the IF1 interface of the second CPU and the IF2 interface of the first CPU with the IF2 interface of the second CPU.

Removing the synchronization module

1. Slightly press the release of the fiber-optic cable and remove it from the synchronization module.
2. Fold the clip of the synchronization module to the front and remove the synchronization module from the fault-tolerant CPU interface.
3. Place the dummy plug on the synchronization module.
4. Repeat this procedure for all interfaces and both fault-tolerant CPUs.
Technical data

<table>
<thead>
<tr>
<th>Technical data</th>
<th>6ES7 960–1AA05–0XA0</th>
<th>6ES7 960–1AB05–0XA0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum distance between the CPUs</td>
<td>10 m</td>
<td>10 km</td>
</tr>
<tr>
<td>Power supply</td>
<td>3.3 V, supplied by the CPU</td>
<td>3.3 V, supplied by the CPU</td>
</tr>
<tr>
<td>Current consumption</td>
<td>220 mA</td>
<td>240 mA</td>
</tr>
<tr>
<td>Power loss</td>
<td>0.77 W</td>
<td>0.83 W</td>
</tr>
<tr>
<td>Wavelength of the optical transceivers</td>
<td>850 nm</td>
<td>1310 nm</td>
</tr>
<tr>
<td>Maximal permitted attenuation of the fiber-optic cable</td>
<td>7.5 dB</td>
<td>9.5 dB</td>
</tr>
<tr>
<td>Maximum permitted difference in cable lengths</td>
<td>9 m</td>
<td>50 m</td>
</tr>
<tr>
<td>Dimensions W x H x D (mm)</td>
<td>13 x 14 x 58</td>
<td>13 x 14 x 58</td>
</tr>
<tr>
<td>Weight</td>
<td>0.014 kg</td>
<td>0.014 kg</td>
</tr>
</tbody>
</table>

See also

Installation of fiber-optic cables (Page 327)

18.2 Installation of fiber-optic cables

Introduction

Fiber-optic cables may only be installed by trained and qualified personnel. Always observe the applicable rules and statutory regulations. The installation must be carried out with meticulous care, because faulty installations represent the most common source of error. Causes are:

- Kinking of the fiber-optic cable due to an insufficient bending radius.
- Crushing of the cable as a result of excess forces caused by persons treading on the cable, or by pinching, or by the load of other heavy cables.
- Overstretching due to high tensile forces.
- Damage on sharp edges etc.

Permitted bending radius for prefabricated cables

The following bending radii must not be undershot when installation the cable (6ES7960–1AA04–5xA0) prefabricated by SIEMENS.

- During installation: 88 mm (repeated)
- After installation: 59 mm (one-time)
Synchronization modules

18.2 Installation of fiber-optic cables

Permitted bending radii for prefabricated cables

When you install self-assembled cable make sure to comply with the bending radii specified by the manufacturer. Note that approx. 50 mm of space is available for the connector and the fiber-optic cable under the front over of the CPU and that no tight bending radius of a fiber-optic cable is therefore possible in the proximity of the connector.

Points to observe when installing the fiber-optic cables for the S7-400H synchronization link

Always route the two fiber-optic cables separately. This increases availability and protects the fiber-optic cables from potential double errors caused, for example, by interrupting both cables at the same time.

Always make sure the fiber-optic cables are connected to both CPUs before switching on the power supply or the system, otherwise the CPUs may process the user program as the master CPU.

Local quality assurance

Check the points outlined below before you install the fiber-optic cables:

- Does the delivered package contain the correct fiber-optic cables?
- Any visible transport damage to the product?
- Have you organized a suitable intermediate on-site storage for the fiber-optic cables?
- Does the category of the cables match the connecting components?

Check the attenuation of the fiber-optic cables after installation.

Storage of the fiber-optic cables

if you do not install the fiber-optic cable immediately after you received the package, it is advisable to store it in a dry location where it is protected from mechanical and thermal influences. Observe the permitted storage temperatures specified in the data sheet of the fiber-optic cable. You should not remove the fiber-optic cables from the original packaging until you are going to install them.

NOTICE

Reduced optical performance due to dirt

Even slight amounts of dirt at the end of a fiber-optic cable will adversely affect its optical performance and thus the quality of the signal transmission. This can lead to synchronization losses during operation. Protect the ends of the fiber-optic cables against dirt during storing and installation. If the ends of the fiber-optic cable are covered when delivered, do not remove these covers.
Open installation, wall breakthroughs, cable ducts:

Note the points outlined below when you install fiber-optic cables:

- The fiber-optic cables may be installed in open locations, provided you can safely exclude any damage in those areas (vertical risers, connecting shafts, telecommunications switchboard rooms, etc.).
- Fiber-optic cables should be mounted on mounting rails (cable trays, wire mesh ducts) using cable ties. Take care not to crush the cable when you fasten it (see Pressure).
- Always deburr or round the edges of the breakthrough before you install the fiber-optic cable, in order to prevent damage to the sheathing when you pull in and fasten the cable.
- The bending radii must not be smaller than the value specified in the manufacturer’s data sheet.
- The branching radii of the cable ducts must correspond to the specified bending radius of the fiber-optic cable.

Cable pull-in

Note the points below when pulling-in fiber-optic cables:

- Always observe the information on pull forces in the data sheet of the corresponding fiber-optic cable.
- Do not reel off any greater lengths when you pull in the cables.
- Install the fiber-optic cable directly from the cable drum wherever possible.
- Do not spool the fiber-optic cable sideways off the drum flange (risk of twisting).
- You should use a cable pulling sleeve to pull in the fiber-optic cable.
- Always observe the specified bending radii.
- Do not use any grease or oil-based lubricants.
  You may use the lubricants listed below to support the pulling-in of fiber-optic cables.
  - Yellow compound (Wire-Pulling, lubricant from Klein Tools; 51000)
  - Soft soap
  - Dishwashing liquid
  - Talcum powder
  - Detergent

Pressure

Do not exert any pressure on the cable, for example, by the inappropriate use of clamps (cable quick-mount) or cable ties. Your installation should also prevent anyone from stepping onto the cable.

Influence of heat

Fiber-optic cables are highly sensitive to direct heat, which means the cables must not be worked on using hot-air guns or gas burners as used in heat-shrink tubing technology.
18.3 Selecting fiber-optic cables

Check or make allowance for the following conditions and situations when selecting a suitable fiber-optic cable:

- Required cable lengths
- Indoor or outdoor installation
- Any particular protection against mechanical stress required?
- Any particular protection against rodents required?
- Can an outside cable be routed directly underground?
- Does the fiber-optic cable need to be water-proof?
- Which temperatures influence the installed fiber-optic cable?

Cable length up to 10 m

The synchronization module 6ES7 960–1AA06–0XA0 can be operated in pairs with fiber-optic cables up to a length of 10 m.

Select cables with the following specification for lengths up to 10 m:

- Multimode fiber 50/125 µ or 62.5/125 µ
- Patch cable for indoor applications
- 2 x duplex cables per fault-tolerant system, cross-over
- Connector type LC–LC

Such cables are available in the following length as accessories for fault-tolerant systems:

Table 18-1 Accessory fiber-optic cable

<table>
<thead>
<tr>
<th>Length</th>
<th>Order number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 m</td>
<td>6ES7960–1AA04–5AA0</td>
</tr>
<tr>
<td>2 m</td>
<td>6ES7960–1AA04–5BA0</td>
</tr>
<tr>
<td>10 m</td>
<td>6ES7960–1AA04–5KA0</td>
</tr>
</tbody>
</table>
Cable length up to 10 km

The synchronization module 6ES7 960-1AB06-0XA0 can be operated in pairs with fiber-optic cables up to a length of 10 km.

The following rules apply:

- Make sure of adequate strain relief on the modules if you use fiber-optic cables longer than 10 m.
- Keep to the specified environmental conditions of the fiber-optic cables used (bending radii, pressure, temperature...)
- Observe the technical specifications of the fiber-optic cable (attenuation, bandwidth...)

Fiber-optic cables with lengths above 10 m usually have to be custom-made. First, select the following specification:

- Single-mode fiber (mono-mode fiber) 9/125 µ

In exceptional situations, you may also use the lengths up to 10 m available as accessories for short distances when testing and commissioning. However, only the use of specified cables with single-mode fibers is allowed for continuous operation.

Note

Cable up to 10 m length on the synchronization module 6ES7 960-1AB06-0XA0

Cables up to a length of 10 m are available on order as accessories. If you use one of these cables on the synchronization module 6ES7 960-1AB06-0XA0, you may see the error message "Optical performance too high" at the call of OB 82.

The table below shows the further specifications, based on your application:

<table>
<thead>
<tr>
<th>Cabling</th>
<th>Components required</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>The entire cabling is routed within a building</td>
<td>Patch cables</td>
<td>2 x duplex cables per system</td>
</tr>
<tr>
<td>No cable junction is required between the indoor and outdoor area</td>
<td></td>
<td>Connector type LC–LC</td>
</tr>
<tr>
<td>The necessary cable length is available in one piece.</td>
<td></td>
<td>Crossed cores</td>
</tr>
<tr>
<td>There is no need to connect several cable segments by means of distribution boxes.</td>
<td></td>
<td>Further specifications you may need to observe for your plant, e.g.:</td>
</tr>
<tr>
<td>Convenient and complete installation using patch cables</td>
<td></td>
<td>UL approval</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Halogen-free materials</td>
</tr>
<tr>
<td>Assembled patch cable</td>
<td></td>
<td>Multicore cables, 4 cores per system</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Connector type LC–LC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Crossed cores</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Further specifications you may need to observe for your plant, e.g.:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UL approval</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Halogen-free materials</td>
</tr>
</tbody>
</table>
## 18.3 Selecting fiber-optic cables

<table>
<thead>
<tr>
<th>Cabling</th>
<th>Components required</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>The entire cabling is routed within a building</td>
<td>including patch cables for indoor applications as required</td>
<td>1 cable with 4 cores per fault-tolerant system</td>
</tr>
<tr>
<td>No cable junction is required between the indoor and outdoor area</td>
<td></td>
<td>Both interfaces in one cable</td>
</tr>
<tr>
<td>The necessary cable length is available in one piece.</td>
<td></td>
<td>1 or 2 cables with several shared cores</td>
</tr>
<tr>
<td>There is no need to connect several cable segments by means of distribution boxes.</td>
<td></td>
<td>Separate installation of the interfaces in order to increase availability (reduction of common cause factor)</td>
</tr>
<tr>
<td>Convenient and complete installation using patch cables</td>
<td></td>
<td>Connector type ST or SC, for example, to match other components; see below</td>
</tr>
<tr>
<td></td>
<td>Patch cable for indoor applications</td>
<td>Further specifications you may need to observe for your plant:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UL approval</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Halogen-free materials</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Avoid splicing cables in the field. Use prefabricated cables with pulling protection/aids in whiplash or breakout design, including measuring log.</td>
</tr>
<tr>
<td>Installation using distribution boxes, see Fig. 18-2</td>
<td>One distribution/junction box per branch</td>
<td>Connector type LC on ST or SC, for example, to match other components</td>
</tr>
<tr>
<td></td>
<td>Installation and patch cables are connected via the distribution box. Either ST or SC plug-in connections can be used, for example. Check the cross-over installation when you wire the CPUs.</td>
<td>Connector type ST or SC, for example, to match other components.</td>
</tr>
</tbody>
</table>
## 18.3 Selecting fiber-optic cables

### Table 18-3 Specification of fiber-optic cables for outdoor applications

<table>
<thead>
<tr>
<th>Cabling</th>
<th>Components required</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>A cable junction is required between the indoor and outdoor area. See Figure 18-2.</td>
<td>- Installation cables for outdoor applications</td>
<td>- Installation cables for outdoor applications</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 1 cable with 4 cores per fault-tolerant system</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Both interfaces in one cable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 1 or 2 cables with several shared cores</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Separate installation of the interfaces in order to increase availability (reduction of common cause factor)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connector type ST or SC, for example, to match other components; see below</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Further specifications you may need to observe for your plant:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- UL approval</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Halogen-free materials</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Further specifications you may need to observe for your plant:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Protection against increased mechanical stress</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Protection against rodents</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Water-proofing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Suitable for direct underground installation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Suitable for the given temperature ranges</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Avoid splicing cables in the field. Use prefabricated cables with pulling protection/aids in whiplash design, including measuring log.</td>
</tr>
<tr>
<td></td>
<td>- including patch cables for indoor applications as required</td>
<td>- 1 cable with 4 cores per fault-tolerant system</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Both interfaces in one cable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 1 or 2 cables with several shared cores</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Separate installation of the interfaces in order to increase availability (reduction of common cause factor)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connector type ST or SC, for example, to match other components; see below</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Further specifications you may need to observe for your plant:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- UL approval</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Halogen-free materials</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Avoid splicing cables in the field. Use prefabricated cables with pulling protection/aids in whiplash or breakout design, including measuring log.</td>
</tr>
<tr>
<td></td>
<td>- Patch cable for indoor applications</td>
<td>- Connector type LC on ST or SC, for example, to match other components</td>
</tr>
</tbody>
</table>
### 18.3 Selecting fiber-optic cables

<table>
<thead>
<tr>
<th>Cabling</th>
<th>Components required</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>A cable junction is required between the indoor and outdoor area</td>
<td>• One distribution/junction box per branch</td>
<td>• Connector type ST or SC, for example, to match other components</td>
</tr>
<tr>
<td>see Figure 18-2</td>
<td>Installation and patch cables are connected via the distribution box. Either ST or SC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>plug-in connections can be used, for example</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Check the cross-over installation when you wire the CPUs.</td>
<td></td>
</tr>
</tbody>
</table>

Figure 18-2  Fiber-optic cables, installation using distribution boxes

S7-400 with CPU 414-4H
rack 0

Further distribution boxes, for example with SC or ST plug and socket connectors, in order to increase total lengths by interconnecting the single segments.

Patch cable (duplex), e.g. LC - SC/ST

S7-400 with CPU 414-4H
rack 1

max. 10 km installation cable (indoor/outdoor)

Distribution box, e.g. with SC or ST plug and socket connectors

Distribution box, e.g. with SC or ST plug and socket connectors

Patch cable (duplex), e.g. LC - SC/ST
S7–400 cycle and response times

This section describes the decisive factors in the cycle and response times of your S7-400 station.

You can read out the cycle time of the user program from the relevant CPU using the programming device (refer to the manual Configuring Hardware and Connections with STEP 7).

The examples included show you how to calculate the cycle time.

An important aspect of a process is its response time. How to calculate this factor is described in detail in this section. When operating a CPU 41x-H as master on the PROFIBUS DP network, you also need to include the additional DP cycle times in your calculation (see section Response time (Page 347)).

Additional information

For more detailed information on the following execution times, refer to the S7–400H instruction list. This lists all the STEP 7 instructions that can be executed by the particular CPUs along with their execution times and all the SFCs/SFBs integrated in the CPUs and the IEC functions that can be called in STEP 7 with their execution times.

19.1 Cycle time

This section describes the decisive factors in the cycle time, and how to calculate it.

Definition of cycle time

The cycle time is the time the operating system requires to execute a program, i.e. to execute OB 1, including all interrupt times required by program parts and for system activities.

This time is monitored.

Time slice model

Cyclic program processing, and therefore also user program processing, is based on time slices. To demonstrate the processes, let us presume a global time slice length of exactly 1 ms.

Process image

During cyclic program processing, the CPU requires a consistent image of the process signals. To ensure this, the process signals are read/written prior to program execution. Subsequently, during program processing the CPU does not access the signal modules.
directly when addressing the input (I) and output (O) address areas, but rather it accesses the CPU's internal memory area containing the I/O process image.

Sequence of cyclic program processing

The table below shows the various phases in cyclic program execution.

Table 19-1  Cyclic program processing

<table>
<thead>
<tr>
<th>Step</th>
<th>Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The operating system initiates the scan cycle monitoring time.</td>
</tr>
<tr>
<td>2</td>
<td>The CPU copies the values from the process output images to the output modules.</td>
</tr>
<tr>
<td>3</td>
<td>The CPU reads the status of inputs of the input modules, and then updates the process image of the inputs.</td>
</tr>
<tr>
<td>4</td>
<td>The CPU processes the user program in time slices and executes the instructions specified in the program.</td>
</tr>
<tr>
<td>5</td>
<td>At the end of a cycle, the operating system executes pending tasks, e.g. loading and deleting of blocks.</td>
</tr>
<tr>
<td>6</td>
<td>Finally, on expiration of any given minimum cycle time, the CPU returns to the start of the cycle and restarts cycle monitoring.</td>
</tr>
</tbody>
</table>

Elements of the cycle time

![Elements and composition of the cycle time](image)

Figure 19-1  Elements and composition of the cycle time
19.2 Calculating the cycle time

Extending the cycle time

The cycle time of a user program is extended by the factors outlined below:

- Time-based interrupt processing
- Hardware interrupt processing (see also section "Interrupt response time" (Page 358))
- Diagnostics and error processing (see also section "Example of calculation of the interrupt response time" (Page 360))
- Communication via MPI or the integrated PROFINET interface and CPs connected by means of the communication bus (e.g.: Ethernet, Profibus, DP) as a factor in communication load
- Special functions such as operator control and monitoring of tags or the block status
- Transfer and deletion of blocks, compressing of the user program memory
- Runtime of signals using the synchronization cable

Influencing factors

The table below shows the factors influencing the cycle time.

Table 19-2 Factors influencing cycle time

<table>
<thead>
<tr>
<th>Factors</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer time for the process output image (POI) and process input image (PII)</td>
<td>See tables from 19-3 onwards</td>
</tr>
<tr>
<td>User program execution time</td>
<td>This value is calculated based on the execution times of the various statements (see the S7-400 statement list).</td>
</tr>
<tr>
<td>Operating system execution time at the cycle control point</td>
<td>See Table 19-7</td>
</tr>
<tr>
<td>Extension of cycle time due to communication load</td>
<td>You configure the maximum permitted communication load on the cycle as a percentage in STEP 7 (Programming with STEP 7 manual). See section Communication load (Page 345).</td>
</tr>
<tr>
<td>Load on cycle times due to interrupts</td>
<td>Interrupt requests can always stop user program execution. See Table 19-8</td>
</tr>
</tbody>
</table>

Process image update

The table below shows the time a CPU requires to update the process image (process image transfer time). The specified times only represent "ideal values", and may be extended accordingly by any interrupts or communication of the CPU.

Calculation of the transfer time for process image update:

K+ portion in the central controller (from row A in the following table) + portion in the expansion device with local connection (from row B)
+ portion in the expansion device with remote connection (from row C)
+ portion via integrated DP interface (from row D1)
+ portion via external DP interface (from row D2)
portion of consistent data via integrated DP interface (from row E1)
+ portion of consistent data via external DP interface (from row E2)
+ portion in PN/IO area for the integrated PROFINET interface (from row F)
+ portion for each submodule with 32 byte of consistent data for the integrated PROFINET interface (from row G)

= **Transfer time for process image update**

The tables below show the various portions of the transfer time for a process image update (process image transfer time). The specified times only represent "ideal values", and may be extended accordingly by any interrupts or communication of the CPU.

### Table 19-3 Portion of the process image transfer time, CPU 412-5H

<table>
<thead>
<tr>
<th>Portion</th>
<th>CPU 412-5H stand-alone mode</th>
<th>CPU 412-5H redundant</th>
</tr>
</thead>
<tbody>
<tr>
<td>K</td>
<td>Base load</td>
<td>10 µs</td>
</tr>
<tr>
<td>A *)</td>
<td>In the central controller</td>
<td>9.5 µs</td>
</tr>
<tr>
<td></td>
<td>Read/write byte/word/double word</td>
<td></td>
</tr>
<tr>
<td>B *)</td>
<td>In the expansion unit with local link</td>
<td>24 µs</td>
</tr>
<tr>
<td></td>
<td>Read/write byte/word/double word</td>
<td></td>
</tr>
<tr>
<td>C ***)</td>
<td>In the expansion unit with remote link</td>
<td>48 µs</td>
</tr>
<tr>
<td></td>
<td>Read/write byte/word/double word</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>In the DP area for the integrated DP interface</td>
<td>0.75 µs</td>
</tr>
<tr>
<td></td>
<td>Read byte/word/double word</td>
<td>35 µs</td>
</tr>
<tr>
<td>D2 ***)</td>
<td>In the DP area for the external DP interfaces</td>
<td>6.0 µs</td>
</tr>
<tr>
<td></td>
<td>Read/write byte/word/double word</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>Consistent data in the process image for the integrated DP interface</td>
<td>28 µs</td>
</tr>
<tr>
<td></td>
<td>Read/write data</td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>Consistent data in the process image for the external DP interface (CP 443–5 extended)</td>
<td>250 µs</td>
</tr>
<tr>
<td></td>
<td>Read write</td>
<td>70 µs</td>
</tr>
<tr>
<td>F</td>
<td>In the PN/IO area for the integrated PROFINET interface</td>
<td>4 µs</td>
</tr>
<tr>
<td></td>
<td>Read/write for each byte/word/double word</td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>Per submodule with 32 bytes of consistent data for the integrated PROFINET interface</td>
<td>28 µs</td>
</tr>
</tbody>
</table>

*) In the case of I/O inserted into the central controller or expansion device, the specified value contains the execution time of the I/O module.
The module data is updated with the minimum number of accesses.
(example: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)

**) Measured with IM460-3 and IM461-3 at a link length of 100 m

***) Measured with modules with 1 byte of user data, e.g. DI 16.
### 19.2 Calculating the cycle time

#### Table 19-4 Portion of the process image transfer time, CPU 414-5H

<table>
<thead>
<tr>
<th>Portion</th>
<th>CPU 414-5H</th>
<th>CPU 414-5H</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>stand-alone mode</td>
<td>redundant</td>
</tr>
<tr>
<td>K Base load</td>
<td>8 µs</td>
<td>9 µs</td>
</tr>
<tr>
<td>A *) In the central controller</td>
<td>8.5 µs</td>
<td>25 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B *) In the expansion unit with local link</td>
<td>23 µs</td>
<td>40 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C **) In the expansion unit with remote link</td>
<td>47 µs</td>
<td>64 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1 In the DP area for the integrated DP interface</td>
<td>0.5 µs</td>
<td>21.5 µs</td>
</tr>
<tr>
<td>Read byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2 *** In the DP area for the external DP interfaces</td>
<td>5.2 µs</td>
<td>24.6 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1 Consistent data in the process image for the integrated DP interface</td>
<td>15 µs</td>
<td>45 µs</td>
</tr>
<tr>
<td>Read/write data</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2 Consistent data in the process image for the external DP interface (CP 443–5 extended)</td>
<td>130 µs</td>
<td>170 µs</td>
</tr>
<tr>
<td>Read/Write</td>
<td>65 µs</td>
<td>100 µs</td>
</tr>
<tr>
<td>F In the PNIO area for the integrated PROFINET interface</td>
<td>3 µs</td>
<td>25 µs</td>
</tr>
<tr>
<td>Read/write for each byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G Per submodule with 32 bytes of consistent data for the integrated PROFINET interface</td>
<td>15 µs</td>
<td>45 µs</td>
</tr>
</tbody>
</table>

*) In the case of I/O inserted into the central controller or expansion device, the specified value contains the execution time of the I/O module. The module data is updated with the minimum number of accesses. (example: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)

**) Measured with IM460-3 and IM461-3 at a link length of 100 m

***) Measured with modules with 1 byte of user data, e.g. DI 16.

#### Table 19-5 Portion of the process image transfer time, CPU 416-5H

<table>
<thead>
<tr>
<th>Portion</th>
<th>CPU 416-5H</th>
<th>CPU 416-5H</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>stand-alone mode</td>
<td>redundant</td>
</tr>
<tr>
<td>K Base load</td>
<td>5 µs</td>
<td>6 µs</td>
</tr>
<tr>
<td>A *) In the central controller</td>
<td>8 µs</td>
<td>20 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B *) In the expansion unit with local link</td>
<td>22 µs</td>
<td>35 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C **) In the expansion unit with remote link</td>
<td>46 µs</td>
<td>57 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1 In the DP area for the integrated DP interface</td>
<td>0.45 µs</td>
<td>15 µs</td>
</tr>
<tr>
<td>Read byte/word/double word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2 *** In the DP area for the external DP interfaces</td>
<td>5.1 µs</td>
<td>20 µs</td>
</tr>
<tr>
<td>Read/write byte/word/double word</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## 19.2 Calculating the cycle time

### Calculating the cycle time

<table>
<thead>
<tr>
<th>Portion</th>
<th><strong>CPU 416–5H</strong></th>
<th><strong>CPU 416–5H</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>stand-alone mode</strong></td>
<td><strong>redundant</strong></td>
</tr>
</tbody>
</table>

| E1       | Consistent data in the process image for the integrated DP interface  
          | Read/write data          | 12 µs          | 35 µs          |
| E2       | Consistent data in the process image for the external DP interface (CP 443–5 extended)  
          | Read/write               | 127 µs         | 141 µs         |
|          |                      | 60 µs          | 80 µs          |
| F        | In the PNIO area for the integrated PROFINET interface  
          | Read/write for each byte/word/double word       | 2.5 µs         | 20 µs          |
| G        | Per submodule with 32 bytes of consistent data for the integrated PROFINET interface  
          |                          | 12 µs          | 35 µs          |

*) In the case of I/O inserted into the central controller or expansion device, the specified value contains the execution time of the I/O module. The module data is updated with the minimum number of accesses. (example: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)

**) Measured with IM460-3 and IM461-3 at a link length of 100 m

***) Measured with modules with 1 byte of user data, e.g. DI 16.

### Table 19-6 Portion of the process image transfer time, CPU 417-5H

<table>
<thead>
<tr>
<th>Portion</th>
<th><strong>CPU 417–5H</strong></th>
<th><strong>CPU 417–5H</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>stand-alone mode</strong></td>
<td><strong>redundant</strong></td>
</tr>
</tbody>
</table>

| K | Base load | 3 µs | 4 µs |
| A | In the central controller  
    | Read/write byte/word/double word       | 7.3 µs         | 15 µs          |
| B | In the expansion unit with local link  
    | Read/write byte/word/double word       | 20 µs          | 26 µs          |
| C | In the expansion unit with remote link  
    | Read/write byte/word/double word       | 45 µs          | 50 µs          |
| D1 | In the DP area for the integrated DP interface  
    | Read byte/word/double word             | 0.4 µs         | 10 µs          |
| D2 | In the DP area for the external DP interfaces  
    | Read/write byte/word/double word       | 5 µs           | 15 µs          |
| E1 | Consistent data in the process image for the integrated DP interface  
    | Read/write data                        | 8 µs           | 30 µs          |
| E2 | Consistent data in the process image for the external DP interface (CP 443–5 extended)  
    | Read/write                              | 80 µs          | 100 µs         |
|   |                      | 60 µs          | 70 µs          |
| F | In the PNIO area for the integrated PROFINET interface  
    | Read/write for each byte/word/double word | 2 µs           | 15 µs          |
| G | Per submodule with 32 bytes of consistent data for the integrated PROFINET interface  
    |                          | 8 µs           | 30 µs          |
19.2 Calculating the cycle time

Portion

CPU 417–5H
stand-alone mode
CPU 417–5H
redundant

*) In the case of I/O inserted into the central controller or expansion device, the specified value contains the execution time of the I/O module. The module data is updated with the minimum number of accesses. (example: 8 bytes result in 2 double word accesses; 16 bytes in 4 double word accesses.)

**) Measured with IM460-3 and IM461-3 at a link length of 100 m

***) Measured with modules with 1 byte of user data, e.g. DI 16.

Extending the cycle time

The calculated cycle time of a S7-400H CPU must be multiplied by a CPU-specific factor. The table below lists these factors:

Table 19- 7 Extending the cycle time

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Factor</td>
<td>1.05</td>
<td>1.2</td>
<td>1.05</td>
<td>1.2</td>
<td>1.05</td>
<td>1.2</td>
<td>1.05</td>
<td>1.2</td>
</tr>
</tbody>
</table>

Long synchronization cables may increase cycle times. This extension can have the factor 2 - 5 with a cable length of 10 km.

Operating system execution time at the cycle control point

The table below shows the operating system execution time at the cycle checkpoint of the CPUs.

Table 19- 8 Operating system execution time at the cycle control point

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle control at the SCCP</td>
<td>120-700 μs</td>
<td>405-2080 μs</td>
<td>70-450 μs</td>
<td>260-1350 μs</td>
<td>50-400 μs</td>
<td>180-970 μs</td>
<td>30 - 330 μs</td>
<td>115 - 650 μs</td>
</tr>
<tr>
<td>⊗ 130 μs</td>
<td>⊗ 505 μs</td>
<td>⊗ 80 μs</td>
<td>⊗ 310 μs</td>
<td>⊗ 55</td>
<td>⊗ 215</td>
<td>⊗ 35 μs</td>
<td>⊗ 130 μs</td>
<td></td>
</tr>
</tbody>
</table>
## Extended cycle time due to nested interrupts

The program runtime at interrupt level must be added to this time extension.

The corresponding times are added together if the program contains nested interrupts.

### Table 19- 9 Extended cycle time due to nested interrupts

<table>
<thead>
<tr>
<th>CPU</th>
<th>Hardware interrupt</th>
<th>Diagnostic interrupt</th>
<th>Time-of-day interrupt</th>
<th>Delay interrupt</th>
<th>Cyclic interrupt</th>
<th>Programming error</th>
<th>I/O access error</th>
<th>Asynchronous error</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU 412–5H stand-alone mode</td>
<td>240 µs</td>
<td>240 µs</td>
<td>230 µs</td>
<td>150 µs</td>
<td>150 µs</td>
<td>80 µs</td>
<td>80 µs</td>
<td>180 µs</td>
</tr>
<tr>
<td>CPU 412–5H redundant</td>
<td>680 µs</td>
<td>550 µs</td>
<td>700 µs</td>
<td>580 µs</td>
<td>450 µs</td>
<td>350 µs</td>
<td>179 µs</td>
<td>550 µs</td>
</tr>
<tr>
<td>CPU 414–5H stand-alone mode</td>
<td>160 µs</td>
<td>120 µs</td>
<td>150 µs</td>
<td>100 µs</td>
<td>100 µs</td>
<td>60 µs</td>
<td>60 µs</td>
<td>120 µs</td>
</tr>
<tr>
<td>CPU 414–5H redundant</td>
<td>420 µs</td>
<td>400 µs</td>
<td>490 µs</td>
<td>360 µs</td>
<td>280 µs</td>
<td>220 µs</td>
<td>120 µs</td>
<td>306 µs</td>
</tr>
<tr>
<td>CPU 416–5H stand-alone mode</td>
<td>120 µs</td>
<td>110 µs</td>
<td>100 µs</td>
<td>80 µs</td>
<td>60 µs</td>
<td>40 µs</td>
<td>40 µs</td>
<td>80 µs</td>
</tr>
<tr>
<td>CPU 416–5H redundant</td>
<td>300 µs</td>
<td>250 µs</td>
<td>370 µs</td>
<td>220 µs</td>
<td>200 µs</td>
<td>150 µs</td>
<td>90 µs</td>
<td>230 µs</td>
</tr>
<tr>
<td>CPU 417–5H stand-alone mode</td>
<td>90 µs</td>
<td>70 µs</td>
<td>70 µs</td>
<td>50 µs</td>
<td>50 µs</td>
<td>30 µs</td>
<td>30 µs</td>
<td>70 µs</td>
</tr>
<tr>
<td>CPU 417–5H redundant</td>
<td>200 µs</td>
<td>170 µs</td>
<td>230 µs</td>
<td>150 µs</td>
<td>150 µs</td>
<td>100 µs</td>
<td>45 µs</td>
<td>133 µs</td>
</tr>
</tbody>
</table>
19.3 Different cycle times

The cycle time \((T_{\text{cyc}})\) length is not the same in every cycle. The figure below shows different cycle times \(T_{\text{cyc1}}\) and \(T_{\text{cyc2}}\). \(T_{\text{cyc2}}\) is longer than \(T_{\text{cyc1}}\) because the cyclically executed OB 1 is interrupted by a TOD interrupt OB (here: OB 10).

![Figure 19-2 Different cycle times](image)

Fluctuation of the block processing time (e.g. OB 1) may also be a factor causing cycle time fluctuation, due to:

- conditional instructions
- conditional block calls
- different program paths
- loops, etc.

Maximum cycle time

In STEP 7 you can modify the default maximum cycle time (scan cycle monitoring time). OB 80 is called when this time expires. In this block you can specify the CPUs response to this time error. If you do not retrigger the cycle time with SFC 43, OB 80 doubles the cycle time at the first call. In this case the CPU switches to STOP mode when OB 80 is called a second time.

The CPU switches to STOP mode if OB 80 does not exist in its memory.
Minimum cycle time

In STEP 7 you can set a minimum cycle time for a CPU. This is practical if

- the intervals between starting program execution of OB 1 (free cycle) are to be more or less of the same length, or
- the cycle time were too short, the process images would be updated more often than necessary

The actual cycle time is the sum of $T_{cyc}$ and $T_{wait}$. It is thus always longer or equal to $T_{min}$. 
19.4 Communication load

The operating system provides the CPU continuously with the configured time slices as a percentage of the overall CPU processing resources (time slice technique). Processing performance not required for communication is made available to other processes.

In the hardware configuration you can specify a communication load value between 5% and 50%. The default value is 20%.

This percentage is to be interpreted as mean value, i.e. communication resources may take significantly more than 20% of a time slice. The communication portion is then only a few % or 0% in the next time slice.

The formula below describes the influence of communication load on the cycle time:

\[
\text{Actual cycle time} = \frac{\text{Cycle time} \times 100}{100 - \text{"Configured communication load in %"}}
\]

Round the result up to the next highest integer!

Figure 19-4 Formula: Influence of communication load

Data consistency

The user program is interrupted to process communications. This interruption can be triggered after any statement. These communication jobs may lead to a change in user data. As a result, data consistency cannot be ensured over several accesses. How to ensure data consistency in operations comprising more than one command is described in the "Consistent data" section.

Figure 19-5 Distribution of a time slice

The operating system takes a certain portion of the remaining time slice for internal tasks. This portion is included in the factor defined in the tables starting at 16-3.

Example: 20% communication load

In the hardware configuration you have set a communication load of 20%.

The calculated cycle time is 10 ms.

This means that a setting of 20% communication load allocates an average of 200 μs to communication and 800 μs to the user program in each time slice. So the CPU requires 10 ms / 800 μs = 13 time slices to execute one cycle. This means the physical cycle time is
equivalent to 13 times 1-ms time slice = 13 ms, if the CPU fully utilizes the configured communication load.

That is to say, 20% communication does not extend the cycle by a linear amount of 2 ms, but by 3 ms.

**Example: 50% communication load**

In the hardware configuration you have set a communication load of 50%.

The calculated cycle time is 10 ms.

This means that 500 µs remain in each time slice for the cycle. So the CPU requires 10 ms / 500 µs = 20 time slices to execute one cycle. This means the physical cycle time is 20 ms if the CPU fully utilizes the configured communication load.

So a setting of 50% communication load allocates 500 µs to communication and 500 µs to the user program in each time slice. So the CPU requires 10 ms / 500 µs = 20 time slices to execute one cycle. This means the physical cycle time is equivalent to 20 times 1-ms time slice = 20 ms, if the CPU fully utilizes the configured communication load.

This means that 50% communication does not extend the cycle by a linear amount of 5 ms, but by 10 ms (= doubling the calculated cycle time).

**Dependency of the actual cycle time on communication load**

The figure below describes the non-linear dependency of the actual cycle time on communication load. In our example we have chosen a cycle time of 10 ms.

![Figure 19-6 Dependency of the cycle time on communication load](image-url)
**Further effects on the actual cycle time**

Seen statistically, the extension of cycle times due to communication load leads to more asynchronous events occurring within an OB 1 cycle, for example interrupts. This further extends the OB 1 cycle. How much it is extended depends on the number of events per OB 1 cycle and the time required for processing these events.

**Remarks**

- Change the value of the "communication load" parameter to check the effects on the cycle time during system runtime.
- Always take the communication load into account when you set the maximum cycle time, otherwise you risk timeouts.

**Recommendations**

- Use the default setting whenever possible.
- Increase this value only if the CPU is used primarily for communication, and if time is not a critical factor for the user program! In all other situations you should only reduce this value!

### 19.5 Response time

**Definition of response time**

The response time is the time from detecting an input signal to changing the output signal associated with it.

**Fluctuation range**

The actual response time lies between the shortest and the longest response time. You must always assume the longest response time when configuring your system.

The section below deals with the shortest and longest response times, in order to provide an overview of the fluctuation in the length of response times.

**Factors**

The response time depends on the cycle time and the following factors:

- Delay of the inputs and outputs
- Additional DP cycle times on the PROFIBUS DP network
- Execution in the user program
Delay of the I/Os

Make allowances for the following module-specific delay times:

- For digital inputs: the input delay time
- For digital inputs with interrupt function: the input delay time + internal preparation time
- For digital outputs: negligible delay times
- For relay outputs: typical delay times of 10 ms to 20 ms. The delay of relay outputs also depends on the temperature and voltage.
- For analog inputs: cycle time for analog input
- For analog outputs: response time at analog outputs

For information on delay times, refer to the technical specifications of the signal modules.

DP cycle times on the PROFIBUS DP network

If you configured your PROFIBUS DP network in STEP 7, STEP 7 calculates the typical DP cycle time to be expected. You can then view the DP cycle time of your configuration on the PG in the bus parameters section.

The figure below provides an overview of the DP cycle time. In this example, we assume an average value for each DP slave of 4 bytes of data.
If you are operating a PROFIBUS DP network with more than one master, you will need to take the DP cycle time into account for each master. In other words, perform a separate calculation for each master and add the results together.
**Shortest response time**

The figure below shows the conditions under which the shortest response time is achieved.

![Diagram showing the conditions for the shortest response time]

**Calculation**

The (shortest) response time is calculated as follows:

- 1 x process image transfer time of the inputs +
- 1 x process image transfer time of the outputs +
- 1 x program processing time +
- 1 x operating system processing time at the SCCP +
- Delay of the inputs and outputs

The result is equivalent to the sum of the cycle time plus the I/O delay times.

**Note**

If the CPU and signal module are not in the central unit, you will have to add twice the delay time of the DP slave frame (including processing in the DP master).
Longest response time

The figure below shows the conditions under which the longest response time is achieved.

![Diagram of the longest response time](image)

Figure 19-9 Longest response time

Calculation

The (longest) response time is calculated as follows:

- $2 \times$ process image transfer time of the inputs +
- $2 \times$ process image transfer time of the outputs +
- $2 \times$ operating system processing time +
- $2 \times$ program processing time +
- $2 \times$ delay of the DP slave frame (including processing in the DP master) +
- Delay of the inputs and outputs

This is equivalent to the sum of twice the cycle time and the delay in the inputs and outputs plus twice the DP cycle time.
Processing direct I/O access

You can achieve faster response times with direct access to the I/Os in your user program, e.g. with the following operations:

- L PEB
- T PQW

However, note that any I/O access requires a synchronization of the two units and thus extends the cycle time.

Reducing the response time

This reduces the maximum response time to

- Delay of the inputs and outputs
- User program execution time (can be interrupted by higher-priority interrupt handling)
- Runtime of direct access
- Twice the bus delay time of DP

The following table lists the execution times of direct access by the CPU to I/O modules. The specified times are pure CPU processing times and do not include the processing times of the signal modules.

Table 19-10 Direct access of the CPUs to I/O modules in the central rack

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Read byte</td>
<td>3.0 µs</td>
<td>33.9 µs</td>
<td>2.6 µs</td>
<td>21.0 µs</td>
<td>2.3 µs</td>
<td>15.9 µs</td>
<td>2.2 µs</td>
<td>11.2 µs</td>
</tr>
<tr>
<td>Read word</td>
<td>4.0 µs</td>
<td>33.9 µs</td>
<td>4.0 µs</td>
<td>24.5 µs</td>
<td>4.0 µs</td>
<td>16.2 µs</td>
<td>3.9 µs</td>
<td>11.7 µs</td>
</tr>
<tr>
<td>Read double word</td>
<td>7.0 µs</td>
<td>33.9 µs</td>
<td>7.0 µs</td>
<td>24.5 µs</td>
<td>7.0 µs</td>
<td>17.2 µs</td>
<td>7.0 µs</td>
<td>14.7 µs</td>
</tr>
<tr>
<td>Write byte</td>
<td>3.0 µs</td>
<td>33.9 µs</td>
<td>2.6 µs</td>
<td>21.5 µs</td>
<td>2.4 µs</td>
<td>16.0 µs</td>
<td>2.3 µs</td>
<td>11.3 µs</td>
</tr>
<tr>
<td>Write word</td>
<td>4.0 µs</td>
<td>33.9 µs</td>
<td>4.0 µs</td>
<td>24.5 µs</td>
<td>4.0 µs</td>
<td>16.2 µs</td>
<td>3.9 µs</td>
<td>11.8 µs</td>
</tr>
<tr>
<td>Write double word</td>
<td>7.5 µs</td>
<td>33.9 µs</td>
<td>7.4 µs</td>
<td>24.5 µs</td>
<td>7.3 µs</td>
<td>18.5 µs</td>
<td>7.1 µs</td>
<td>15.0 µs</td>
</tr>
</tbody>
</table>
### 19.5 Response time

#### Table 19-11 Direct access of the CPUs to I/O modules in the expansion unit with local link

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Read byte</td>
<td>6.0 µs</td>
<td>36.0 µs</td>
<td>5.6 µs</td>
<td>24.5 µs</td>
<td>5.6 µs</td>
<td>16.1 µs</td>
<td>5.6 µs</td>
<td>13.4 µs</td>
</tr>
<tr>
<td>Write byte</td>
<td>5.3 µs</td>
<td>35.3 µs</td>
<td>5.3 µs</td>
<td>24.5 µs</td>
<td>5.3 µs</td>
<td>16.1 µs</td>
<td>5.3 µs</td>
<td>13.4 µs</td>
</tr>
<tr>
<td>Read word</td>
<td>11.0 µs</td>
<td>41.3 µs</td>
<td>10.5 µs</td>
<td>32.1 µs</td>
<td>10.5 µs</td>
<td>23.8 µs</td>
<td>10.5 µs</td>
<td>18.6 µs</td>
</tr>
<tr>
<td>Write word</td>
<td>10.6 µs</td>
<td>41.3 µs</td>
<td>10.2 µs</td>
<td>28.6 µs</td>
<td>10.2 µs</td>
<td>21.5 µs</td>
<td>10.2 µs</td>
<td>18.3 µs</td>
</tr>
<tr>
<td>Read double word</td>
<td>20.0 µs</td>
<td>49.0 µs</td>
<td>19.9 µs</td>
<td>40.0 µs</td>
<td>19.9 µs</td>
<td>31.7 µs</td>
<td>19.9 µs</td>
<td>28.7 µs</td>
</tr>
<tr>
<td>Write double word</td>
<td>19.8 µs</td>
<td>49.0 µs</td>
<td>19.8 µs</td>
<td>39.8 µs</td>
<td>19.8 µs</td>
<td>31.5 µs</td>
<td>19.8 µs</td>
<td>28.0 µs</td>
</tr>
</tbody>
</table>

#### Table 19-12 Direct access of the CPUs to I/O modules in the expansion unit with remote link, setting 100 m

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Read byte</td>
<td>11.5 µs</td>
<td>41.3 µs</td>
<td>11.5 µs</td>
<td>27.5 µs</td>
<td>11.4 µs</td>
<td>20.3 µs</td>
<td>11.3 µs</td>
<td>17.0 µs</td>
</tr>
<tr>
<td>Write byte</td>
<td>11.0 µs</td>
<td>41.3 µs</td>
<td>11.0 µs</td>
<td>27.0 µs</td>
<td>10.8 µs</td>
<td>20.2 µs</td>
<td>10.8 µs</td>
<td>16.8 µs</td>
</tr>
<tr>
<td>Read word</td>
<td>23.0 µs</td>
<td>49.0 µs</td>
<td>23.0 µs</td>
<td>39.8 µs</td>
<td>22.8 µs</td>
<td>31.5 µs</td>
<td>21.9 µs</td>
<td>27.8 µs</td>
</tr>
<tr>
<td>Write word</td>
<td>22.0 µs</td>
<td>49.0 µs</td>
<td>22.0 µs</td>
<td>39.8 µs</td>
<td>21.9 µs</td>
<td>31.5 µs</td>
<td>21.9 µs</td>
<td>27.8 µs</td>
</tr>
<tr>
<td>Read double word</td>
<td>46.0 µs</td>
<td>72.1 µs</td>
<td>46.0 µs</td>
<td>62.9 µs</td>
<td>45.9 µs</td>
<td>54.5 µs</td>
<td>54.5 µs</td>
<td>50.0 ms</td>
</tr>
<tr>
<td>Write double word</td>
<td>44.5 µs</td>
<td>72.1 µs</td>
<td>44.5 µs</td>
<td>62.9 µs</td>
<td>44.0 µs</td>
<td>44.0 µs</td>
<td>44.0 µs</td>
<td>50.0 ms</td>
</tr>
</tbody>
</table>

**Note**

You can also achieve fast response times by using hardware interrupts; see section **Interrupt response time** (Page 358).
### 19.6 Calculating cycle and response times

#### Cycle time

1. Using the Instruction List, determine the runtime of the user program.
2. Calculate and add the process image transfer time. You will find guide values for this in the tables starting at 16-3.
3. Add the processing time at the scan cycle checkpoint. You will find guide values for this in Table 16–8.
4. Multiply the calculated value by the factor in Table 16–7.

The final result is the **cycle time**.

#### Extension of the cycle time due to communication and interrupts

1. Multiply the result by the following factor:
   \[
   \frac{100}{100 - \text{"configured communication load in %"}}
   \]
2. Using the instruction list, calculate the runtime of the program elements processing the interrupts. To do so, add the relevant value from Table 16-9. Multiply this value by the factor from step 4. Add this value to the theoretical cycle time as often as the interrupt is triggered or is expected to be triggered during the cycle time.

The result is an approximated **actual cycle time**. Note down the result.

#### Table 19-13 Example of calculating the response time

<table>
<thead>
<tr>
<th>Shortest response time</th>
<th>Longest response time</th>
</tr>
</thead>
<tbody>
<tr>
<td>3. Next, calculate the delays in the inputs and outputs and, if applicable, the cycle times on the PROFIBUS DP network.</td>
<td>3. Multiply the actual cycle time by factor 2.</td>
</tr>
<tr>
<td>4. The result you obtain is the <strong>shortest response time</strong>.</td>
<td>4. Next, calculate the delays in the inputs and outputs and the DP cycle times on the PROFIBUS DP network.</td>
</tr>
<tr>
<td>5. The result you obtain is the <strong>longest response time</strong>.</td>
<td></td>
</tr>
</tbody>
</table>

---

*System Manual, 07/2014, A5E00267695-13*
19.7 Examples of calculating the cycle and response times

Example I
You have installed an S7-400 with the following modules in the central unit:
- a CPU 414–5H in redundant mode
- 2 digital input modules SM 421; DI 32xDC 24 V (each with 4 bytes in the PI)
- 2 digital output modules SM 422; DO 32xDC 24 V/0.5 (each with 4 bytes in the PI)

User program
According to the instruction list, the user program runtime is 15 ms.

Calculating the cycle time
The cycle time for the example results from the following times:
- As the CPU-specific factor is 1.2, the user program execution time is:
  approx. 18.0 ms
- Process image transfer time (4 double-word accesses)
  Process image: 9 µs + 4 x 25 µs = approx. 0.109 ms
- OS execution time at the scan cycle checkpoint:
  approx. 0.31 ms
The total of the listed times is equivalent to the cycle time:
\[
\text{Cycle time} = 18.0 \text{ ms} + 0.109 \text{ ms} + 0.31 \text{ ms} = 18.419 \text{ ms}.
\]

Calculation of the actual cycle time
- Allowance for communication load (default value: 20%):
  \[18.419 \text{ ms} \times 100 / (100–20) = 23.024 \text{ ms}.
\]
- There is no interrupt processing.
So the actual, cycle time is approx. 23 ms.

Calculating the longest response time
- Longest response time
  \[23.024 \text{ ms} \times 2 = 46.048 \text{ ms}.
\]
- The delay of the inputs and outputs is negligible.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- There is no interrupt processing.
So the longest, rounded up response time is = 46.1 ms.
Example II
You have installed an S7-400 with the following modules:

- a CPU 414–5H in redundant mode
- 4 digital input modules SM 421; DI 32×DC 24 V (each with 4 bytes in the PI)
- 3 digital output modules SM 422; DO 16xDC 24 V /2 (each with 2 bytes in the PI)
- 2 analog input modules SM 431; AI 8x13 bit (not in the PI)
- 2 analog output modules SM 432; AO 8x13 bit (not in the PI)

CPU parameters
The CPU was parameterized as follows:
- Cycle load due to communication: 40 %

User program
According to the instruction list, the user program runtime is 10.0 ms.

Calculating the cycle time
The theoretical cycle time for the example is derived from the following times:

- As the CPU-specific factor is 1.2, the user program execution time is:
  approx. 12.0 ms
- Process image transfer time (4 x double-word access and 3 x word access)
  Process image: 9 µs + 7 ×25 µs = approx. 0.184 ms
- Operating system runtime at scan cycle checkpoint:
  approx. 0.31 ms

The total of the listed times is equivalent to the cycle time:

\[
\text{Cycle time} = 12.0 \text{ ms} + 0.184 \text{ ms} + 0.31 \text{ ms} = 12.494 \text{ ms}
\]

Calculation of the actual cycle time

- Allowance for communication load:
  \[12.494 \text{ ms} \times 100 / (100–40) = 20.823 \text{ ms}\.
- A time-of-day interrupt with a runtime of 0.5 ms is triggered every 100 ms.
  The interrupt can be triggered a maximum of one time during a cycle:
  \[0.5 \text{ ms} + 0.490 \text{ ms (from table 16-9)} = 0.99 \text{ ms}\.
  Allowing for communication load:
  \[0.99 \text{ ms} \times 100 / (100–40) = 1.65 \text{ ms}\.
- \[20.823 \text{ ms} + 1.65 \text{ ms} = 22.473 \text{ ms}\.

Taking into account the time slices, the actual rounded up cycle time is **22.5 ms**.
Calculating the longest response time

- Longest response time
  
  \[ 22.5 \text{ ms} \times 2 = 45 \text{ ms}. \]

- Delay of inputs and outputs
  
  - The maximum input delay of the digital input module SM 421; DI 32\times DC 24 V is 4.8 ms per channel
  
  - The output delay of the digital output module SM 422; DO 16\times DC 24 V/2A is negligible.
  
  - Analog input module SM 431; AI 8\times 13Bit was parameterized for 50 Hz interference frequency suppression. The result is a conversion time of 25 ms per channel. As 8 channels are active, a cycle time of the analog input module of 200 ms results.
  
  - Analog output module SM 432; AO 8\times 13Bit was parameterized for operation in the measuring range 0 ... 10 V. This results in a conversion time of 0.3 ms per channel. Since 8 channels are active, the result is a cycle time of 2.4 ms. The transient time of a resistive load of 0.1 ms must be added to this. The result is an analog output response time of 2.5 ms.

- All components are installed in the central unit, so DP cycle times can be ignored.

- Case 1: The system sets an output channel of the digital output module after a digital input signal is read in. The result is as follows:

  Response time = 45 ms + 4.8 ms = 49.8 ms.

- Case 2: The system reads in and outputs an analog value. The result is as follows:

  Response time = 45 ms + 200 ms + 2.5 ms = 247.5 ms.
19.8 Interrupt response time

Definition of interrupt response time

The interrupt response time is the time from the first occurrence of an interrupt signal to the call of the first instruction in the interrupt OB.

General rule: Higher priority interrupts are handled first. This means the interrupt response time is increased by the program execution time of the higher-priority interrupt OBs, and by previous interrupt OBs of the same priority which have not yet been processed (queue).

Note that any update of the standby CPU extends the interrupt response time.

Calculating the interrupt response time

Minimum interrupt response time of the CPU
+ minimum interrupt response time of the signal modules
+ PROFIBUS DP cycle time on PROFINET
= Shortest interrupt response time

Minimum interrupt response time of the CPU
+ maximum interrupt response time of the signal modules
+ 2 * cycle time on PROFIBUS DP or PROFINET
= Longest interrupt response time

Process and diagnostic interrupt response times of the CPUs

Table 19-14 Process and interrupt response times; maximum interrupt response time without communication

<table>
<thead>
<tr>
<th>CPU</th>
<th>Hardware interrupt response times</th>
<th>Diagnostic interrupt response times</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>min.</td>
<td>max.</td>
</tr>
<tr>
<td>412-5H stand-alone mode</td>
<td>190 µs</td>
<td>370 µs</td>
</tr>
<tr>
<td>412-5H redundant</td>
<td>370 µs</td>
<td>850 µs</td>
</tr>
<tr>
<td>414-5H stand-alone mode</td>
<td>140 µs</td>
<td>200 µs</td>
</tr>
<tr>
<td>414-5H redundant</td>
<td>330 µs</td>
<td>620 µs</td>
</tr>
<tr>
<td>416-5H stand-alone mode</td>
<td>90 µs</td>
<td>140 µs</td>
</tr>
<tr>
<td>416-5H redundant</td>
<td>240 µs</td>
<td>500 µs</td>
</tr>
<tr>
<td>417-5H stand-alone mode</td>
<td>80 µs</td>
<td>90 µs</td>
</tr>
<tr>
<td>417-5H redundant</td>
<td>160 µs</td>
<td>310 µs</td>
</tr>
</tbody>
</table>
Increasing the maximum interrupt response time with communication

The maximum interrupt response time is extended when the communication functions are active. The additional time is calculated using the following formula:

\[ \text{CPU 41x-5H } t_v = 100 \mu s + 1000 \mu s \times n\% \text{, significant extension possible} \]

where \( n = \) cycle load due to communication

Signal modules

The process interrupt response time of signal modules is made up as follows:

- **Digital input modules**

  Process interrupt response time = internal interrupt processing time + input delay

  You will find these times in the data sheet for the respective digital input module.

- **Analog input modules**

  Process interrupt response time = internal interrupt processing time + conversion time

  The internal interrupt processing time for analog input modules can be neglected. The conversion times can be found in the data sheet for the individual analog input modules.

The diagnostic interrupt response time of the signal modules is the time from detection of a diagnostic event by the signal module to the triggering of the diagnostic interrupt by the signal module. This short time can be neglected.

Hardware interrupt processing

Hardware interrupt processing begins when the process interrupt OB4x is called. Higher-priority interrupts stop process interrupt processing. Direct access to I/O modules is executed during the execution time of the operation. After the process interrupt has been processed, the system either resumes cyclic program processing, or calls and processes interrupt OBs of the same or lower priority.
19.9 Example of calculation of the interrupt response time

Elements of the interrupt response time

As a reminder: The process interrupt response time is made up of:

- The process interrupt response time of the CPU
- The process interrupt response time of the signal module
- Twice the DP cycle time on PROFIBUS DP

Example: You have installed a 417-5H CPU and four digital modules in the central controller. One digital input module is the SM 421; DI 16×UC 24/60 V; with process and diagnostic interrupts. You have enabled only the process interrupt in your CPU and SM parameterization. You decided not to use time-driven processing, diagnostics or error handling. You have parameterized an input delay of 0.5 ms for the digital input modules. No activities are required at the scan cycle checkpoint. You have set a cycle load of 20% due to communication.

Calculation

In this example, the process interrupt response time is based on following time factors:

- Process interrupt response time of CPU 417-5H: Approx. 0.3 ms (mean value in redundant system mode)
- Extension due to communication according to the description in section Interrupt response time (Page 358):
  \[100 \mu s + 1000 \mu s \times 20\% = 300 \mu s = 0.3 \text{ ms}\]

- Process interrupt response time of SM 421; DI 16×UC 24/60 V:
  - Internal interrupt processing time: 0.5 ms
  - Input delay: 0.5 ms

- The DP cycle time on the PROFIBUS DP is irrelevant, because the signal modules are installed in the central unit.

The process interrupt response time is equivalent to the sum of the listed time factors:

Process interrupt response time = 0.3 ms + 0.3 ms + 0.5 ms + 0.5 ms = approx. 1.6 ms.

This calculated process interrupt response time is the time between detection of a signal at the digital input and the call of the first instruction in OB 4x.
19.10 Reproducibility of delay and watchdog interrupts

Definition of "reproducibility"

Time-delay interrupt:
The period that expires between the call of the first operation in the interrupt OB and the programmed time of interrupt.

Cyclic interrupt:
The fluctuation range of the interval between two successive calls, measured between the respective initial operations of the interrupt OB.

Reproducibility

The following table contains the reproducibility of time-delay and cyclic interrupts of the CPUs.

Table 19-15 Reproducibility of time-delay and cyclic interrupts of the CPUs

<table>
<thead>
<tr>
<th>Module</th>
<th>Reproducibility</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Time-delay interrupt</td>
</tr>
<tr>
<td>CPU 412-5H stand-alone mode</td>
<td>± 230 µs</td>
</tr>
<tr>
<td>CPU 412-5H redundant</td>
<td>± 430 µs</td>
</tr>
<tr>
<td>CPU 414-5H stand-alone mode</td>
<td>± 160 µs</td>
</tr>
<tr>
<td>CPU 414-5H redundant</td>
<td>± 280 µs</td>
</tr>
<tr>
<td>CPU 416-5H stand-alone mode</td>
<td>± 130 µs</td>
</tr>
<tr>
<td>CPU 416-5H redundant</td>
<td>± 230 µs</td>
</tr>
<tr>
<td>CPU 417-5H stand-alone mode</td>
<td>± 120 µs</td>
</tr>
<tr>
<td>CPU 417-5H redundant</td>
<td>± 200 µs</td>
</tr>
</tbody>
</table>

These times only apply if the interrupt can actually be executed at this time and if it is not delayed, for example, by higher-priority interrupts or queued interrupts of equal priority.
19.10 Reproducibility of delay and watchdog interrupts
## Technical data

### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

<table>
<thead>
<tr>
<th>CPU and firmware version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order number</td>
</tr>
<tr>
<td>Firmware version</td>
</tr>
<tr>
<td>Corresponding programming package</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Work memory</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>Load memory</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>• Expandable FEPROM</td>
</tr>
<tr>
<td>• Expandable RAM</td>
</tr>
<tr>
<td>Battery backup</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Typical execution times</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execution times of</td>
</tr>
<tr>
<td>• Bit instructions</td>
</tr>
<tr>
<td>• Word instructions</td>
</tr>
<tr>
<td>• Fixed-point arithmetic</td>
</tr>
<tr>
<td>• Floating-point arithmetic</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timers/counters and their retentivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>S7 counters</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
</tr>
<tr>
<td>• Default</td>
</tr>
<tr>
<td>• Counting range</td>
</tr>
<tr>
<td>IEC counters</td>
</tr>
<tr>
<td>• Type</td>
</tr>
<tr>
<td>S7 timers</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
</tr>
<tr>
<td>• Default</td>
</tr>
<tr>
<td>• Time range</td>
</tr>
</tbody>
</table>
### Technical data

**20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)**

<table>
<thead>
<tr>
<th>IEC timers</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Type</td>
<td>SFB</td>
</tr>
</tbody>
</table>

#### Data areas and their retentivity

<table>
<thead>
<tr>
<th>Total retentive data area (incl. bit memories, timers, counters)</th>
<th>Total work and load memory (with backup battery)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit memory</td>
<td>8 KB</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
<td>From MB 0 to MB 8191</td>
</tr>
<tr>
<td>• Preset retentivity</td>
<td>From MB 0 to MB 15</td>
</tr>
</tbody>
</table>

#### Clock memories

<table>
<thead>
<tr>
<th>Data blocks</th>
<th>Maximum 6000 (DB 0 reserved) Number range 1 - 16000</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
</tbody>
</table>

#### Local data (configurable)

<table>
<thead>
<tr>
<th>Data blocks</th>
<th>Maximum 16 KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Default</td>
<td>8 KB</td>
</tr>
</tbody>
</table>

#### Blocks

<table>
<thead>
<tr>
<th>OBs</th>
<th>See <em>instruction list</em></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
</tbody>
</table>

- Number of free-cycle OBs: OB 1
- Number of time-of-day interrupt OBs: OB 10, 11, 12, 13
- Number of time-delay interrupt OBs: OB 20, 21, 22, 23
- Number of cyclic interrupts: OB 32, 33, 34, 35
- Number of process interrupt OBs: OB 40, 41, 42, 43
- Number of DPV1 interrupt OBs: OB 55, 56, 57
- Number of redundancy error OBs: OB 70, 72
- Number of asynchronous error OBs: OB 80, 81, 82, 83, 84, 85, 86, 87, 88
- Number of restart OBs: OB 100, 102
- Number of synchronous error OBs: OB 121, 122

#### Nesting depth

- Per priority class: 24
- Additional ones in an error OB: 1

<table>
<thead>
<tr>
<th>FBs</th>
<th>Maximum 3000 Number range 0 - 7999</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FCs</th>
<th>Maximum 3000 Number range 0 - 7999</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
</tbody>
</table>

| SDBs | Maximum 2048 |

#### Address ranges (I/O)

<table>
<thead>
<tr>
<th>Total I/O address range</th>
<th>8 KB/8 KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>• of those distributed</td>
<td>Including diagnostics addresses, addresses for I/O interfaces, etc.</td>
</tr>
</tbody>
</table>

| MPI/DP interface | 2 KB/2 KB |
## Technical data

### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

| DP interface | 4 KB/4 KB |
| PN interface | 8 KB/8 KB |
| Process image | 8 KB / 8 KB (configurable) |
| • Default | 256 bytes/256 bytes |
| • Number of process image partitions | Maximum 15 |
| • Consistent data | Max. 244 bytes |

Access to consistent data in the process image: Yes

Consistent data via PROFIBUS:
- Via integrated PROFINET interface: Max. 244 bytes
- Max. 1024 bytes

Digital channels:
- Maximum 65536/Maximum 65536
  - of those central: Maximum 65536/Maximum 65536

Analog channels:
- Maximum 4096/Maximum 4096
  - of those central: Maximum 4096/Maximum 4096

### Configuration

**Central controllers/expansion units**
- Maximum 2/20

**Multicomputing**
- No

**Number of plug-in IMs (total)**
- Maximum 6
  - IM 460: Maximum 6
  - IM 463–2: Maximum 4, in stand-alone mode only

**Number of DP masters**
- Maximum 4, in stand-alone mode only
  - integrated: 2
  - Via CP 443–5 Ext.: Maximum 10

**Number of plug-in S5 modules via adapter casing (in the central controller)**
- None

**Operable function modules and communication processors**
- Limited by the number of slots and connections
  - FM, CP (point-to-point): Limited by the number of slots and connections
    - see Appendix Function modules and communication processors supported by the S7-400H (Page 429)
  - CP 441: Limited by the number of connections
  - PROFIBUS and Ethernet CPs, including CP 443–5 Extended: Maximum 14, of which max. 10 CPs as DP masters

**Connectable OPs**
- 47

### Time

**Clock (real-time clock)**
- Yes

**Buffered**
- Yes

**Resolution**
- 1 ms
### Technical data

#### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Maximum deviation per day</th>
<th>1.7 s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power off (backed up)</td>
<td></td>
</tr>
<tr>
<td>Power on (not backed up)</td>
<td>8.6 s</td>
</tr>
<tr>
<td>Operating hours counter</td>
<td>16</td>
</tr>
<tr>
<td>Number/number range</td>
<td>0 to 15</td>
</tr>
<tr>
<td>Range of values</td>
<td>SFC 2, 3 and 4:0 to 32767 hours 0 to $2^{31} - 1$ hours when SFC 101 is used:</td>
</tr>
<tr>
<td>Granularity</td>
<td>1 hour</td>
</tr>
<tr>
<td>Retentive</td>
<td>Yes</td>
</tr>
<tr>
<td>Time synchronization</td>
<td>Yes</td>
</tr>
<tr>
<td>In AS, on MPI, DP and Ethernet MMS</td>
<td>As master or slave</td>
</tr>
<tr>
<td>On Ethernet over NTP</td>
<td>As client</td>
</tr>
<tr>
<td>Time difference in the system with synchronization via MPI</td>
<td>Max. 200 ms</td>
</tr>
<tr>
<td>Time difference in the system with synchronization via Ethernet</td>
<td>Max. 10 ms</td>
</tr>
</tbody>
</table>

#### S7 alarm functions

| Number of stations that can be logged on | 47          |
| For block-related alarms with SFC (Alarm_S/SQ and/or Alarm_D/DQ) |             |
| For block-related alarms with SFB (Notify, Notify_8, Alarm, Alarm_8, Alarm 8P) | 8           |
| Block-related alarms with SFC          | Yes         |
| Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks | Maximum 250 |
| Block-related alarms with SFB          | Yes         |
| Number of communication jobs for block-related alarms with SFC and blocks for S7 communication (programmable) | Maximum 600 |
| Default                               | 300         |
| Process control alarms                | Yes         |
| Number of archives that can be logged on simultaneously (SFB 37 AR_SEND) | 16          |

#### Test and commissioning functions

<table>
<thead>
<tr>
<th>Status/modify tag</th>
<th>Yes, maximum 16 tag tables</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tag</td>
<td>Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters</td>
</tr>
<tr>
<td>Number of tags</td>
<td>Maximum 70</td>
</tr>
<tr>
<td>Forcing</td>
<td>Yes</td>
</tr>
<tr>
<td>Tag</td>
<td>Inputs/outputs, bit memories, distributed I/O</td>
</tr>
<tr>
<td>Number of tags</td>
<td>Maximum 256</td>
</tr>
<tr>
<td>Status LED</td>
<td>Yes, FRCE-LED</td>
</tr>
</tbody>
</table>
### Block status
Yes, maximum 16 blocks at the same time

### Single-step
Yes

### Number of breakpoints
Maximum 16

### Diagnostics buffer
Yes

- **Number of entries**
  - Maximum 3200 (configurable)
- **Default**
  - 120

### Communication

#### PG/OP communication
Yes

#### Routing
Yes

#### S7 communication
Yes

- **User data per job**
  - Maximum 64 KB
- **of which consistent**
  - 1 tag (462 bytes)

#### S7 basic communication
No

#### Global data communication
No

#### S5-compatible communication
Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5

- **User data per job**
  - Maximum 8 KB
- **of which consistent**
  - 240 bytes

#### Number of simultaneous AG_SEND/AG_RECV jobs
Maximum 64/64, see CP manual

#### Standard communication (FMS)
Yes, via CP and loadable FB

#### Number of connection resources for S7 connections across all interfaces and CPs
48, incl. one each reserved for programming device and OP

#### Open IE communication over TCP/IP

- **Number of connections / access points, total**
  - Maximum 46
- **Possible port numbers**
  - 1 to 49151
- **Reserved port numbers**
  - 0 reserved
  - TCP 20, 21 FTP
  - TCP 25 SMTP
  - TCP 102 RFC1006
  - UDP 135 RPC-DCOM
  - UDP 161 SNMP_REQUEST
  - UDP 34962 PN IO
  - UDP 34963 PN IO
  - UDP 34964 PN IO
  - UDP 65532 NTP
  - UDP 65533 NTP
  - UDP 65534 NTP
  - UDP 65535 NTP

- **TCP/IP**
  - Yes, via integrated PROFINET interface and loadable FBs
- **Maximum number of connections**
  - 46
- **Data length, max.**
  - 32 KB
## Technical data

### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

<table>
<thead>
<tr>
<th>ISO-on-TCP</th>
<th>Yes (via integrated PROFINET interface or CP 443-1/ EX20/GX 20 and loadable FBs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Maximum number of connections</td>
<td>46</td>
</tr>
<tr>
<td>• Maximum data length via integrated PROFINET interface</td>
<td>32 KB</td>
</tr>
<tr>
<td>• Maximum data length via CP 443-1</td>
<td>1452 bytes</td>
</tr>
</tbody>
</table>

**UDP**

| Yes, via integrated PROFINET interface and loadable blocks |
| • Maximum number of connections | 46 |
| • Data length, max. | 1472 bytes |

### Interfaces

You may **not** configure the CPU as DP slave

#### 1st interface

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>X1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of interface</td>
<td>integrated</td>
</tr>
<tr>
<td>Physics</td>
<td>RS 485/PROFIBUS and MPI</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply to interface (15 V DC to 30 V DC)</td>
<td>Max. 150 mA</td>
</tr>
<tr>
<td>Number of connection resources</td>
<td>MPI: 32, DP: 16</td>
</tr>
<tr>
<td></td>
<td>If a diagnostics repeater is used on the segment, the number of connection resources on the segment is reduced by 1</td>
</tr>
</tbody>
</table>

#### Functionality

- **MPI**
  - Yes
- **PROFIBUS DP**
  - DP master

#### Utilities

- **PG/OP communication**
  - Yes
- **Routing**
  - Yes
- **S7 communication**
  - Yes
- **Global data communication**
  - No
- **S7 basic communication**
  - No
- **Transmission rates**
  - Maximum 12 Mbps

#### 1st interface in MPI mode

<table>
<thead>
<tr>
<th>Utilities</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PG/OP communication</strong></td>
</tr>
<tr>
<td><strong>Routing</strong></td>
</tr>
<tr>
<td><strong>S7 communication</strong></td>
</tr>
<tr>
<td><strong>Global data communication</strong></td>
</tr>
</tbody>
</table>

#### 1st interface in DP master mode

<table>
<thead>
<tr>
<th>Utilities</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PG/OP communication</strong></td>
</tr>
<tr>
<td><strong>Routing</strong></td>
</tr>
<tr>
<td><strong>S7 communication</strong></td>
</tr>
<tr>
<td><strong>Global data communication</strong></td>
</tr>
</tbody>
</table>
20.1 Technical specification of the CPU 412-5H PN/DP; (6ES7 412-5HK06-0AB0)

- S7 basic communication: No
- Constant bus cycle time: No
- Isochronous mode: No
- SYNC/FREEZE: No
- Enable/disable DP slaves: No
- Direct data exchange (cross-traffic): No

**Transmission rates**
- Maximum 12 Mbps

**Number of DP slaves**
- Maximum 32

**Number of slots per interface**
- Maximum 544

**Address range**
- Maximum 2 KB inputs / 2 KB outputs

**User data per DP slave**
- Maximum 244
- Maximum 244 bytes inputs
- Maximum 244 bytes outputs
- Maximum 244 slots
- Maximum 128 bytes per slot

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.

### 2nd interface

<table>
<thead>
<tr>
<th><strong>Interface designation</strong></th>
<th>X2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type of interface</strong></td>
<td>integrated</td>
</tr>
<tr>
<td><strong>Physics</strong></td>
<td>RS 485/Profibus</td>
</tr>
<tr>
<td><strong>Electrically isolated</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Power supply to interface (15 V DC to 30 V DC)</strong></td>
<td>Max. 150 mA</td>
</tr>
<tr>
<td><strong>Number of connection resources</strong></td>
<td>16</td>
</tr>
</tbody>
</table>

#### Functionality

- PROFIBUS DP: DP master

**2nd interface in DP master mode**

<table>
<thead>
<tr>
<th><strong>Utilities</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
</tr>
<tr>
<td>Routing</td>
</tr>
<tr>
<td>S7 communication</td>
</tr>
<tr>
<td>Global data communication</td>
</tr>
<tr>
<td>S7 basic communication</td>
</tr>
<tr>
<td>Constant bus cycle time</td>
</tr>
<tr>
<td>SYNC/FREEZE</td>
</tr>
<tr>
<td>Enable/disable DP slaves</td>
</tr>
</tbody>
</table>
## Technical data

### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct data exchange (cross-traffic)</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Up to 12 Mbps</td>
</tr>
<tr>
<td>Number of DP slaves</td>
<td>Maximum 64</td>
</tr>
<tr>
<td>Number of slots per interface</td>
<td>Maximum 1088</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 4 KB inputs / 4 KB outputs</td>
</tr>
<tr>
<td>User data per DP slave</td>
<td>Maximum 244 bytes</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 bytes inputs,</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 bytes outputs,</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 slots</td>
</tr>
<tr>
<td></td>
<td>Maximum 128 bytes per slot</td>
</tr>
</tbody>
</table>

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 4 KB inputs / 4 KB outputs) must not be exceeded in total across all 96 slaves.

### 3rd interface

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>X5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of interface</td>
<td>PROFINET</td>
</tr>
<tr>
<td>Physics</td>
<td>Ethernet RJ45</td>
</tr>
<tr>
<td></td>
<td>2 ports (switch)</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Autosensing (10/100 Mbps)</td>
<td>Yes</td>
</tr>
<tr>
<td>Autonegotiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Auto-crossover</td>
<td>Yes</td>
</tr>
<tr>
<td>Media redundancy</td>
<td>Yes</td>
</tr>
<tr>
<td>System redundancy</td>
<td>Yes</td>
</tr>
<tr>
<td>Changeover time on line interruption, typical</td>
<td>200 ms (PROFINET MRP)</td>
</tr>
<tr>
<td>Number of nodes on the ring, max.</td>
<td>50</td>
</tr>
<tr>
<td>Change of the IP address at runtime, supported</td>
<td>No</td>
</tr>
<tr>
<td>Keep Alive function, supported</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Functionality

- PROFINET: Yes

### Utilities

- PG communication: Yes
- OP communication: Yes
- S7 communication: Yes
- Maximum number of configurable connections: 48, one of each reserved for programming device and OP
- Maximum number of instances: 600
- S7 routing: Yes
- PROFINET IO controller: Yes
## Technical data

### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROFINET I-Device</td>
<td>No</td>
</tr>
<tr>
<td>PROFINET CBA</td>
<td>No</td>
</tr>
<tr>
<td>Open IE communication</td>
<td></td>
</tr>
<tr>
<td>over TCP/IP</td>
<td>Yes</td>
</tr>
<tr>
<td>ISO-on-TCP</td>
<td>Yes</td>
</tr>
<tr>
<td>UDP</td>
<td>Yes</td>
</tr>
<tr>
<td>Time synchronization</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### PROFINET IO

- **PNO ID (hexadecimal)**
  - Vendor ID: 0x002A
  - Device ID: 0x0102
- **Number of integrated PROFINET IO controllers**: 1
- **Number of PROFINET IO devices that can be connected**: 256
- **Number of connectable IO devices for RT of which are in line**: 256
- **Shared Device, supported**: No
- **Address range**: Maximum 8 KB inputs/outputs
- **Number of submodules**: Maximum 8192
- **Mixed modules count twice**: 1440 bytes
- **Maximum user data length, including user data qualifiers**: 1024 bytes
- **Maximum user data consistency, including user data qualifiers**: 1024 bytes
- **Send clock cycles**: 250 μs, 500 μs, 1 ms, 2 ms, 4 ms
- **Update Time**: 250 μs, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, and 512 ms
  - The minimum value depends on the communication slice set for PROFINET IO, the number of IO devices, and the amount of configured user data.
- **Maximum user data length**: 1024 bytes per address range
- **Maximum consistency of user data**: 1024 bytes per address range

### S7 protocol functions

- **PG functions**: Yes
- **OP functions**: Yes
- **IRT (Isochronous Real Time)**: No
- **Prioritized startup**: No
- **Accelerated (ASU) and Fast Startup Mode (FSU)**: No
- **Tool change**: No
- **Changing an IO device without Micro Memory Card or PG**: Yes

### 4th and 5th interface

- **Designation of the interfaces**: IF1, IF2
- **Type of interface**: Plug-in synchronization module (FOC)
### Technical data

#### 20.1 Technical specification of the CPU 412–5H PN/DP; (6ES7 412–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Usable interface module</th>
<th>Synchronization module IF 960 (only in redundant mode; in stand-alone mode the interface remains free/covered)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length of the synchronization cable</td>
<td>Max. 10 km</td>
</tr>
</tbody>
</table>

**Programming**

<table>
<thead>
<tr>
<th>Programming language</th>
<th>LAD, FBD, STL, SCL, CFC, Graph, HiGraph®</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction set</td>
<td>See instruction list</td>
</tr>
<tr>
<td>Nesting levels</td>
<td>7</td>
</tr>
<tr>
<td>System functions (SFC)</td>
<td>See instruction list</td>
</tr>
</tbody>
</table>

**Number of simultaneously active SFCs per segment**

- SFC 50 "RD_REC" 8
- SFC 58 "WR_REC" 8
- SFC 55 "WR_PARM" 8
- SFC 57 "PARM_MOD" 1
- SFC 56 "WR_DPARM" 2
- SFC 13 "DPNRM_DG" 8
- SFC 51 "RDSYSST" 8
- SFC 103 "DP_TOPOL" 1

The total number of active SFCs on all external segments may be four times more than on one single segment.

**System function blocks (SFB)**

<table>
<thead>
<tr>
<th>System function blocks (SFB)</th>
<th>See instruction list</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of simultaneously active SFBs per segment</td>
<td></td>
</tr>
</tbody>
</table>

- SFB 52 "RDREC" 8
- SFB 53 "WRREC" 8

The total number of active SFBs on all external segments may be four times more than on one single segment.

**User program protection**

- Password protection
- Access-protected blocks Yes, with S7 Block Privacy
- Access to consistent data in the process image Yes

**CiR synchronization time (in stand-alone mode)**

| Total load | 100 ms |

**Dimensions**

<table>
<thead>
<tr>
<th>Mounting dimensions W x H x D (mm)</th>
<th>50 x 290 x 219</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slots required</td>
<td>2</td>
</tr>
<tr>
<td>Weight</td>
<td>Approx. 995 g</td>
</tr>
</tbody>
</table>

**Voltagess and currents**

<table>
<thead>
<tr>
<th>Current consumption from S7-400 bus (5 V DC)</th>
<th>Typ. 1.6 A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max. 1.9 A</td>
</tr>
</tbody>
</table>
### Current consumption from S7-400 bus (24 V DC)

The CPU does not consume any current at 24 V; it only makes this voltage available on the MPI/DP interface.

<table>
<thead>
<tr>
<th>Total current consumption of the components connected to the MPI/DP interfaces, but maximum 150 mA per interface</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Current output to DP interface (5 V DC)</th>
<th>Max. 90 mA</th>
</tr>
</thead>
</table>
| Backup current | Typically 180 µA (up to 40 °C)  
Maximum 1000 µA |
| Maximum backup time | See Module Specifications Reference Manual, chapter 3.3. |
| Feed of external backup voltage to the CPU | 5 V DC to 15 V DC |
| Power loss | Typ. 7.5 W |
20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

<table>
<thead>
<tr>
<th>CPU and firmware version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order number</td>
</tr>
<tr>
<td>Firmware version</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Corresponding programming package</th>
<th>as of STEP7 V 5.5 SP2 HF 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>see also Preface (Page 19)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Work memory</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>Load memory</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>• Expandable FEPROM</td>
</tr>
<tr>
<td>• Expandable RAM</td>
</tr>
<tr>
<td>Battery backup</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Typical execution times</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execution times of</td>
</tr>
<tr>
<td>• Bit instructions</td>
</tr>
<tr>
<td>• Word instructions</td>
</tr>
<tr>
<td>• Fixed-point arithmetic</td>
</tr>
<tr>
<td>• Floating-point arithmetic</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timers/counters and their retentivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>S7 counters</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
</tr>
<tr>
<td>• Default</td>
</tr>
<tr>
<td>• Counting range</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IEC counters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFB</td>
</tr>
</tbody>
</table>

| S7 timers | 2048 |
|-----------|
| • Retentivity, configurable | From T 0 to T 2047 |
| • Default | No retentive timers |
| • Time range | 10 ms to 9990 s |

<table>
<thead>
<tr>
<th>IEC timers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Data areas and their retentivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total retentive data area (incl. bit memories, timers, counters)</td>
</tr>
</tbody>
</table>
## Technical data

### 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

<table>
<thead>
<tr>
<th>Bit memory</th>
<th>8 KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Retentivity, configurable</td>
<td>From MB 0 to MB 8191</td>
</tr>
<tr>
<td>• Preset retentivity</td>
<td>From MB 0 to MB 15</td>
</tr>
</tbody>
</table>

### Clock memories

- 8 (1 bit memory byte)

### Data blocks

- Maximum 6000 (DB 0 reserved)
- Number range 1 - 16000

### Local data (configurable)

- Maximum 16 KB
- Default 8 KB

#### Blocks

**OBs**
- See instruction list

**Number of free-cycle OBs**
- OB 1

**Number of time-of-day interrupt OBs**
- OB 10, 11, 12, 13

**Number of time-delay interrupt OBs**
- OB 20, 21, 22, 23

**Number of cyclic interrupts**
- OB 32, 33, 34, 35

**Number of process interrupt OBs**
- OB 40, 41, 42, 43

**Number of DPV1 interrupt OBs**
- OB 55, 56, 57

**Number of redundancy error OBs:**
- OB 70, 72

**Number of asynchronous error OBs**
- OB 80, 81, 82, 83, 84, 85, 86, 87, 88

**Number of restart OBs**
- OB 100, 102

**Number of synchronous error OBs**
- OB 121, 122

### Nesting depth

- Per priority class 24
- Additional ones in an error OB 1

### FBs

- Maximum 3000
- Number range 0 - 7999

### FCs

- Maximum 3000
- Number range 0 - 7999

### SDBs

- Maximum 2048

### Address ranges (I/O)

- Total I/O address range 8 KB/8 KB
- of those distributed Including diagnostic addresses, addresses for I/O interfaces, etc.

**MPI/DP interface**
- 2 KB/2 KB

**DP interface**
- 6 KB/6 KB

**Process image**
- 8 KB / 8 KB (configurable)
- Default 256 bytes/256 bytes
- Number of process image partitions Maximum 15
## 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

<table>
<thead>
<tr>
<th>Consistent data via PROFIBUS Via integrated PROFINET interface</th>
<th>Max. 244 bytes Max. 1024 bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Consistent data</td>
<td>Max. 244 bytes</td>
</tr>
</tbody>
</table>

### Access to consistent data in the process image

- Yes

### Digital channels

- Maximum 65536/ Maximum 65536

- • of those central Maximum 65536/ Maximum 65536

### Analog channels

- Maximum 4096/ Maximum 4096

- • of those central Maximum 4096/ Maximum 4096

#### Configuration

<table>
<thead>
<tr>
<th>Central controllers/expansion units</th>
<th>Maximum 2/20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multicomputing</td>
<td>No</td>
</tr>
<tr>
<td>Number of plug-in IMs (total)</td>
<td>Maximum 6</td>
</tr>
</tbody>
</table>

- • IM 460 Maximum 6

- • IM 463–2 Maximum 4, in stand-alone mode only

<table>
<thead>
<tr>
<th>Number of DP masters</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• integrated</td>
<td>2</td>
</tr>
<tr>
<td>• Via CP 443–5 Ext.</td>
<td>Maximum 10</td>
</tr>
</tbody>
</table>

| Number of plug-in S5 modules via adapter casing in the central controller | None |

- Operable function modules and communication processors

- • FM, CP (point-to-point) Limited by the number of slots and connections

  see Appendix Function modules and communication processors supported by the S7-400H (Page 429)

- • CP 441 Limited by the number of connections

- • PROFIBUS and Ethernet CPs, including CP 443–5 Extended Maximum 14, of which max. 10 CPs as DP masters

| Connectable OPs | 63 |

#### Time

<table>
<thead>
<tr>
<th>Clock</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Buffered</td>
<td>Yes</td>
</tr>
<tr>
<td>• Resolution</td>
<td>1 ms</td>
</tr>
<tr>
<td>Maximum deviation per day</td>
<td></td>
</tr>
<tr>
<td>• Power off (backed up)</td>
<td>1.7 s</td>
</tr>
<tr>
<td>• Power on (not backed up)</td>
<td>8.6 s</td>
</tr>
<tr>
<td>Operating hours counter</td>
<td>16</td>
</tr>
</tbody>
</table>

| • Number/number range | 0 to 15 |
### Technical data

#### 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

- **Range of values**: 0 to 32767 hours
  - 0 to \(2^{31} - 1\) hours when SFC 101 is used

- **Granularity**: 1 hour

- **Retentive**: Yes

- **Time synchronization**: Yes

- **In AS, on MPI and DP**: As master or slave

- **Time difference in the system with synchronization via MPI**: Max. 200 ms

- **Time difference in the system with synchronization via Ethernet**: Max. 10 ms

### S7 alarm functions

<table>
<thead>
<tr>
<th>Number of stations that can be logged on</th>
<th>For block-related alarms with SFC (Alarm_S/SQ and/or Alarm_D/DQ)</th>
<th>63</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>For block-related alarms with SFB (Notify, Notify_8, Alarm, Alarm_8, Alarm 8P)</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Block-related alarms with SFC</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks</td>
<td>Maximum 400</td>
</tr>
<tr>
<td></td>
<td>Block-related alarms with SFB</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Number of communication jobs for block-related alarms with SFC and blocks for S7 communication (programmable)</td>
<td>Maximum 2500</td>
</tr>
<tr>
<td></td>
<td>Default</td>
<td>900</td>
</tr>
<tr>
<td></td>
<td>Process control alarms</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Number of archives that can be logged on simultaneously (SFB 37 AR_SEND)</td>
<td>16</td>
</tr>
</tbody>
</table>

### Test and commissioning functions

<table>
<thead>
<tr>
<th>Status/modify tag</th>
<th>Yes, maximum 16 tag tables</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tag</td>
<td>Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters</td>
</tr>
<tr>
<td>Number of tags</td>
<td>Maximum 70</td>
</tr>
<tr>
<td>Forcing</td>
<td>Yes</td>
</tr>
<tr>
<td>Tag</td>
<td>Inputs/outputs, bit memories, distributed I/O</td>
</tr>
<tr>
<td>Number of tags</td>
<td>Maximum 256</td>
</tr>
<tr>
<td>Status LED</td>
<td>Yes, FRCE-LED</td>
</tr>
<tr>
<td>Block status</td>
<td>Yes, maximum 16 blocks at the same time</td>
</tr>
<tr>
<td>Single-step</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of breakpoints</td>
<td>Maximum 16</td>
</tr>
<tr>
<td>Diagnostic buffer</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of entries</td>
<td>Maximum 3200 (configurable)</td>
</tr>
<tr>
<td>Default</td>
<td>120</td>
</tr>
</tbody>
</table>
### Communication

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>User data per job</td>
<td>Maximum 64 KB</td>
</tr>
<tr>
<td>of which consistent</td>
<td>1 tag (462 bytes)</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S5-compatible communication</td>
<td>Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5</td>
</tr>
<tr>
<td>User data per job</td>
<td>Maximum 8 KB</td>
</tr>
<tr>
<td>of which consistent</td>
<td>240 bytes</td>
</tr>
<tr>
<td>Number of simultaneous AG_SEND/AG_RECV jobs</td>
<td>Maximum 64/64, see CP manual</td>
</tr>
<tr>
<td>Standard communication (FMS)</td>
<td>Yes, via CP and loadable FB</td>
</tr>
<tr>
<td>Number of connection resources for S7 connections across all interfaces and CPs</td>
<td>64, incl. one each reserved for programming device and OP</td>
</tr>
</tbody>
</table>

### Open IE communication over TCP/IP

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of connections / access points, total</td>
<td>Maximum 62</td>
</tr>
<tr>
<td>Possible port numbers</td>
<td>1 to 49151</td>
</tr>
<tr>
<td>Where parameters are assigned without specification of a port number, the system assigns a port from the dynamic port number range between 49152 and 65534</td>
<td></td>
</tr>
<tr>
<td>Reserved port numbers</td>
<td></td>
</tr>
<tr>
<td>TCP/IP</td>
<td>Yes, via integrated PROFINET interface and loadable FBs</td>
</tr>
<tr>
<td>Maximum number of connections</td>
<td>62</td>
</tr>
<tr>
<td>Data length, max.</td>
<td>32767 bytes</td>
</tr>
<tr>
<td>ISO-on-TCP</td>
<td>Yes (via integrated PROFINET interface or CP 443-1/EX20/GX 20 and loadable FBs)</td>
</tr>
<tr>
<td>Maximum number of connections</td>
<td>62</td>
</tr>
<tr>
<td>Maximum data length via integrated PROFINET interface</td>
<td>32767 bytes</td>
</tr>
<tr>
<td>Maximum data length via CP 443-1</td>
<td>1452 bytes</td>
</tr>
</tbody>
</table>
### Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

#### Interfaces

You may **not** configure the CPU as DP slave

<table>
<thead>
<tr>
<th><strong>1st interface</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Interface designation</strong></td>
<td>X1</td>
</tr>
<tr>
<td><strong>Type of interface</strong></td>
<td>integrated</td>
</tr>
<tr>
<td><strong>Physics</strong></td>
<td>RS 485/Profibus</td>
</tr>
<tr>
<td><strong>Electrically isolated</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Power supply to interface (15 V DC to 30 V DC)</strong></td>
<td>Max. 150 mA</td>
</tr>
</tbody>
</table>

#### Functionality

<table>
<thead>
<tr>
<th><strong>1st interface in MPI mode</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MPI</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PROFIBUS DP</strong></td>
<td>DP master</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Utilities</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PG/OP communication</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Routing</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>S7 communication</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Global data communication</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>S7 basic communication</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>Transmission rates</strong></td>
<td>Maximum 12 Mbps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>1st interface in DP master mode</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Utilities</strong></td>
<td></td>
</tr>
<tr>
<td><strong>PG/OP communication</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Routing</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>S7 communication</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Global data communication</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>S7 basic communication</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>Constant bus cycle time</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>SYNC/FREEZE</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>Enable/disable DP slaves</strong></td>
<td>No</td>
</tr>
<tr>
<td><strong>Direct data exchange (cross-traffic)</strong></td>
<td>No</td>
</tr>
</tbody>
</table>
## Technical data

### 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission rates</td>
<td>Maximum 12 Mbps</td>
</tr>
<tr>
<td>Number of DP slaves</td>
<td>Maximum 32</td>
</tr>
<tr>
<td>Number of slots per interface</td>
<td>Maximum 544</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 2 KB inputs / 2 KB outputs</td>
</tr>
<tr>
<td>User data per DP slave</td>
<td>Maximum 244 bytes</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 bytes inputs</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 bytes outputs</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 slots</td>
</tr>
<tr>
<td></td>
<td>Maximum 128 bytes per slot</td>
</tr>
</tbody>
</table>

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.

### 2nd interface

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>X2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of interface</td>
<td>integrated</td>
</tr>
<tr>
<td>Physics</td>
<td>RS 485/Profibus</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply to interface</td>
<td>Max. 150 mA</td>
</tr>
<tr>
<td>Number of connection resources</td>
<td>16</td>
</tr>
</tbody>
</table>

**Functionality**

- **PROFIBUS DP**
  - DP master

### 2nd interface in DP master mode

<table>
<thead>
<tr>
<th>Utilities</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Constant bus cycle time</td>
<td>No</td>
</tr>
<tr>
<td>SYNC/FREEZE</td>
<td>No</td>
</tr>
<tr>
<td>Enable/disable DP slaves</td>
<td>No</td>
</tr>
<tr>
<td>Direct data exchange (cross-traffic)</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Up to 12 Mbps</td>
</tr>
<tr>
<td>Number of DP slaves</td>
<td>Maximum 96</td>
</tr>
<tr>
<td>Number of slots per interface</td>
<td>Maximum 1632</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 6 KB inputs / 6 KB outputs</td>
</tr>
</tbody>
</table>
### 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

- **User data per DP slave**
  - Maximum 244 bytes
  - Maximum 244 bytes inputs
  - Maximum 244 bytes outputs
  - Maximum 244 slots
  - Maximum 128 bytes per slot

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 6 KB inputs / 6 KB outputs) must not be exceeded in total across all 96 slaves.

<table>
<thead>
<tr>
<th>3rd interface</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface designation</td>
<td>X5</td>
</tr>
<tr>
<td>Type of interface</td>
<td>PROFINET</td>
</tr>
<tr>
<td>Physics</td>
<td>Ethernet RJ45 2 ports (switch)</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Autosensing (10/100 Mbps)</td>
<td>Yes</td>
</tr>
<tr>
<td>Autonegotiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Auto-crossover</td>
<td>Yes</td>
</tr>
<tr>
<td>Media redundancy</td>
<td>Yes</td>
</tr>
<tr>
<td>System redundancy</td>
<td>Yes</td>
</tr>
<tr>
<td>Changeover time on line interruption, typical</td>
<td>200 ms (PROFINET MRP)</td>
</tr>
<tr>
<td>Number of nodes on the ring, max.</td>
<td>50</td>
</tr>
<tr>
<td>Change of the IP address at runtime, supported</td>
<td>No</td>
</tr>
<tr>
<td>Keep Alive function, supported</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Functionality**
- **PROFINET**
  - Yes

**Utilities**
- **PG communication**
  - Yes
- **OP communication**
  - Yes
- **S7 communication**
  - Maximum number of configurable connections
    - Yes
  - Maximum number of instances
    - 64, one of each reserved for programming device and OP
    - 2500
- **S7 routing**
  - Yes
- **PROFINET IO controller**
  - Yes
- **PROFINET I-Device**
  - No
- **PROFINET CBA**
  - No
- **Open IE communication**
  - over TCP/IP
    - Yes
  - ISO-on-TCP
    - Yes
### 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

- UDP: Yes
- Time Synchronization: Yes

#### PROFINET IO

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PNO ID (hexadecimal)</td>
<td>Vendor ID: 0x002A, Device ID: 0x0102</td>
</tr>
<tr>
<td>Number of integrated PROFINET IO controllers</td>
<td>1</td>
</tr>
<tr>
<td>Number of PROFINET IO devices that can be</td>
<td>256</td>
</tr>
<tr>
<td>connected</td>
<td></td>
</tr>
<tr>
<td>Number of connectable IO devices for RT</td>
<td>256</td>
</tr>
<tr>
<td>of which are in line</td>
<td>256</td>
</tr>
<tr>
<td>Shared Device, supported</td>
<td>No</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 8 KB inputs/outputs</td>
</tr>
<tr>
<td>Number of submodules</td>
<td>Maximum 8192</td>
</tr>
<tr>
<td></td>
<td>Mixed modules count twice</td>
</tr>
<tr>
<td>Maximum user data length, including user data</td>
<td>1440 bytes</td>
</tr>
<tr>
<td>qualifications</td>
<td></td>
</tr>
<tr>
<td>Maximum user data consistency, including</td>
<td>1024 bytes</td>
</tr>
<tr>
<td>user data qualifications</td>
<td></td>
</tr>
<tr>
<td>Send clock cycles</td>
<td>250 µs, 500 µs, 1 ms, 2 ms, 4 ms</td>
</tr>
<tr>
<td>Update Time</td>
<td>250 µs, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, and 512 ms</td>
</tr>
<tr>
<td></td>
<td>The minimum value depends on the</td>
</tr>
<tr>
<td></td>
<td>communication slice set for PROFINET IO,</td>
</tr>
<tr>
<td></td>
<td>the number of IO devices, and the amount</td>
</tr>
<tr>
<td></td>
<td>of configured user data.</td>
</tr>
<tr>
<td>IRT (Isochronous Real Time)</td>
<td>No</td>
</tr>
<tr>
<td>S7 protocol functions</td>
<td></td>
</tr>
<tr>
<td>• PG functions</td>
<td>Yes</td>
</tr>
<tr>
<td>• OP functions</td>
<td>Yes</td>
</tr>
<tr>
<td>Prioritized startup</td>
<td>No</td>
</tr>
<tr>
<td>Accelerated (ASU) and Fast Startup Mode (FSU)</td>
<td>No</td>
</tr>
<tr>
<td>Tool change</td>
<td>No</td>
</tr>
<tr>
<td>Changing an IO device without Micro Memory</td>
<td>Yes</td>
</tr>
<tr>
<td>Card or PG</td>
<td></td>
</tr>
</tbody>
</table>

#### 4th and 5th interface

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Designation of the interfaces</td>
<td>IF1, IF2</td>
</tr>
<tr>
<td>Type of interface</td>
<td>Plug-in synchronization module (FOC)</td>
</tr>
<tr>
<td>Usable interface module</td>
<td>Synchronization module IF 960 (only in redundant mode; in stand-alone mode the interface remains free/covered)</td>
</tr>
<tr>
<td>Length of the synchronization cable</td>
<td>Maximum 10 km</td>
</tr>
</tbody>
</table>

#### Programming

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming language</td>
<td>LAD, FBD, STL, SCL, CFC, Graph, HiGraph®</td>
</tr>
<tr>
<td>Instruction set</td>
<td>See instruction list</td>
</tr>
<tr>
<td>Nesting levels</td>
<td>7</td>
</tr>
</tbody>
</table>
## 20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)

### System functions (SFC)

<table>
<thead>
<tr>
<th>Number of simultaneously active SFCs per segment</th>
<th>See instruction list</th>
</tr>
</thead>
<tbody>
<tr>
<td>• SFC 59 &quot;RD_REC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 58 &quot;WR_REC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 55 &quot;WR_PARM&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 57 &quot;PARM_MOD&quot;</td>
<td>1</td>
</tr>
<tr>
<td>• SFC 56 &quot;WR_DPARM&quot;</td>
<td>2</td>
</tr>
<tr>
<td>• SFC 13 &quot;DPNRM_DG&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 51 &quot;RDSYSST&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 103 &quot;DP_TOPOL&quot;</td>
<td>1</td>
</tr>
</tbody>
</table>

The total number of active SFCs on all external segments may be four times more than on one single segment.

### System function blocks (SFB)

<table>
<thead>
<tr>
<th>Number of simultaneously active SFBs per segment</th>
<th>See instruction list</th>
</tr>
</thead>
<tbody>
<tr>
<td>• SFB 52 &quot;RDREC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFB 53 &quot;WRREC&quot;</td>
<td>8</td>
</tr>
</tbody>
</table>

The total number of active SFBs on all external segments may be four times more than on one single segment.

### User program protection

- **Password protection**
  - Access-protected blocks: Yes, with S7 Block Privacy
  - Access to consistent data in the process image: Yes

### CiR synchronization time (in stand-alone mode)

| Total load | 100 ms |

### Dimensions

<table>
<thead>
<tr>
<th>Mounting dimensions W x H x D (mm)</th>
<th>50 x 290 x 219</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slots required</td>
<td>2</td>
</tr>
<tr>
<td>Weight</td>
<td>Approx. 995 g</td>
</tr>
</tbody>
</table>

### Voltages and currents

- **Current consumption from S7–400 bus (5 V DC)**
  - Typ. 1.6 A
  - Max. 1.9 A

- **Current consumption from S7-400 bus (24 V DC)**
  - The CPU does not consume any current at 24 V, it only makes this voltage available on the MPI/DP interface.
  - Total current consumption of the components connected to the MPI/DP interfaces, but maximum 150 mA per interface

- **Current output to DP interface (5 V DC)**
  - Max. 90 mA

- **Backup current**
  - Typically 180 µA (up to 40 °C)
  - Maximum 1000 µA

- **Maximum backup time**
  - See Module Specifications Reference Manual, chapter 3.3.

- **Feed of external backup voltage to the CPU**
  - 5 V DC to 15 V DC

- **Power loss**
  - Typ. 7.5 W
Technical data

20.2 Technical specifications of the CPU 414–5H PN/DP; (6ES7 414–5HM06–0AB0)
## 20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

### CPU and firmware version

<table>
<thead>
<tr>
<th>Order number</th>
<th>6ES7 416–5HS06–0AB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Firmware version</td>
<td>V 6.0</td>
</tr>
</tbody>
</table>

Corresponding programming package: as of STEP7 V 5.5 SP2 HF 1

### Memory

<table>
<thead>
<tr>
<th>Work memory</th>
<th>6 MB for code</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10 MB for data</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Load memory</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>integrated</td>
<td>1 MB RAM</td>
</tr>
</tbody>
</table>

- Expandable FEPROM
  - With memory card (FLASH) 1 MB to 64 MB

- Expandable RAM
  - With memory card (RAM) 256 KB to 64 MB

**Battery backup**: Yes, all data

### Typical execution times

<table>
<thead>
<tr>
<th>Execution times of</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit instructions</td>
<td>12.5 ns</td>
</tr>
<tr>
<td>Word instructions</td>
<td>12.5 ns</td>
</tr>
<tr>
<td>Fixed-point arithmetic</td>
<td>12.5 ns</td>
</tr>
<tr>
<td>Floating-point arithmetic</td>
<td>25 ns</td>
</tr>
</tbody>
</table>

### Timers/counters and their retentivity

**S7 counters**: 2048

- Retentivity, configurable: From C 0 to C 2047
- Default: From C 0 to C 7
- Counting range: 0 to 999

**IEC counters**: Yes

<table>
<thead>
<tr>
<th>Type</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SFB</td>
<td></td>
</tr>
</tbody>
</table>

**S7 timers**: 2048

- Retentivity, configurable: From T 0 to T 2047
- Default: No retentive timers
- Time range: 10 ms to 9990 s

**IEC timers**: Yes

<table>
<thead>
<tr>
<th>Type</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SFB</td>
<td></td>
</tr>
</tbody>
</table>

### Data areas and their retentivity

**Total retentive data area (incl. bit memories, timers, counters)**

**Total work and load memory (with backup battery)**
## Bit memory
- 16 KB

### Retentivity, configurable
- From MB 0 to MB 16383

### Preset retentivity
- From MB 0 to MB 15

## Clock memories
- 8 (1 bit memory byte)

## Data blocks
- Maximum 16000 (DB 0 reserved)
- Number range 1 - 16000

### Size
- Maximum 64 KB

## Local data (configurable)
- Maximum 64 KB

### Default
- 32 KB

### Blocks

#### OBs
- Maximum 64 KB

- **Number of free-cycle OBs**: OB 1
- **Number of time-of-day interrupt OBs**: OB 10, 11, 12, 13, 14, 15, 16, 17
- **Number of time-delay interrupt OBs**: OB 20, 21, 22, 23
- **Number of cyclic interrupts**: OB 30, 31, 32, 33, 34, 35, 36, 37, 38
- **Number of process interrupt OBs**: OB 40, 41, 42, 43, 44, 45, 46, 47
- **Number of DPV1 interrupt OBs**: OB 55, 56, 57
- **Number of redundancy error OBs**: OB 70, 72
- **Number of asynchronous error OBs**: OB 80, 81, 82, 83, 84, 85, 86, 87, 88
- **Number of restart OBs**: OB 100, 102
- **Number of synchronous error OBs**: OB 121, 122

#### Nesting depth
- Per priority class: 24
- Additional ones in an error OB: 2

#### FBs
- Maximum 8000
- Number range 0 - 7999

### Size
- Maximum 64 KB

#### FCs
- Maximum 8000
- Number range 0 - 7999

### Size
- Maximum 64 KB

#### SDBs
- Maximum 2048

### Address ranges (I/O)

- **Total I/O address range**: 16 KB/16 KB
- **of those distributed**: Including diagnostic addresses, addresses for I/O interfaces, etc.
- **MPI/DP interface**: 2 KB/2 KB
- **DP interface**: 8 KB/8 KB
- **Process image**: 16 KB/16 KB (configurable)
- **Default**: 1024 bytes/1024 bytes
- **Number of process image partitions**: Maximum 15
## Technical data

### 20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

<table>
<thead>
<tr>
<th>Consistent data via PROFIBUS</th>
<th>Max. 244 bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via integrated PROFINET interface</td>
<td>Max. 1024 bytes</td>
</tr>
<tr>
<td>Access to consistent data in the process image</td>
<td>Yes</td>
</tr>
<tr>
<td>Digital channels</td>
<td>Maximum 131072/Maximum 131072</td>
</tr>
<tr>
<td>• of those central</td>
<td>Maximum 131072/Maximum 131072</td>
</tr>
<tr>
<td>Analog channels</td>
<td>Maximum 8192/Maximum 8192</td>
</tr>
<tr>
<td>• of those central</td>
<td>Maximum 8192/Maximum 8192</td>
</tr>
</tbody>
</table>

### Configuration

<table>
<thead>
<tr>
<th>Central controllers/expansion units</th>
<th>Maximum 2/20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multicomputing</td>
<td>No</td>
</tr>
<tr>
<td>Number of plug-in IMs (total)</td>
<td>Maximum 6</td>
</tr>
<tr>
<td>• IM 460</td>
<td>Maximum 6</td>
</tr>
<tr>
<td>• IM 463–2</td>
<td>Maximum 4, in stand-alone mode only</td>
</tr>
<tr>
<td>Number of DP masters</td>
<td>2</td>
</tr>
<tr>
<td>• integrated</td>
<td></td>
</tr>
<tr>
<td>• Via CP 443–5 Ext.</td>
<td>Maximum 10</td>
</tr>
<tr>
<td>Number of plug-in S5 modules via adapter casing (in the central controller)</td>
<td>None</td>
</tr>
<tr>
<td>Operable function modules and communication processors</td>
<td></td>
</tr>
<tr>
<td>• FM, CP (point-to-point)</td>
<td>Limited by the number of slots and connections</td>
</tr>
<tr>
<td>see Appendix Function modules and communication processors supported by the S7-400H (Page 429)</td>
<td></td>
</tr>
<tr>
<td>• CP 441</td>
<td>Limited by the number of connections</td>
</tr>
<tr>
<td>• PROFIBUS and Ethernet CPs, including CP 443–5 Extended</td>
<td>Maximum 14, of which max. 10 CPs as DP masters</td>
</tr>
</tbody>
</table>

### Connectable OPs

| Connectable OPs | 95 |

### Time

<table>
<thead>
<tr>
<th>Clock</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Buffered</td>
<td>Yes</td>
</tr>
<tr>
<td>• Resolution</td>
<td>1 ms</td>
</tr>
<tr>
<td>Maximum deviation per day</td>
<td></td>
</tr>
<tr>
<td>• Power off (backed up)</td>
<td>1.7 s</td>
</tr>
<tr>
<td>• Power on (not backed up)</td>
<td>8.6 s</td>
</tr>
</tbody>
</table>
## Technical data

### 20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

<table>
<thead>
<tr>
<th>Operating hours counter</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Number/number range</td>
<td>0 to 15</td>
</tr>
<tr>
<td>• Range of values</td>
<td>0 to 32767 hours</td>
</tr>
<tr>
<td></td>
<td>0 to 2^{31} -1 hours when SFC 101 is used</td>
</tr>
<tr>
<td>• Granularity</td>
<td>1 hour</td>
</tr>
<tr>
<td>• Retentive</td>
<td>Yes</td>
</tr>
</tbody>
</table>

#### Time synchronization

- **In AS, on MPI and DP**: As master or slave
- **Time difference in the system with synchronization via MPI**: Max. 200 ms
- **Time difference in the system with synchronization via Ethernet**: Max. 10 ms

#### Operating hours counter

- **Number/number range**: 0 to 15
- **Range of values**: 0 to 32767 hours (0 to 2^{31} -1 hours when SFC 101 is used)
- **Granularity**: 1 hour
- **Retentive**: Yes

#### S7 alarm functions

<table>
<thead>
<tr>
<th>Number of stations that can be logged on</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>For block-related alarms with SFC (Alarm_S/SQ and/or Alarm_D/DQ)</td>
<td>95</td>
</tr>
<tr>
<td>For block-related alarms with SFB (Notify, Notify_8, Alarm, Alarm_8, Alarm 8P)</td>
<td>16</td>
</tr>
<tr>
<td>Block-related alarms with SFC</td>
<td>Yes</td>
</tr>
<tr>
<td>• Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks</td>
<td>Maximum 1000</td>
</tr>
<tr>
<td>Block-related alarms with SFB</td>
<td>Yes</td>
</tr>
<tr>
<td>• Number of communication jobs for block-related alarms with SFC and blocks for S7 communication (programmable)</td>
<td>Maximum 10000</td>
</tr>
<tr>
<td>• Default</td>
<td>1200</td>
</tr>
</tbody>
</table>

#### Process control alarms

- **Number of archives that can be logged on simultaneously (SFB 37 AR_SEND)**: 64

#### Test and commissioning functions

<table>
<thead>
<tr>
<th>Status/modify tag</th>
<th>Yes, maximum 16 tag tables</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Tag</td>
<td>Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters</td>
</tr>
<tr>
<td>• Number of tags</td>
<td>Maximum 70</td>
</tr>
</tbody>
</table>

#### Forcing

- **Tag**: Inputs/outputs, bit memories, distributed I/O
- **Number of tags**: Maximum 512

#### Status LED

- **Yes, FRCE-LED**

#### Block status

- **Yes, maximum 16 blocks at the same time**

#### Single-step

- **Yes**

#### Number of breakpoints

- **Maximum 16**

#### Diagnostic buffer

- **Yes**
<table>
<thead>
<tr>
<th><strong>Number of entries</strong></th>
<th>Maximum 3200 (configurable)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Default</strong></td>
<td>120</td>
</tr>
</tbody>
</table>

**Communication**

- **PG/OP communication**: Yes
- **Routing**: Yes
- **S7 communication**: Yes
- **User data per job**: Maximum 64 KB
- **of which consistent**: 1 tag (462 bytes)
- **S7 basic communication**: No
- **Global data communication**: No
- **S5-compatible communication**: Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5
- **User data per job**: Maximum 8 KB
- **of which consistent**: 240 bytes
- **Number of simultaneous AG_SEND/AG_RECV jobs**: Maximum 64/64, see CP manual
- **Standard communication (FMS)**: Yes, via CP and loadable FB
- **Number of connection resources for S7 connections across all interfaces and CPs**: 96, incl. one each reserved for programming device and OP, 62 of which fault-tolerant connections

**Open IE communication over TCP/IP**

- **Number of connections / access points, total**: Maximum 94
- **Possible port numbers**: 1 to 49151

Where parameters are assigned without specification of a port number, the system assigns a port from the dynamic port number range between 49152 and 65534

**Reserved port numbers**

- TCP 20, 21 FTP
- TCP 25 SMTP
- TCP 102 RFC1006
- UDP 135 RPC-DCOM
- UDP 161 SNMP_REQUEST
- UDP 34962 PN IO
- UDP 34963 PN IO
- UDP 34964 PN IO
- UDP 65532 NTP
- UDP 65533 NTP
- UDP 65534 NTP
- UDP 65535 NTP

**TCP/IP**

- **Yes, via integrated PROFINET interface and loadable FBs**
- **Maximum number of connections**: 94
- **Data length, max.**: 32767 bytes

**ISO-on-TCP**

- **Yes (via integrated PROFINET interface or CP 443-1/EX20/GX 20 and loadable FBs)**
- **Maximum number of connections**: 94
Technical data
20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

- **Maximum data length via integrated PROFINET interface**: 32767 bytes
- **Maximum data length via CP 443-1**: 1452 bytes
- **UDP**: Yes, via integrated PROFINET interface and loadable blocks
- **Maximum number of connections**: 94
- **Data length, max.**: 1472 bytes

**Interfaces**

You may **not** configure the CPU as DP slave

**1st interface**

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>Type of interface</th>
<th>Physics</th>
<th>Electrically isolated</th>
<th>Power supply to interface (15 V DC to 30 V DC)</th>
<th>Number of connection resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>integrated</td>
<td>RS 485/Profibus</td>
<td>Yes</td>
<td>Max. 150 mA</td>
<td>MPI: 44, DP: 32</td>
</tr>
</tbody>
</table>

**Functionality**

- **MPI**: Yes
- **PROFIBUS DP**: DP master

**1st interface in MPI mode**

<table>
<thead>
<tr>
<th>Utilities</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Maximum 12 Mbps</td>
</tr>
</tbody>
</table>

**1st interface in DP master mode**

- **Utilities**:  
- **PG/OP communication**: Yes  
- **Routing**: Yes  
- **S7 communication**: Yes  
- **Global data communication**: No  
- **S7 basic communication**: No  
- **Constant bus cycle time**: No  
- **SYNC/FREEZE**: No
### 20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

- **Enable/disable DP slaves**: No
- **Direct data exchange (cross-traffic)**: No
- **Transmission rates**: Maximum 12 Mbps
- **Number of DP slaves**: Maximum 32
- **Number of slots per interface**: Maximum 544
- **Address range**: Maximum 2 KB inputs / 2 KB outputs
- **User data per DP slave**: Maximum 244 bytes
  - Maximum 244 bytes inputs
  - Maximum 244 bytes outputs
  - Maximum 244 slots
  - Maximum 128 bytes per slot

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.

#### 2nd interface

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>X2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physics</td>
<td>RS 485/Profibus</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply to interface (15 V DC to 30 V DC)</td>
<td>Max. 150 mA</td>
</tr>
<tr>
<td>Number of connection resources</td>
<td>32</td>
</tr>
</tbody>
</table>

#### Functionality

- **PROFIBUS DP**: DP master

#### 2nd interface in DP master mode

<table>
<thead>
<tr>
<th>Utilities</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Constant bus cycle time</td>
<td>No</td>
</tr>
<tr>
<td>SYNC/FREEZE</td>
<td>No</td>
</tr>
<tr>
<td>Enable/disable DP slaves</td>
<td>No</td>
</tr>
<tr>
<td>Direct data exchange (cross-traffic)</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Up to 12 Mbps</td>
</tr>
<tr>
<td>Number of DP slaves</td>
<td>Maximum 125</td>
</tr>
<tr>
<td>Number of slots per interface</td>
<td>Maximum 2173</td>
</tr>
</tbody>
</table>
### 20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

#### Address range
- Maximum 8 KB inputs / 8 KB outputs

#### User data per DP slave
- Maximum 244 bytes
- Maximum 244 bytes inputs
- Maximum 244 bytes outputs
- Maximum 244 slots
- Maximum 128 bytes per slot

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 8 KB inputs / 8 KB outputs) must not be exceeded in total across all 125 slaves.

<table>
<thead>
<tr>
<th>3rd interface</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Interface designation</strong></td>
</tr>
<tr>
<td><strong>Type of interface</strong></td>
</tr>
<tr>
<td><strong>Physics</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Electrically isolated</strong></td>
</tr>
<tr>
<td><strong>Autosensing (10/100 Mbps)</strong></td>
</tr>
<tr>
<td><strong>Autonegotiation</strong></td>
</tr>
<tr>
<td><strong>Auto-crossover</strong></td>
</tr>
<tr>
<td><strong>Media redundancy</strong></td>
</tr>
<tr>
<td><strong>System redundancy</strong></td>
</tr>
<tr>
<td><strong>Changeover time on line interruption, typical</strong></td>
</tr>
<tr>
<td><strong>Number of nodes on the ring, max.</strong></td>
</tr>
<tr>
<td><strong>Change of the IP address at runtime, supported</strong></td>
</tr>
<tr>
<td><strong>Keep Alive function, supported</strong></td>
</tr>
</tbody>
</table>

**Functionality**
- PROFINET Yes

**Utilities**
- PG communication Yes
- OP communication Yes
- S7 communication
  - Maximum number of configurable connections: Yes
  - Maximum number of instances: 96, one of each reserved for programming device and OP 10000
- S7 routing Yes
- PROFINET IO controller Yes
- PROFINET I-Device No
- PROFINET CBA No
- Open IE communication
  - over TCP/IP Yes
  - ISO-on-TCP Yes
## Technical data

### 20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>UDP</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Time synchronization</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PROFINET IO</strong></td>
<td></td>
</tr>
<tr>
<td>PNO ID (hexadecimal)</td>
<td>Vendor ID: 0x002A</td>
</tr>
<tr>
<td></td>
<td>Device ID: 0x0102</td>
</tr>
<tr>
<td>Number of integrated PROFINET IO controllers</td>
<td>1</td>
</tr>
<tr>
<td>Number of PROFINET IO devices that can be</td>
<td>256</td>
</tr>
<tr>
<td>connected</td>
<td></td>
</tr>
<tr>
<td>Number of connectable IO devices for RT of</td>
<td>256</td>
</tr>
<tr>
<td>which are in line</td>
<td>256</td>
</tr>
<tr>
<td>Shared Device, supported</td>
<td>No</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 8 KB inputs/outputs</td>
</tr>
<tr>
<td>Number of submodules</td>
<td>Maximum 8192</td>
</tr>
<tr>
<td></td>
<td>Mixed modules count twice</td>
</tr>
<tr>
<td>Maximum user data length, including user</td>
<td>1440 bytes</td>
</tr>
<tr>
<td>data qualifiers</td>
<td></td>
</tr>
<tr>
<td>Maximum user data consistency, including</td>
<td>1024 bytes</td>
</tr>
<tr>
<td>user data qualifiers</td>
<td></td>
</tr>
<tr>
<td>Send clock cycles</td>
<td>250 μs, 500 μs, 1 ms, 2 ms, 4</td>
</tr>
<tr>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Update Time</td>
<td>250 μs, 0.5 ms, 1 ms, 2 ms, 4</td>
</tr>
<tr>
<td></td>
<td>ms, 8 ms, 16 ms, 32 ms, 64</td>
</tr>
<tr>
<td></td>
<td>ms, 128 ms, 256 ms, 512 ms</td>
</tr>
<tr>
<td>The minimum value depends on the</td>
<td></td>
</tr>
<tr>
<td>communication slice set for PROFINET IO, the</td>
<td></td>
</tr>
<tr>
<td>number of IO devices, and the amount of</td>
<td></td>
</tr>
<tr>
<td>configured user data.</td>
<td></td>
</tr>
<tr>
<td>S7 protocol functions</td>
<td></td>
</tr>
<tr>
<td><strong>PG functions</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>OP functions</strong></td>
<td>Yes</td>
</tr>
<tr>
<td>IRT (Isochronous Real Time)</td>
<td>No</td>
</tr>
<tr>
<td>Prioritized startup</td>
<td>No</td>
</tr>
<tr>
<td>Accelerated (ASU) and Fast Startup Mode (FSU)</td>
<td>No</td>
</tr>
<tr>
<td>Tool change</td>
<td>No</td>
</tr>
<tr>
<td>Changing an IO device without Micro Memory</td>
<td>Yes</td>
</tr>
<tr>
<td>Card or PG</td>
<td></td>
</tr>
<tr>
<td><strong>4th and 5th interface</strong></td>
<td></td>
</tr>
<tr>
<td>Designation of the interfaces</td>
<td>IF1, IF2</td>
</tr>
<tr>
<td>Type of interface</td>
<td>Plug-in synchronization module (FOC)</td>
</tr>
<tr>
<td>Usable interface module</td>
<td>Synchronization module IF 960 (only in redundant mode; in stand-alone mode the interface remains free/covered)</td>
</tr>
<tr>
<td>Length of the synchronization cable</td>
<td>Maximum 10 km</td>
</tr>
<tr>
<td><strong>Programming</strong></td>
<td></td>
</tr>
<tr>
<td>Programming language</td>
<td>LAD, FBD, STL, SCL, CFC, Graph, HiGraph®</td>
</tr>
<tr>
<td>Instruction set</td>
<td>See instruction list</td>
</tr>
<tr>
<td>Nesting levels</td>
<td>7</td>
</tr>
</tbody>
</table>

---

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Technical data

20.3 Technical specifications of the CPU 416–5H PN/DP; (6ES7 416–5HS06–0AB0)

<table>
<thead>
<tr>
<th>System functions (SFC)</th>
<th>See instruction list</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of simultaneously active SFCs per segment</td>
<td></td>
</tr>
<tr>
<td>• SFC 59 &quot;RD_REC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 58 &quot;WR_REC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 55 &quot;WR_PARM&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 57 &quot;PARM_MOD&quot;</td>
<td>1</td>
</tr>
<tr>
<td>• SFC 56 &quot;WR_DPARM&quot;</td>
<td>2</td>
</tr>
<tr>
<td>• SFC 13 &quot;DPNRM_DG&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 51 &quot;RDSYSST&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 103 &quot;DP_TOPOL&quot;</td>
<td>1</td>
</tr>
</tbody>
</table>

The total number of active SFCs on all external segments may be four times more than on one single segment.

<table>
<thead>
<tr>
<th>System function blocks (SFB)</th>
<th>See instruction list</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of simultaneously active SFBs per segment</td>
<td></td>
</tr>
<tr>
<td>• SFB 52 &quot;RDREC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFB 53 &quot;WRREC&quot;</td>
<td>8</td>
</tr>
</tbody>
</table>

The total number of active SFBs on all external segments may be four times more than on one single segment.

User program protection | Password protection
Access-protected blocks | Yes, with S7 Block Privacy
Access to consistent data in the process image | Yes

**CIR synchronization time (in stand-alone mode)**

Total load | 100 ms

**Dimensions**

Mounting dimensions W x H x D (mm) | 50 x 290 x 219
Slots required | 2
Weight | Approx. 995 g

**Voltages and currents**

Current consumption from S7–400 bus (5 V DC) | Typ. 1.6 A Max. 1.9 A

Current consumption from S7–400 bus (24 V DC) | Total current consumption of the components connected to the MPI/DP interfaces, but maximum 150 mA per interface
The CPU does not consume any current at 24 V, it only makes this voltage available on the MPI/DP interface.

Current output to DP interface (5 V DC) | Max. 90 mA
Backup current | Typically 180 µA (up to 40 °C) Maximum 1000 µA
Maximum backup time | See Module Specifications Reference Manual, chapter 3.3.
Feed of external backup voltage to the CPU | 5 V DC to 15 V DC
Power loss | Typ. 7.5 W
## 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>CPU and firmware version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order number</td>
</tr>
<tr>
<td>• Firmware version</td>
</tr>
<tr>
<td>Corresponding programming package</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Work memory</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Load memory</td>
</tr>
<tr>
<td>• integrated</td>
</tr>
<tr>
<td>• Expandable FEPROM</td>
</tr>
<tr>
<td>• Expandable RAM</td>
</tr>
<tr>
<td>Battery backup</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Typical execution times</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execution times of</td>
</tr>
<tr>
<td>• Bit instructions</td>
</tr>
<tr>
<td>• Word instructions</td>
</tr>
<tr>
<td>• Fixed-point arithmetic</td>
</tr>
<tr>
<td>• Floating-point arithmetic</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timers/counters and their retentivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>S7 counters</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
</tr>
<tr>
<td>• Default</td>
</tr>
<tr>
<td>• Counting range</td>
</tr>
<tr>
<td>IEC counters</td>
</tr>
<tr>
<td>• Type</td>
</tr>
<tr>
<td>S7 timers</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
</tr>
<tr>
<td>• Default</td>
</tr>
<tr>
<td>• Time range</td>
</tr>
<tr>
<td>IEC timers</td>
</tr>
<tr>
<td>• Type</td>
</tr>
</tbody>
</table>

<p>| Data areas and their retentivity       |</p>
<table>
<thead>
<tr>
<th>Total retentive data area (incl. bit memories, timers, counters)</th>
<th>Total work and load memory (with backup battery)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit memory</td>
<td>16 KB</td>
</tr>
<tr>
<td>• Retentivity, configurable</td>
<td>From MB 0 to MB 16383</td>
</tr>
<tr>
<td>• Preset retentivity</td>
<td>From MB 0 to MB 15</td>
</tr>
<tr>
<td>Clock memories</td>
<td>8 (1 bit memory byte)</td>
</tr>
<tr>
<td>Data blocks</td>
<td>Maximum 16000 (DB 0 reserved)</td>
</tr>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
<tr>
<td>Local data (configurable)</td>
<td>Maximum 64 KB</td>
</tr>
<tr>
<td>• Default</td>
<td>32 KB</td>
</tr>
</tbody>
</table>

### Blocks

<table>
<thead>
<tr>
<th>OBs</th>
<th>See instruction list</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
<tr>
<td>Number of free-cycle OBs</td>
<td>OB 1</td>
</tr>
<tr>
<td>Number of time-of-day interrupt OBs</td>
<td>OB 10, 11, 12, 13, 14, 15, 16, 17</td>
</tr>
<tr>
<td>Number of time-delay interrupt OBs</td>
<td>OB 20, 21, 22, 23</td>
</tr>
<tr>
<td>Number of cyclic interrupts</td>
<td>OB 30, 31, 32, 33, 34, 35, 36, 37, 38</td>
</tr>
<tr>
<td>Number of process interrupt OBs</td>
<td>OB 40, 41, 42, 43, 44, 45, 46, 47</td>
</tr>
<tr>
<td>Number of DPV1 interrupt OBs</td>
<td>OB 55, 56, 57</td>
</tr>
<tr>
<td>Number of asynchronous error OBs</td>
<td>OB 80, 81, 82, 83, 84, 85, 86, 87, 88</td>
</tr>
<tr>
<td>Number of background OBs</td>
<td>OB 90</td>
</tr>
<tr>
<td>Number of restart OBs</td>
<td>OB 100, 102</td>
</tr>
<tr>
<td>Number of synchronous error OBs</td>
<td>OB 121, 122</td>
</tr>
</tbody>
</table>

### Nesting depth

- Per priority class: 24
- Additional ones in an error OB: 2

<table>
<thead>
<tr>
<th>SDBs</th>
<th>Maximum 512</th>
</tr>
</thead>
<tbody>
<tr>
<td>FBs</td>
<td>Maximum 8000</td>
</tr>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
<tr>
<td>FCs</td>
<td>Maximum 8000</td>
</tr>
<tr>
<td>• Size</td>
<td>Maximum 64 KB</td>
</tr>
</tbody>
</table>

### Address ranges (I/O)

- Total I/O address range: 16 KB/16 KB
- of those distributed: Including diagnostic addresses, addresses for I/O interfaces, etc.
- MPI/DP interface: 2 KB/2 KB
- DP interface: 8 KB/8 KB
- Process image: 16 KB/16 KB (configurable)
## Technical data

*20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)*

### Default
- 1024 bytes/1024 bytes

### Number of process image partitions
- Maximum 15

<table>
<thead>
<tr>
<th>Consistent data via PROFIBUS</th>
<th>Via integrated PROFINET interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. 244 bytes</td>
<td>Max. 1024 bytes</td>
</tr>
</tbody>
</table>

### Access to consistent data in the process image
- Yes

### Digital channels
- Maximum 131072/
- Maximum 131072
- of those central
  - Maximum 131072/
  - Maximum 131072

### Analog channels
- Maximum 8192/
- Maximum 8192
- of those central
  - Maximum 8192/
  - Maximum 8192

### Configuration

#### Central controllers/expansion units
- Maximum 2/20

#### Multicomputing
- No

#### Number of plug-in IMs (total)
- Maximum 6

- IM 460
  - Maximum 6

- IM 463–2
  - Maximum 4, in stand-alone mode only

#### Number of DP masters
- 2
- integrated
- Via CP 443–5 Ext.
  - Maximum 10

#### Number of plug-in S5 modules via adapter casing (in the central controller)
- None

#### Operable function modules and communication processors
  - FM, CP (point-to-point)
    - Limited by the number of slots and connections
  - see Appendix Function modules and communication processors supported by the S7-400H [Page 429]

  - CP 441
    - Limited by the number of connections

  - PROFIBUS and Ethernet CPs, including CP 443–5 Extended
    - Maximum 14, of which max. 10 CPs as DP masters

#### Connectable OPs
- 63

### Time

#### Clock
- Yes
  - Buffered
    - Yes
  - Resolution
    - 1 ms

#### Maximum deviation per day
- Power off (backed up)
  - 1.7 s
- Power on (not backed up)
  - 8.6 s

#### Operating hours counter
- 16
### 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number/number range</td>
<td>0 to 15</td>
</tr>
<tr>
<td>Range of values</td>
<td>0 to 32767 hours</td>
</tr>
<tr>
<td>Granularity</td>
<td>1 hour</td>
</tr>
<tr>
<td>Retentive</td>
<td>Yes</td>
</tr>
<tr>
<td>Time synchronization</td>
<td>Yes</td>
</tr>
<tr>
<td>In AS, on MPI and DP</td>
<td>As master or slave</td>
</tr>
<tr>
<td>Time difference in the system with synchronization via MPI</td>
<td>Max. 200 ms</td>
</tr>
<tr>
<td>Time difference in the system with synchronization via Ethernet</td>
<td>Max. 10 ms</td>
</tr>
</tbody>
</table>

#### S7 alarm functions

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of stations that can be logged on</td>
<td></td>
</tr>
<tr>
<td>For block-related alarms with SFC (Alarm_S/SQ and/or Alarm_D/DQ)</td>
<td>119</td>
</tr>
<tr>
<td>For block-related alarms with SFB (Notify, Notify_8, Alarm, Alarm_8, Alarm 8P)</td>
<td>16</td>
</tr>
<tr>
<td>Block-related alarms with SFC</td>
<td>Yes</td>
</tr>
<tr>
<td>Simultaneously active Alarm_S/SQ blocks or Alarm_D/DQ blocks</td>
<td>Maximum 1000</td>
</tr>
<tr>
<td>Block-related alarms with SFB</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of communication jobs for ALARM_8 blocks and blocks for S7 communication (selectable)</td>
<td>Maximum 10000</td>
</tr>
<tr>
<td>Default</td>
<td>1200</td>
</tr>
<tr>
<td>Process control alarms</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of archives that can be logged on</td>
<td>64</td>
</tr>
</tbody>
</table>

#### Test and commissioning functions

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status/modify tag</td>
<td>Yes, maximum 16 tag tables</td>
</tr>
<tr>
<td>Tag</td>
<td>Inputs/outputs, bit memories, DB, distributed inputs/outputs, timers, counters</td>
</tr>
<tr>
<td>Number of tags</td>
<td>Maximum 70</td>
</tr>
<tr>
<td>Forcing</td>
<td>Yes</td>
</tr>
<tr>
<td>Tag</td>
<td>Inputs/outputs, bit memories, distributed I/O</td>
</tr>
<tr>
<td>Number of tags</td>
<td>Maximum 512</td>
</tr>
<tr>
<td>Status LED</td>
<td>Yes, FRCE-LED</td>
</tr>
<tr>
<td>Block status</td>
<td>Yes, maximum 16 blocks at the same time</td>
</tr>
<tr>
<td>Single-step</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of breakpoints</td>
<td>Maximum 16</td>
</tr>
<tr>
<td>Diagnostic buffer</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of entries</td>
<td>Maximum 3200 (configurable)</td>
</tr>
</tbody>
</table>
### Technical data

#### 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Default</strong></td>
<td>120</td>
</tr>
<tr>
<td><strong>Communication</strong></td>
<td></td>
</tr>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of connection resources for S7 connections across all interfaces and CPs</td>
<td>120, incl. one each reserved for programming device and OP 62 reserved for fault-tolerant connections</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>• User data per job</td>
<td>Maximum 64 KB</td>
</tr>
<tr>
<td>• of which consistent</td>
<td>1 tag (462 bytes)</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>S5-compatible communication</td>
<td>Using FC AG_SEND and AG_RECV, max. via 10 CPs 443–1 or 443–5</td>
</tr>
<tr>
<td>• User data per job</td>
<td>Maximum 8 KB</td>
</tr>
<tr>
<td>• of which consistent</td>
<td>240 bytes</td>
</tr>
<tr>
<td>Number of simultaneous AG_SEND/AG_RECV jobs</td>
<td>Maximum 64/64, see CP manual</td>
</tr>
<tr>
<td>Standard communication (FMS)</td>
<td>Yes, via CP and loadable FB</td>
</tr>
<tr>
<td>Number of connection resources for S7 connections across all interfaces and CPs</td>
<td>120, incl. one each reserved for programming device and OP 62 of which fault-tolerant connections</td>
</tr>
<tr>
<td><strong>Open IE communication over TCP/IP</strong></td>
<td></td>
</tr>
<tr>
<td>Number of connections / access points, total</td>
<td>Maximum 118</td>
</tr>
<tr>
<td>Possible port numbers</td>
<td>1 to 49151</td>
</tr>
<tr>
<td>Where parameters are assigned without specification of a port number, the system assigns a port from the dynamic port number range between 49152 and 65534</td>
<td></td>
</tr>
<tr>
<td>Reserved port numbers</td>
<td>0 reserved TCP 20, 21 FTP TCP 25 SMTP TCP 102 RFC1006 UDP 135 RPC-DCOM UDP 161 SNMP_REQUEST UDP 34962 PN IO UDP 34963 PN IO UDP 34964 PN IO UDP 65532 NTP UDP 65533 NTP UDP 65534 NTP UDP 65535 NTP</td>
</tr>
<tr>
<td>TCP/IP</td>
<td>Yes, via integrated PROFINET interface and loadable FB</td>
</tr>
<tr>
<td>• Maximum number of connections</td>
<td>118</td>
</tr>
<tr>
<td>• Data length, max.</td>
<td>32 KB</td>
</tr>
<tr>
<td>ISO-on-TCP</td>
<td>Yes (via integrated PROFINET interface or CP 443-1/ EX20/GX 20 and loadable FBs)</td>
</tr>
</tbody>
</table>
### Technical data

#### 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum number of connections</td>
<td>118</td>
</tr>
<tr>
<td>Maximum data length via integrated PROFINET interface</td>
<td>32 KB</td>
</tr>
<tr>
<td>Maximum data length via CP 443-1</td>
<td>1452 bytes</td>
</tr>
<tr>
<td>UDP</td>
<td>Yes, via integrated PROFINET interface and loadable blocks</td>
</tr>
<tr>
<td>Maximum number of connections</td>
<td>118</td>
</tr>
<tr>
<td>Data length, max.</td>
<td>1472 bytes</td>
</tr>
</tbody>
</table>

### Interfaces

You may **not** configure the CPU as DP slave

#### 1st interface

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>X1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of interface</td>
<td>integrated</td>
</tr>
<tr>
<td>Physics</td>
<td>RS 485/Profibus</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply to interface (15 V DC to 30 V DC)</td>
<td>Max. 150 mA</td>
</tr>
<tr>
<td>Number of connection resources</td>
<td>MPI: 44, DP: 32</td>
</tr>
</tbody>
</table>

*If a diagnostic repeater is used on the segment, the number of connection resources on the segment is reduced by 1.*

### Functionality

- **MPI** Yes
- **PROFIBUS DP** DP master

#### 1st interface in MPI mode

<table>
<thead>
<tr>
<th>Utilities</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Maximum 12 Mbps</td>
</tr>
</tbody>
</table>

#### 1st interface in DP master mode

<table>
<thead>
<tr>
<th>Utilities</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Constant bus cycle time</td>
<td>No</td>
</tr>
</tbody>
</table>
### Technical data

#### 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC/FREEZE</td>
<td>No</td>
</tr>
<tr>
<td>Enable/disable DP slaves</td>
<td>No</td>
</tr>
<tr>
<td>Direct data exchange (cross-traffic)</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Maximum 12 Mbps</td>
</tr>
<tr>
<td>Number of DP slaves</td>
<td>Maximum 32</td>
</tr>
<tr>
<td>Number of slots per interface</td>
<td>Maximum 544</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 2 KB inputs / 2 KB outputs</td>
</tr>
<tr>
<td>User data per DP slave</td>
<td>Maximum 244 bytes</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 bytes inputs</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 bytes outputs</td>
</tr>
<tr>
<td></td>
<td>Maximum 244 slots</td>
</tr>
<tr>
<td></td>
<td>Maximum 128 bytes per slot</td>
</tr>
</tbody>
</table>

**Note:**

- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 2 KB inputs / 2 KB outputs) must not be exceeded in total across all 32 slaves.

#### 2nd interface

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface designation</td>
<td>X2</td>
</tr>
<tr>
<td>Type of interface</td>
<td>integrated</td>
</tr>
<tr>
<td>Physics</td>
<td>RS 485/Profibus</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply to interface (15 V DC to 30 V DC)</td>
<td>Max. 150 mA</td>
</tr>
<tr>
<td>Number of connection resources</td>
<td>32, a diagnostic repeater in the segment reduces the number of connection resources by 1</td>
</tr>
</tbody>
</table>

**Functionality**

- PROFIBUS DP

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd interface in DP master mode</td>
<td>DP master</td>
</tr>
<tr>
<td>PG/OP communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Routing</td>
<td>Yes</td>
</tr>
<tr>
<td>S7 communication</td>
<td>Yes</td>
</tr>
<tr>
<td>Global data communication</td>
<td>No</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>No</td>
</tr>
<tr>
<td>Constant bus cycle time</td>
<td>No</td>
</tr>
<tr>
<td>SYNC/FREEZE</td>
<td>No</td>
</tr>
<tr>
<td>Enable/disable DP slaves</td>
<td>No</td>
</tr>
<tr>
<td>Direct data exchange (cross-traffic)</td>
<td>No</td>
</tr>
<tr>
<td>Transmission rates</td>
<td>Maximum 12 Mbps</td>
</tr>
<tr>
<td>Number of DP slaves</td>
<td>Maximum 125</td>
</tr>
</tbody>
</table>
20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

| Number of slots per interface | Maximum 2173 |
| Address range                 | Maximum 8 KB inputs / 8 KB outputs |
| User data per DP slave        | Maximum 244 bytes |
|                               | Maximum 244 bytes inputs, |
|                               | Maximum 244 bytes outputs, |
|                               | Maximum 244 slots |
|                               | Maximum 128 bytes per slot |

**Note:**
- The total of input bytes across all slots may not exceed 244.
- The total of output bytes across all slots may not exceed 244.
- The address range of the interface (maximum 8 KB inputs / 8 KB outputs) must not be exceeded in total across all 125 slaves.

### 3rd interface

<table>
<thead>
<tr>
<th>Interface designation</th>
<th>X5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of interface</td>
<td>PROFINET</td>
</tr>
<tr>
<td>Physics</td>
<td>Ethernet RJ45</td>
</tr>
<tr>
<td></td>
<td>2 ports (switch)</td>
</tr>
<tr>
<td>Electrically isolated</td>
<td>Yes</td>
</tr>
<tr>
<td>Autosensing (10/100 Mbps)</td>
<td>Yes</td>
</tr>
<tr>
<td>Autonegotiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Auto-crossover</td>
<td>Yes</td>
</tr>
<tr>
<td>Media redundancy</td>
<td>Yes</td>
</tr>
<tr>
<td>System redundancy</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Changeover time on line interruption, typical 200 ms (PROFINET MRP)</td>
</tr>
<tr>
<td></td>
<td>Number of nodes on the ring, max. 50</td>
</tr>
<tr>
<td>Change of the IP address at runtime, supported</td>
<td>No</td>
</tr>
<tr>
<td>Keep Alive function, supported</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Functionality**
- PROFINET Yes

**Utilities**
- PG communication Yes
- OP communication Yes
- S7 communication
  - Maximum number of configurable connections 120, one of each reserved for programming device and OP
  - Maximum number of instances 10000
- S7 routing Yes
- PROFINET IO controller Yes
- PROFINET I-Device No
- PROFINET CBA No
- Open IE communication
- over TCP/IP Yes
## Technical data

### 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>ISO-on-TCP</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>UDP</td>
<td>Yes</td>
</tr>
<tr>
<td>Time synchronization</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### PROFINET IO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>PNO ID (hexadecimal)</td>
<td>Vendor ID: 0x002A, Device ID: 0x0102</td>
</tr>
<tr>
<td>Number of integrated PROFINET IO controllers</td>
<td>1</td>
</tr>
<tr>
<td>Number of PROFINET IO devices that can be connected</td>
<td>256</td>
</tr>
<tr>
<td>Number of connectable IO devices for RT of which are in line</td>
<td>256, 256</td>
</tr>
<tr>
<td>Shared Device, supported</td>
<td>No</td>
</tr>
<tr>
<td>Address range</td>
<td>Maximum 8 KB inputs/outputs</td>
</tr>
<tr>
<td>Number of submodules</td>
<td>Maximum 8192, Mixed modules count twice</td>
</tr>
<tr>
<td>Maximum user data length, including user data qualifiers</td>
<td>1440 bytes</td>
</tr>
<tr>
<td>Maximum user data consistency, including user data qualifiers</td>
<td>1024 bytes</td>
</tr>
<tr>
<td>Send clock cycles</td>
<td>250 μs, 500 μs, 1 ms, 2 ms, 4 ms</td>
</tr>
<tr>
<td>Update Time</td>
<td>250 μs, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, and 512 ms</td>
</tr>
<tr>
<td></td>
<td>The minimum value depends on the communication slice set for PROFINET IO, the number of IO devices, and the amount of configured user data.</td>
</tr>
</tbody>
</table>

### S7 protocol functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG functions</td>
<td>Yes</td>
</tr>
<tr>
<td>OP functions</td>
<td>Yes</td>
</tr>
<tr>
<td>IRT (Isochronous Real Time)</td>
<td>No</td>
</tr>
<tr>
<td>Prioritized startup</td>
<td>No</td>
</tr>
<tr>
<td>Accelerated (ASU) and Fast Startup Mode (FSU)</td>
<td>No</td>
</tr>
<tr>
<td>Tool change</td>
<td>No</td>
</tr>
<tr>
<td>Changing an IO device without Micro Memory Card or PG</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### 4th and 5th interface

<table>
<thead>
<tr>
<th>Interface Parameters</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Designation of the interfaces</td>
<td>IF1, IF2</td>
</tr>
<tr>
<td>Type of interface</td>
<td>Plug-in synchronization module (FOC)</td>
</tr>
<tr>
<td>Usable interface module</td>
<td>Synchronization module IF 960 (only in redundant mode; in stand-alone mode the interface remains free/covered)</td>
</tr>
<tr>
<td>Length of the synchronization cable</td>
<td>Maximum 10 km</td>
</tr>
</tbody>
</table>

### Programming

<table>
<thead>
<tr>
<th>Development Environment</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming language</td>
<td>LAD, FBD, STL, SCL, CFC, Graph, HiGraph®</td>
</tr>
<tr>
<td>Instruction set</td>
<td>See instruction list</td>
</tr>
</tbody>
</table>
### 20.4 Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Technical data</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Nesting levels</strong></td>
<td>7</td>
</tr>
<tr>
<td><strong>System functions (SFC)</strong></td>
<td>See instruction list</td>
</tr>
<tr>
<td><strong>Number of simultaneously active SFCs per segment</strong></td>
<td></td>
</tr>
<tr>
<td>• SFC 59 &quot;RD_REC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 58 &quot;WR_REC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 55 &quot;WR_PARM&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 57 &quot;PARAM_MOD&quot;</td>
<td>1</td>
</tr>
<tr>
<td>• SFC 56 &quot;WR_DPARM&quot;</td>
<td>2</td>
</tr>
<tr>
<td>• SFC 13 &quot;DPNRM_DG&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 51 &quot;RDSYSST&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFC 103 &quot;DP_TOPOL&quot;</td>
<td>1</td>
</tr>
<tr>
<td>The total number of active SFCs on all external segments may be four times more</td>
<td>than on one single segment.</td>
</tr>
<tr>
<td><strong>System function blocks (SFB)</strong></td>
<td>See instruction list</td>
</tr>
<tr>
<td><strong>Number of simultaneously active SFBs per segment</strong></td>
<td></td>
</tr>
<tr>
<td>• SFB 52 &quot;RDREC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>• SFB 53 &quot;WRREC&quot;</td>
<td>8</td>
</tr>
<tr>
<td>The total number of active SFBs on all external segments may be four times more</td>
<td>than on one single segment.</td>
</tr>
<tr>
<td><strong>User program protection</strong></td>
<td>Password protection</td>
</tr>
<tr>
<td><strong>Access-protected blocks</strong></td>
<td>Yes, with S7 Block Privacy</td>
</tr>
<tr>
<td><strong>Access to consistent data in the process image</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>CIR synchronization time (in stand-alone mode)</strong></td>
<td>60 ms</td>
</tr>
<tr>
<td><strong>Dimensions</strong></td>
<td></td>
</tr>
<tr>
<td>Mounting dimensions W x H x D (mm)</td>
<td>50 x 290 x 219</td>
</tr>
<tr>
<td><strong>Slots required</strong></td>
<td>2</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>Approx. 995 g</td>
</tr>
<tr>
<td><strong>Voltages and currents</strong></td>
<td></td>
</tr>
<tr>
<td>Current consumption from S7–400 bus (5 V DC)</td>
<td>Typ. 1.6 A&lt;br&gt;Max. 1.9 A</td>
</tr>
<tr>
<td>Current consumption from S7–400 bus (24 V DC)</td>
<td>The CPU does not consume any current at 24 V, it only makes this</td>
</tr>
<tr>
<td>Current output to DP interface (5 V DC)</td>
<td>Max. 90 mA</td>
</tr>
<tr>
<td><strong>Backup current</strong></td>
<td>Typically 180 µA (up to 40 °C)&lt;br&gt;Maximum 1000 µA</td>
</tr>
<tr>
<td>Maximum backup time</td>
<td>See the Module Specifications reference manual, chapter 3.3.</td>
</tr>
</tbody>
</table>
### Technical specifications of the CPU 417–5H PN/DP; (6ES7 417–5HK06–0AB0)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feed of external backup voltage to the CPU</td>
<td>5 V DC to 15 V DC</td>
</tr>
<tr>
<td>Power loss</td>
<td>Typ. 7.5 W</td>
</tr>
</tbody>
</table>
## 20.5 Technical data of memory cards

### Data

<table>
<thead>
<tr>
<th>Name</th>
<th>Order number</th>
<th>Current consumption at 5 V</th>
<th>Backup currents</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC 952 / 256 KB / RAM</td>
<td>6ES7952-1AH00-0AA0</td>
<td>typ. 35 mA max. 80 mA</td>
<td>typ. 1 µA max. 40 µA</td>
</tr>
<tr>
<td>MC 952 / 1 MB / RAM</td>
<td>6ES7952-1AK00-0AA0</td>
<td>typ. 40 mA max. 90 mA</td>
<td>typ. 3 µA max. 50 µA</td>
</tr>
<tr>
<td>MC 952 / 2 MB / RAM</td>
<td>6ES7952-1AL00-0AA0</td>
<td>typ. 45 mA max. 100 mA</td>
<td>typ. 5 µA max. 60 µA</td>
</tr>
<tr>
<td>MC 952 / 4 MB / RAM</td>
<td>6ES7952-1AM00-0AA0</td>
<td>typ. 45 mA max. 100 mA</td>
<td>typ. 5 µA max. 60 µA</td>
</tr>
<tr>
<td>MC 952 / 8 MB / RAM</td>
<td>6ES7952-1AP00-0AA0</td>
<td>typ. 45 mA max. 100 mA</td>
<td>typ. 5 µA max. 60 µA</td>
</tr>
<tr>
<td>MC 952 / 16 MB / RAM</td>
<td>6ES7952-1AS00-0AA0</td>
<td>typ. 100 mA max. 150 mA</td>
<td>typ. 50 µA max. 125 µA</td>
</tr>
<tr>
<td>MC 952 / 64 MB / RAM</td>
<td>6ES7952-1AY00-0AA0</td>
<td>typ. 100 mA max. 150 mA</td>
<td>typ. 100 µA max. 500 µA</td>
</tr>
<tr>
<td>MC 952 / 1 MB / 5 V FLASH</td>
<td>6ES7952-1KK00-0AA0</td>
<td>typ. 40 mA max. 90 mA</td>
<td>–</td>
</tr>
<tr>
<td>MC 952 / 2 MB / 5 V FLASH</td>
<td>6ES7952-1KL00-0AA0</td>
<td>typ. 50 mA max. 100 mA</td>
<td>–</td>
</tr>
<tr>
<td>MC 952 / 4 MB / 5 V FLASH</td>
<td>6ES7952-1KM00-0AA0</td>
<td>typ. 40 mA max. 90 mA</td>
<td>–</td>
</tr>
<tr>
<td>MC 952 / 8 MB / 5 V FLASH</td>
<td>6ES7952-1KP00-0AA0</td>
<td>typ. 50 mA max. 100 mA</td>
<td>–</td>
</tr>
<tr>
<td>MC 952 / 16 MB / 5 V FLASH</td>
<td>6ES7952-1KS00-0AA0</td>
<td>typ. 55 mA max. 110 mA</td>
<td>–</td>
</tr>
<tr>
<td>MC 952 / 32 MB / 5 V FLASH</td>
<td>6ES7952-1KT00-0AA0</td>
<td>typ. 55 mA max. 110 mA</td>
<td>–</td>
</tr>
<tr>
<td>MC 952 / 64 MB / 5 V FLASH</td>
<td>6ES7952-1KY00-0AA0</td>
<td>typ. 55 mA max. 110 mA</td>
<td>–</td>
</tr>
</tbody>
</table>

Dimensions WxHxD (in mm) 7.5 x 57 x 87

Weight Max. 35 g

EMC protection Provided by construction
## 20.6 Runtimes of the FCs and FBs for redundant I/Os

Table 20- 1  Runtimes of the blocks for redundant I/Os

<table>
<thead>
<tr>
<th>Block</th>
<th>Runtime in stand-alone/single mode</th>
<th>Runtime in redundant mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC 450 RED_INIT</td>
<td>2 ms + 300 µs / configured module pairs</td>
<td>-</td>
</tr>
<tr>
<td>Specifications are based on the startup</td>
<td>The specification for a module pair is a mean value. The runtime may be &lt; 300 µs for a few modules. For a large number of redundant modules the value may be &gt; 300 µs.</td>
<td></td>
</tr>
<tr>
<td>FC 451 RED_DEPA</td>
<td>160 µs</td>
<td>360 µs</td>
</tr>
<tr>
<td>FB 450 RED_IN</td>
<td>750 µs + 60 µs / module pair of the current TPA</td>
<td>1000 µs + 70 µs / module pair of the current TPA</td>
</tr>
<tr>
<td>Called from the corresponding sequence level.</td>
<td>The specification for a module pair is a mean value. The runtime may be additionally increased if discrepancies occur resulting in passivation and logging to the diagnostic buffer. The runtime may also be increased by a depassivation carried out at the individual sequence levels of FB RED_IN. Depending on the number of modules in the sequence level, the depassivation may increase the runtime of the FB RED_IN by 0.4 ... 8 ms. An 8 ms increase can be expected in redundant operation of modules totaling more than 370 pairs of modules at a sequence level.</td>
<td></td>
</tr>
<tr>
<td>FB 451 RED_OUT</td>
<td>650 µs + 2 µs / module pair of the current TPA</td>
<td>860 µs + 2 µs / module pair of the current TPA</td>
</tr>
<tr>
<td>Called from the corresponding sequence level.</td>
<td>The specification for a module pair is a mean value. The runtime may be &lt; 2 µs for a few modules. For a large number of redundant modules the value may be &gt; 2 µs.</td>
<td></td>
</tr>
</tbody>
</table>

An 8 ms increase can be expected in redundant operation of modules totaling more than 370 pairs of modules at a sequence level.
### Technical data

#### 20.6 Runtimes of the FCs and FBs for redundant I/Os

<table>
<thead>
<tr>
<th>Block</th>
<th>Runtime in stand-alone/single mode</th>
<th>Runtime in redundant mode</th>
</tr>
</thead>
</table>
| FB 452 RED_DIAG | Called in OB 72: 160 µs  
                      Called in OB 82, 83, 85:  
                      250 µs + 5 µs / configured module pairs  
                      Under extreme conditions the runtime of FB RED_DIAG is increased up to 1.5 ms.  
                      This is the case when the working DB is 60 KB or larger and if there are interrupt trigger addresses that do not belong to the redundant I/O. | Called in OB 72: 360 µs  
                                                                                          Called in OB 82, 83, 85:  
                                                                                          430 µs (basic load) + 6 µs / configured module pairs  
                                                                                          Under extreme conditions the runtime of FB RED_DIAG is increased up to 1.5 ms.  
                                                                                          This is the case when the working DB is 60 KB or larger and if there are interrupt trigger addresses that do not belong to the redundant I/O. |
| FB 453 RED_STATUS | 160 µs 4 µs/ configured module pairs * number of module pairs  
                                                                 The runtime depends on the random position of the module being searched for in the working DB.  
                                                                 When a module address is not redundant, the entire working DB is searched. This results in the longest runtime of FB RED_STATUS.  
                                                                 The number of module pairs is based either on all inputs (DI/AI) or all outputs (DO/AO). | 350 µs + 5 µs / configured module pairs * number of module pairs  
                                                                 The runtime depends on the random position of the module being searched for in the working DB.  
                                                                 When a module address is not redundant, the entire working DB is searched. This results in the longest runtime of FB RED_STATUS.  
                                                                 The number of module pairs is based either on all inputs (DI/AI) or all outputs (DO/AO). |

**Note**

These are guide values, not absolute values. The actual value may deviate from these specifications in some cases. This overview is intended as a guide and should help you estimate how use of the RED_IO library may change the cycle time.
Characteristic values of redundant automation systems

This appendix provides a brief introduction to the characteristic values of redundant automation systems, and shows the practical effects of redundant configurations, based on a selection of configurations.

You will find an overview of the MTBF of various SIMATIC products in the SIMATIC FAQ at:
http://support.automation.siemens.com
under entry ID 16818490

A.1 Basic concepts

The quantitative assessment of redundant automation systems is usually based on their reliability and availability parameters. These are described in detail below.

Reliability

Reliability refers to the capability of technical equipment to fulfill its function during its operating period. This is usually no longer the case if any of its components fails.

So a commonly used measure for reliability is the MTBF (Mean Time Between Failure). This can be analyzed statistically based on the parameters of running systems, or by calculating the failure rates of the components used.

Reliability of modules

The reliability of SIMATIC components is extremely high as a consequence of extensive quality assurance measures in design and production.

Reliability of automation systems

The use of redundant modules considerably prolongs the MTBF of a system. The combination of integrated high-quality self-tests and error detection mechanisms of the S7-400H CPUs allows the detection and localization of virtually all errors.

The MTBF of an S7-400H is determined by the MDT (Mean Down Time) of a system unit. This time is derived in essence from the error detection time plus the time required to repair or replace defective modules.

In addition to other measures, a CPU provides a self-test function with an adjustable test cycle time. The default test cycle time is 90 minutes. This time has an influence on the error detection time. The repair time usually required for a modular system such as the S7-400H is 4 hours.
Mean Down Time (MDT)

The MDT of a system is determined by the times outlined below:

- Time required to detect an error
- Time required to find the cause of an error
- Time required for troubleshooting and to restart the system

The system MDT is calculated based on the MDT of the individual system components. The structure in which the components make up the system also forms part of the calculation.

Correlation between MDT and MTBF: MDT << MTBF

The MDT value is of the highest significance for the quality of system maintenance. The most important factors are:

- Qualified personnel
- Efficient logistics
- High-performance tools for diagnostics and error recognition
- A sound repair strategy

The figure below shows the dependency of the MDT on the times and factors mentioned above.

Figure A-1 MDT
The figure below shows the parameters included in the calculation of the MTBF of a system.

![Diagram of MTBF calculation parameters]

**Requirements**

This analysis assumes the following conditions:

- The failure rate of all components and all calculations is based on an average temperature of 40 °C.
- The system installation and configuration is free of errors.
- All replacement parts are available locally, in order to prevent extended repair times due to missing spare parts. This keeps the component MDT down to a minimum.
- The MDT of individual components is 4 h. The system's MDT is calculated based on the MDT of the individual components plus the system structure.
- The MTBF of the components meets the following standards:
  - SN 29500
    - This standard is compliant with MIL–HDBK 217–F.
  - IEC 60050
  - IEC 61709
- The calculations are made using the diagnostic coverage of each component.
- A CCF factor between 0.2% and 2% is assumed, depending on the system configuration.
**Common Cause Failure (CCF)**

The Common Cause Failure (CCF) is an error which is caused by one or more events which also lead to an error state on two or more separate channels or components in a system. A CCF leads to a system failure.

The CCF may be caused by one of the following factors:

- Temperature
- Humidity
- Corrosion
- Vibration and shock
- Electromagnetic interference
- Electrostatic discharge
- RF interference
- Unexpected sequence of events
- Operating errors

The CCF factor defines the ratio between the probability of the occurrence of a CCF and the probability of the occurrence of any other error.

Typical CCF factors range from 2% to 0.2% in a system with identical components, and between 1% and 0.1% in a system containing different components.

Within the range stipulated in IEC 61508, a CCF factor between 0.02% and 5% is used to calculate the MTBF.

**Reliability of an S7-400H**

The use of redundant modules prolongs the system MTBF by a large factor. The integrated high-grade self-test and the test/message functions of the S7-400H CPUs enable the detection and localization of virtually all errors. The calculated diagnostic coverage is around 90%.

The reliability in stand-alone mode is described by the corresponding failure rate. The failure rate for all S7 components is calculated according to the SN29500 standard.

The reliability in redundant mode is described by the failure rate of the components involved. This is termed “MTBF” below. Those combinations of failed components which cause a system failure are described and calculated using Markov models. Calculations of the system MTBF take account of the diagnostic coverage and the common cause factor.
Availability

Availability is the probability that a system is operable at a given point of time. This can be enhanced by means of redundancy, for example by using redundant I/O modules or multiple encoders at the same sampling point. Redundant components are arranged such that system operability is not affected by the failure of a single component. Here, again, an important element of availability is a detailed diagnostics display.

The availability of a system is expressed as a percentage. It is defined by the mean time between failure (MTBF) and the mean time to repair MTTR (MDT). The availability of a two-channel (1-out-of-2) fault-tolerant system can be calculated using the following formula:

\[ V = \frac{MTBF_{1v2}}{MTBF_{1v2} + MDT} \times 100\% \]

Figure A-4  Availability

A.2 Comparison of MTBF for selected configurations

The following sections compare systems with a centralized and distributed I/Os.

The following framework conditions are set for the calculation.

- MDT (Mean Down Time) 4 hours
- Ambient temperature 40 degrees
- Buffer voltage is safeguarded

A.2.1 System configurations with redundant CPU 417-5H

The following system with one CPU (e.g. 417-5H) operating in stand-alone mode forms the basis for calculation of a reference factor, which defines the multiple of the system MTBF of other systems with centralized I/Os compared to the base line.
### Fault-tolerant CPU in stand-alone mode

<table>
<thead>
<tr>
<th>Fault-tolerant CPU in stand-alone mode (e.g. CPU 417–5H)</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS 407, 10 A</td>
<td>1</td>
</tr>
<tr>
<td>CPU 417–5H</td>
<td>1</td>
</tr>
</tbody>
</table>

**Fault-tolerant CPU in stand-alone mode (e.g. CPU 417–5H)**

#### Redundant CPUs in different racks

**Redundant CPU 417–5H in divided rack, CCF = 2%**

<table>
<thead>
<tr>
<th>Redundant CPU 417–5H in divided rack, CCF = 2%</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS 407, 10 A</td>
<td>approximately 20</td>
</tr>
<tr>
<td>CPU 417–4H</td>
<td>2</td>
</tr>
<tr>
<td>2 x fiber-optic cables</td>
<td>1</td>
</tr>
<tr>
<td>Rack UR2-H</td>
<td>2</td>
</tr>
</tbody>
</table>

**Redundant CPU 417–5H in two separate racks, CCF = 1 %**

<table>
<thead>
<tr>
<th>Redundant CPU 417–5H in two separate racks, CCF = 1 %</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS 407, 10 A</td>
<td>approximately 38</td>
</tr>
<tr>
<td>CPU 417–4H</td>
<td>2</td>
</tr>
<tr>
<td>2 x fiber-optic cables</td>
<td>1</td>
</tr>
<tr>
<td>Rack UR1</td>
<td>2</td>
</tr>
</tbody>
</table>

**Redundant CPU 417–5H in two separate racks, CCF = 1 %**
A.2.2 System configurations with distributed I/Os

The system with two fault-tolerant CPUs 417-5H and one-sided I/Os described below is taken as a basis for calculating a reference factor which specifies the multiple of the availability of the other systems with distributed I/Os compared with the base line.

You can find the order numbers of the IMs in chapter Using single-channel, one-sided I/Os (Page 165).

Redundant CPUs with single-channel, one-sided or switched I/Os

<table>
<thead>
<tr>
<th>One-sided distributed I/Os</th>
<th>Base line</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Diagram of one-sided distributed I/Os" /></td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Switched distributed I/O, PROFIUSB DP, CCF = 2 %</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Diagram of switched distributed I/Os" /></td>
<td>approx. 15</td>
</tr>
</tbody>
</table>
Characteristic values of redundant automation systems

A.2 Comparison of MTBF for selected configurations

Switched distributed I/O, PROFINET, CCF = 2 %

<table>
<thead>
<tr>
<th>Switched distributed I/O, PROFINET, CCF = 2 %</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 x fiber-optic cables</td>
<td>approx. 10</td>
</tr>
</tbody>
</table>

The estimate applies if the process allows for any device to fail.

**Redundant CPUs with redundant I/Os**

The comparison only took account of the I/O modules.

<table>
<thead>
<tr>
<th>Single-channel, one-sided I/O</th>
<th>MTBF factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>ET 200M</td>
<td>1</td>
</tr>
</tbody>
</table>
Characteristic values of redundant automation systems

A.2 Comparison of MTBF for selected configurations

<table>
<thead>
<tr>
<th>Redundant I/O</th>
<th>MLFB</th>
<th>MTBF factor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CCF = 1%</td>
</tr>
<tr>
<td>Digital input modules, distributed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DI 24xDC24V</td>
<td>6ES7 326–1BK00–0AB0</td>
<td>approx. 5</td>
</tr>
<tr>
<td>DI 8xNAMUR [EEx ib]</td>
<td>6ES7 326–1RF00–0AB0</td>
<td>approx. 5</td>
</tr>
<tr>
<td>DI16xDC24V, Alarm</td>
<td>6ES7 321–7BH00–0AB0</td>
<td>approx. 4</td>
</tr>
<tr>
<td>Analog input modules, distributed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AI 6x13Bit</td>
<td>6ES7 336–1HE00–0AB0</td>
<td>approx. 5</td>
</tr>
<tr>
<td>AI8x12Bit</td>
<td>6ES7 331–7KF02–0AB0</td>
<td>approx. 5</td>
</tr>
<tr>
<td>Digital output modules, distributed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DO 10xDC24V/2A</td>
<td>6ES7 326–2BF00–0AB0</td>
<td>approx. 5</td>
</tr>
<tr>
<td>DO8xDC24V/2A</td>
<td>6ES7 322–1BF01–0AA0</td>
<td>approx. 3</td>
</tr>
<tr>
<td>DO32xDC24V/0.5A</td>
<td>6ES7 322–1BL00–0AA0</td>
<td>approx. 3</td>
</tr>
</tbody>
</table>

Summary

There are now several thousand applications of redundant automation systems in the field, in various configurations. To calculate the MTBF, we assumed an average configuration. Based on experience in the field, an assumption of MTBF of 3000 years is 95% reliable. The system MTBF value calculated is about 230 years for a system configuration with redundant CPU 417-5H.
A.2.3 Comparison of system configurations with standard and fault-tolerant communication

The next section shows a comparison between standard and fault-tolerant communication for a configuration consisting of a fault-tolerant system, a fault-tolerant CPU operating in stand-alone mode, and a single-channel OS.

The comparison only took account of the CP and cable communication components.

Systems with standard and fault-tolerant communication

<table>
<thead>
<tr>
<th>Standard communication</th>
<th>Base line</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS workstation</td>
<td>S7-400H system</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fault-tolerant communication</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS workstation</td>
<td>S7-400H system</td>
</tr>
</tbody>
</table>
Stand-alone operation

Overview

This appendix provides you with the information for stand-alone operation of a fault-tolerant CPU. You will learn:

- how stand-alone mode is defined
- when stand-alone mode is required
- what you have to take into account for stand-alone operation
- how the fault tolerance-specific LEDs react
- how to configure stand-alone operation of a fault-tolerant CPU
- how you can expand it to form a fault-tolerant system

The differences from a standard S7-400 CPU that you have to take into account when configuring and programming the fault-tolerant CPU are given in appendix Differences between fault-tolerant systems and standard systems (Page 425).

Definition

By stand-alone operation, we mean the use of a fault-tolerant CPU in a standard SIMATIC-400 station.

Reasons for stand-alone operation

The applications outlined below are only possible when using a fault-tolerant CPU, so they are not possible with standard S7-400 CPUs.

- Use of fault-tolerant connections
- Configuration of the S7-400F fail-safe automation system

A fail-safe user program can only be compiled for execution on a fault-tolerant CPU with a F-runtime license (for more details refer to the S7-400F and S7-400FH Automation Systems manuals).

Note

The self-test of the fault-tolerant CPU is also performed in stand-alone mode.
What you have to take into account for stand-alone operation of a fault-tolerant CPU

Note
When operating a fault-tolerant CPU in stand-alone mode, no synchronization modules may be connected. The rack number must be set to "0".

Although a fault-tolerant CPU has additional functions compared to a standard S7-400 CPU, it does not support specific functions. So particularly when programming your automation system, you need to know the CPU on which you are going to run the user program. A user program written for a standard S7-400 CPU usually will not run on a fault-tolerant CPU in stand-alone mode without adaptations.

The table below lists the differences between the operation of a fault-tolerant CPU in stand-alone mode and in redundant mode.

Table B-1 Differences between stand-alone mode and redundant mode

<table>
<thead>
<tr>
<th>Function</th>
<th>Fault-tolerant CPU in stand-alone mode</th>
<th>Fault-tolerant CPU in redundant system mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connection of S5 modules via IM or adapter casing</td>
<td>via IM 463-2</td>
<td>No</td>
</tr>
<tr>
<td>Redundancy error OBs (OB 70, OB 72)</td>
<td>Yes, but no calls</td>
<td>Yes</td>
</tr>
<tr>
<td>CPU hardware fault (OB 84)</td>
<td>after the detection and elimination of memory errors</td>
<td>after the detection and elimination of memory errors with reduced performance of the redundant link between the two CPUs</td>
</tr>
<tr>
<td>SSL ID W#16#0232 index W#16#0004 byte 0 of the &quot;index&quot; word in the data record</td>
<td>W#16#F8</td>
<td>Single mode: W#16#F8 or W#16#F9 Redundant: W#16#F8 and W#16#F1 or W#16#F9 and W#16#F0</td>
</tr>
<tr>
<td>Multi-DP master mode</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>System modifications during operation</td>
<td>Yes, as described in the &quot;System Modification during Operation Using CIR&quot; manual.</td>
<td>Yes, as described in Chapter Failure and replacement of components during operation [Page 253] for redundant operation.</td>
</tr>
<tr>
<td>Shared Device</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
Fault tolerance-specific LEDs

The REDF, IFM1F, IFM2F, MSTR, RACK0 and RACK1 LEDs show the reaction specified in the table below in stand-alone mode.

<table>
<thead>
<tr>
<th>LED</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>REDF</td>
<td>Dark</td>
</tr>
<tr>
<td>IFM1F</td>
<td>Dark</td>
</tr>
<tr>
<td>IFM2F</td>
<td>Dark</td>
</tr>
<tr>
<td>MSTR</td>
<td>Lit</td>
</tr>
<tr>
<td>RACK0</td>
<td>Lit</td>
</tr>
<tr>
<td>RACK1</td>
<td>Dark</td>
</tr>
</tbody>
</table>

Configuring stand-alone mode

Requirement: No synchronization module may be inserted in the fault-tolerant CPU.

Procedure:

1. Insert a SIMATIC-400 station in your project.
2. Configure the station with the fault-tolerant CPU according to your hardware configuration. For stand-alone operation, insert the fault-tolerant CPU in a standard rack (Insert > Station > S7–400 station in SIMATIC Manager).
3. Parameterize the fault-tolerant CPU. Use the default values, or customize the necessary parameters.
4. Configure the necessary networks and connections. For stand-alone operation you can configure “fault-tolerant S7 connections”.

For help on procedure refer to the Help topics in SIMATIC Manager.
Expansion to a fault-tolerant system

Note

You can only expand your system to a fault-tolerant system if you have not assigned any odd numbers to expansion units in stand-alone mode.

To expand the fault-tolerant CPU later to form a fault-tolerant system:

1. Open a new project and insert a fault-tolerant station.
2. Copy the entire rack from the standard SIMATIC-400 station and insert it twice into the fault-tolerant station.
3. Insert the subnets as required.
4. Copy the DP slaves from the old stand-alone project to the fault-tolerant station as required.
5. Reconfigure the communication connections.
6. Carry out all changes required, such as the insertion of one-sided I/Os.

For information on how to configure the project refer to the Online Help.

Changing the operating mode of a fault-tolerant CPU

The procedure for changing the operating mode of a fault-tolerant CPU differs depending on the operating mode you want to switch to and the rack number configured for the CPU:

Changing from redundant to stand-alone mode

1. Remove the synchronization modules
2. Remove the CPU.
3. Set rack number 0 on the CPU.
4. Install the CPU.
5. Download a project with the stand-alone configuration to the CPU.

Changing from stand-alone mode to redundant mode, rack number 0

1. Insert the synchronization modules into the CPU.
2. Run an unbuffered power cycle, for example, by removing and inserting the CPU, or download a project to the CPU in which it is configured for redundant mode.

Changing from stand-alone mode to redundant mode, rack number 1

1. Set rack number 1 on the CPU.
2. Install the CPU.
3. Insert the synchronization modules into the CPU.
System modification during operation in stand-alone mode

With a system modification during operation, it is also possible to make certain configuration changes in RUN on fault-tolerant CPUs. The procedure corresponds to that for standard CPUs. Processing is halted during this, but for no more than 2.5 seconds (parameterizable). During this time, the process outputs retain their current values. In process control systems in particular, this has virtually no effect on the process. See also the "Modifying the System during Operation via CIR" manual.

System modifications during operation are only supported with distributed I/O. They require a configuration as shown in the figure below. To give you a clear overview, this shows only one DP master system and one PA master system.

![Figure B-1 Overview: System structure for system modifications during operation](image)

Hardware requirements for system modifications during operation

To modify a system during operation, the following hardware requirements must be met at the commissioning stage:

- Use of an S7-400 CPU
- S7-400 H-CPU only in stand-alone mode
- If you use a CP 443-5 Extended, this must have a firmware V5.0 or higher.
- To add modules to an ET 200M: Use an IM 153-2, MLFB 6ES7 153-2BA00-0XB0 or higher, or an IM 153-2FO, MLFB 6ES7 153-2BB00-0XB0 or higher. The installed ET 200M also requires an active backplane bus with sufficient free space for the planned expansion. Include the ET 200M so that it complies with IEC 61158.
Stand-alone operation

- If you want to add entire stations: Make sure that you have the required connectors, repeaters, etc.
- If you want to add PA slaves (field devices): Use IM 157, MLFB 6ES7 157-0AA82-0XA00 or higher, in the corresponding DP/PA link.

**Note**
You can freely combine components which support system modifications during operation with those that do not. Depending on your selected configuration, there may be restrictions affecting the components on which you can make system modifications during operation.

Software requirements for system modifications during operation
To make modifications during operation, the user program must be written so that station failures or module faults, for example, do not lead to a CPU STOP.

Permitted system modifications: Overview
During operation, you can make the following system modifications:
- Add components or modules with modular DP slaves ET 200M, ET 200S and ET 200iS, provided they are compliant with IEC 61158
- Use of previously unused channels in a module or submodule of the modular slaves ET 200M, ET 200S, and ET 200iS
- Add DP slaves to an existing DP master system
- Add PA slaves (field devices) to an existing PA master system
- Add DP/PA couplers downstream of an IM 157
- Add PA Links (including PA master systems) to an existing DP master system
- Assign added modules to a process image partition
- Change parameter settings for I/O modules, for example selecting different interrupt limits
- Undo changes: Modules, submodules, DP slaves and PA slaves (field devices) you added earlier can be removed again.
Differences between fault-tolerant systems and standard systems

When configuring and programming a fault-tolerant automation system with fault-tolerant CPUs, you must make allowances for a number of differences from the standard S7-400 CPUs. A fault-tolerant CPU has additional functions compared to a standard S7-400 CPU, on the other hand it does not support specific functions. This has to be taken in account particularly if you wish to run a program that was created for a standard S7-400 CPU on a fault-tolerant CPU.

The ways in which the programming of fault-tolerant systems differs from that for standard systems are summarized below. You will find further differences in appendix Stand-alone operation (Page 419).

If you use any of the affected calls (OBs and SFCs) in your user program, you will need to adapt your program accordingly.

Additional functions of fault-tolerant systems

<table>
<thead>
<tr>
<th>Function</th>
<th>Additional programming</th>
</tr>
</thead>
<tbody>
<tr>
<td>Redundancy error OBs</td>
<td>• I/O redundancy error OB (OB 70)</td>
</tr>
<tr>
<td></td>
<td>• CPU redundancy error OB (OB 72)</td>
</tr>
<tr>
<td></td>
<td>For detailed information, refer to the System and Standard Functions Reference Manual.</td>
</tr>
<tr>
<td>CPU hardware fault</td>
<td>Depending on the configuration, OB 82 or OB 84 is also called if the performance of the redundant link between the two CPUs is reduced.</td>
</tr>
<tr>
<td>Additional information in OB start information and in diagnostic buffer entries</td>
<td>The rack number and the CPU (master/reserve) are specified. You can evaluate this additional information in the program.</td>
</tr>
<tr>
<td>SFC for fault-tolerant systems</td>
<td>You can control processes in fault-tolerant systems using SFC 90 &quot;H_CTRL&quot;.</td>
</tr>
<tr>
<td>Fault-tolerant communication connections</td>
<td>Fault-tolerant connections are configured and do not require further programming.</td>
</tr>
<tr>
<td></td>
<td>You can use the SFBs for configured connections when using fault-tolerant connections.</td>
</tr>
<tr>
<td>Self-test</td>
<td>The self-test is performed automatically, no further programming is required.</td>
</tr>
<tr>
<td>High-quality RAM test</td>
<td>The CPU performs a high-quality RAM test after an unbuffered POWER ON.</td>
</tr>
<tr>
<td>Switched I/O</td>
<td>No additional programming required, see section Using single-channel switched I/O (Page 167).</td>
</tr>
<tr>
<td>Reading type and serial number of a synchronization module</td>
<td>How to read the serial number of a memory card.</td>
</tr>
</tbody>
</table>
# Differences between fault-tolerant systems and standard systems

<table>
<thead>
<tr>
<th>Function</th>
<th>Additional programming</th>
</tr>
</thead>
</table>
| Information in the system status list         | - You can also obtain data records for the fault tolerance-specific LEDs from the partial list with SSL ID W#16#0019.  
- You can also obtain data records for the redundancy error OBs from the partial list with SSL ID W#16#0222.  
- You can obtain information on the current status of the fault-tolerant system from the partial list with SSL ID W#16#xy71.  
- You can also obtain data records for the fault tolerance-specific LEDs from the partial list with SSL ID W#16#0174.  
- The partial list with the SSL ID W#16#xy75 provides information on the status of the communication between the fault-tolerant system and switched DP slaves. |
| Update monitoring                             | The operating system monitors the following four configurable timers:  
- Maximum cycle time extension  
- Maximum communication delay  
- Maximum inhibit time for priority classes > 15  
- Minimum I/O retention time  
No additional programming is required for this. For more detailed information, refer to chapter [Link-up and update](Page 135). |
| SSL ID W#16#0232 index W#16#0004 byte 0 of the "index" word in the data record | Fault-tolerant CPU in stand-alone mode: W#16#F8  
Fault-tolerant CPU in single mode: W#16#F8 or W#16#F9  
Fault-tolerant CPU in redundant mode: W#16#F8 and W#16#F1 or W#16#F9 and W#16#F0 |

## Restrictions of the fault-tolerant CPU compared to a standard CPU

<table>
<thead>
<tr>
<th>Function</th>
<th>Restriction of the fault-tolerant CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hot restart</td>
<td>A hot restart is not possible. OB 101 is not possible</td>
</tr>
<tr>
<td>Multicomputing</td>
<td>Multicomputing is not possible. OB 60 and SFC 35 are not supported</td>
</tr>
<tr>
<td>Startup without configuration loaded</td>
<td>Startup without loaded configuration is not possible.</td>
</tr>
<tr>
<td>Background OB</td>
<td>OB 90 is not supported.</td>
</tr>
<tr>
<td>Multi-DP master mode</td>
<td>The fault-tolerant CPUs do not support multi-DP master mode in REDUNDANT mode.</td>
</tr>
<tr>
<td>Direct communication between DP slaves</td>
<td>Cannot be configured in STEP 7</td>
</tr>
<tr>
<td>Constant bus cycle time for DP slaves</td>
<td>No constant bus cycle time for DP slaves in the fault-tolerant system</td>
</tr>
<tr>
<td>Synchronization of DP slaves</td>
<td>Synchronization of DP slave groups is not supported. SFC 11 &quot;DPSYC_FR&quot; is not supported.</td>
</tr>
<tr>
<td>Disabling and enabling DP slaves</td>
<td>Disabling and enabling DP slaves is not possible. SFC 12 &quot;D_ACT_DP&quot; is not supported.</td>
</tr>
</tbody>
</table>
## Differences between fault-tolerant systems and standard systems

<table>
<thead>
<tr>
<th>Function</th>
<th>Restriction of the fault-tolerant CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Runtime response</td>
<td>The command execution time for a CPU 41x-5H is slightly higher compared to the corresponding standard CPU (see <em>S7-400 Instruction List</em> and <em>S7-400H Instruction List</em>). This must be taken into account for all time-critical applications. You may need to increase the scan cycle monitoring time.</td>
</tr>
<tr>
<td>DP cycle time</td>
<td>A CPU 41x-5H has a slightly longer DP cycle time compared to the corresponding standard CPU.</td>
</tr>
<tr>
<td>Delays and inhibits</td>
<td>During update:</td>
</tr>
<tr>
<td></td>
<td>• The asynchronous SFCs for data records are acknowledged negatively</td>
</tr>
<tr>
<td></td>
<td>• Messages are delayed</td>
</tr>
<tr>
<td></td>
<td>• All priority classes up to 15 are initially delayed</td>
</tr>
<tr>
<td></td>
<td>• Communication jobs are rejected or delayed</td>
</tr>
<tr>
<td></td>
<td>• Finally, all priority classes are disabled</td>
</tr>
<tr>
<td></td>
<td>For more detailed information, refer to chapter 7.</td>
</tr>
<tr>
<td>Use of symbol-oriented messages (SCAN)</td>
<td>The use of symbol-oriented messages is not possible.</td>
</tr>
<tr>
<td>Global data communication</td>
<td>GD communication is not possible (neither cyclically, nor by calling system functions SFC 60 &quot;GD_SND&quot; and SFC 61 &quot;GD_RCV&quot;)</td>
</tr>
<tr>
<td>S7 basic communication</td>
<td>Communication functions (SFCs) for basic communication are not supported.</td>
</tr>
<tr>
<td>S5 connection</td>
<td>The connection of S5 modules by means of an adapter casing is not possible. The connection of S5 modules via IM 463-2 is only supported in stand-alone mode.</td>
</tr>
<tr>
<td>CPU as DP slave</td>
<td>Not possible</td>
</tr>
<tr>
<td>CPU as I-Device</td>
<td>Not possible</td>
</tr>
<tr>
<td>Use of SFC 49 &quot;LGC_GADR&quot;</td>
<td>You are operating an S7-400H automation system in redundant mode. If you declare the logical address of module of the switched DP slave at the LADDR parameter and call SFC 49, the high byte of the RACK parameter returns the DP master system ID of the active channel. If there is no active channel, the function outputs the ID of the DP master system belonging to the master CPU.</td>
</tr>
<tr>
<td>Call of SFC 51 &quot;RDSYSST&quot; with SSL_ID=W#16#xy91</td>
<td>The data records of the SSL partial lists shown below cannot be read with SFC 51 &quot;RDSYSST&quot;:</td>
</tr>
<tr>
<td></td>
<td>• SSL_ID=W#16#0091</td>
</tr>
<tr>
<td></td>
<td>• SSL_ID=W#16#0191</td>
</tr>
<tr>
<td></td>
<td>• SSL_ID=W#16#0291</td>
</tr>
<tr>
<td></td>
<td>• SSL_ID=W#16#0391</td>
</tr>
<tr>
<td></td>
<td>• SSL_ID=W#16#0991</td>
</tr>
<tr>
<td></td>
<td>• SSL_ID=W#16#0E91</td>
</tr>
<tr>
<td>Web server</td>
<td>Not integrated</td>
</tr>
<tr>
<td>PROFINET CBA</td>
<td>Not possible</td>
</tr>
<tr>
<td>IRT</td>
<td>Not possible</td>
</tr>
<tr>
<td>Isochronous mode on PN</td>
<td>Not possible</td>
</tr>
<tr>
<td>Tool changer</td>
<td>Not possible</td>
</tr>
</tbody>
</table>
Differences between fault-tolerant systems and standard systems

<table>
<thead>
<tr>
<th>Function</th>
<th>Restriction of the fault-tolerant CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast Startup</td>
<td>Not possible</td>
</tr>
<tr>
<td>Use of an external PN controller</td>
<td>Not possible</td>
</tr>
</tbody>
</table>

See also

System and operating states of the S7–400H (Page 115)
Function modules and communication processors supported by the S7-400H

You can use the following function modules (FMs) and communication processors (CPs) on an S7-400H automation system.

**Note**
There may be further restrictions for individual modules. Refer to the information in the corresponding product information and FAQ, or in SIMATIC NET News.

### FMs and CPs which can be used centrally

<table>
<thead>
<tr>
<th>Module</th>
<th>Order No.</th>
<th>Release</th>
<th>One-sided</th>
<th>Redundant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter module FM 450</td>
<td>6ES7 450–1AP00–0AE0</td>
<td>As of product version 2</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Function module FM 458-1 DP</td>
<td>6DD 1607-0AA1</td>
<td>As of firmware 1.1.0</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>6DD 1607-0AA2</td>
<td>As of firmware 2.0.0</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Communication processor CP 441-1 (point-to-point link)</td>
<td>6ES7 441–1AA02–0AE0</td>
<td>As of product version 2</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>6ES7 441–1AA03–0AE0</td>
<td>As of product version 1</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td></td>
<td>6ES7 441–1AA04–0AE0</td>
<td>As of product version 1</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Communication processor CP 441-2 (point-to-point link)</td>
<td>6ES7 441–2AA02–0AE0</td>
<td>As of product version 2</td>
<td>Yes</td>
<td>No</td>
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<td></td>
<td>6ES7 441–2AA03–0AE0</td>
<td>As of product version 1</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td></td>
<td>6ES7 441–2AA04–0AE0</td>
<td>As of product version 1</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Communication processor CP 443-1 Multi (Industrial Ethernet, TCP / ISO transport)</td>
<td>6GK7 443–1EX10–0XE0</td>
<td>As of product version 1</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td></td>
<td>6GK7 443–1EX11–0XE0</td>
<td>As of firmware V2.7.3</td>
<td>Yes</td>
<td>Yes</td>
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</tbody>
</table>
| Communication processor CP 443-1 Multi (Industri
| 6GK7 443–1EX20–0XE0 | As of product version 1 | Yes | Yes |
| | 6GK7 443–1GX20–0XE0 | As of firmware V2.0 | Yes | Yes |
| S7 connections via gigabit port are not permitted | 6GK7 443–1GX30–0XE0 | As of product version 1 | Yes | Yes |
| Communication processor CP 443-1 Multi (Industrial Ethernet ISO and TCP/IP, 4-port switch, gigabit port) | 6GK7 443–5FX01–0XE0 | As of firmware V3.1 | Yes | Yes |
### Function modules and communication processors supported by the S7-400H

<table>
<thead>
<tr>
<th>Module</th>
<th>Order No.</th>
<th>Release</th>
<th>One-sided</th>
<th>Redundant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communication processor CP 443-5 Extended (PROFIBUS; master on PROFIBUS DP)</td>
<td>6GK7 443–5FX02–0XE0</td>
<td>As of product version 1 as of firmware V3.2</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td></td>
<td>6GK7 443–5DX02–0XE0</td>
<td>As of product version 2 as of firmware V3.2.3</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Communication processor CP 443-5 Extended (PROFIBUS DPV1)</td>
<td>6GK7 443–5DX03–0XE0</td>
<td>As of product version 1 as of firmware V5.1.4</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td></td>
<td>6GK7 443–5DX04–0XE0</td>
<td>As of product version 1 as of firmware V6.0</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td></td>
<td>6GK7 443–5DX05–0XE0</td>
<td>As of product version 1 as of firmware V7.1</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

1) Only these modules should be used as external master interfaces on the PROFIBUS DP.
2) These modules support DPV1 as external DP master interface module (complying with IEC 61158/EN 50170).

### FMs and CPs usable for distributed one-sided use

**Note**

You can use all the FMs and CPs released for the ET 200M with the S7-400H in distributed and one-sided mode.

### FMs and CPs usable for distributed switched use

<table>
<thead>
<tr>
<th>Module</th>
<th>Order No.</th>
<th>Release</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communication processor CP 341–1 (point-to-point link)</td>
<td>6ES7 341-1AH00–0AE0 6ES7 341-1BH00–0AE0 6ES7 341-1CH00–0AE0</td>
<td>As of product version 3</td>
</tr>
<tr>
<td></td>
<td>6ES7 341-1AH01–0AE0 6ES7 341-1BH01–0AE0 6ES7 341-1CH01–0AE0</td>
<td>As of product version 1 as of firmware V1.0.0</td>
</tr>
<tr>
<td></td>
<td>6ES7 341-1AH02–0AE0 6ES7 341-1BH02–0AE0 6ES7 341-1CH02–0AE0</td>
<td>As of product version 1 as of firmware V2.0.0</td>
</tr>
<tr>
<td>Communication processor CP 342–2 (ASI bus interface module)</td>
<td>6GK7 342–2AH01–0XA0</td>
<td>As of product version 1 as of firmware V1.10</td>
</tr>
<tr>
<td>Communication processor CP 343–2 (ASI bus interface module)</td>
<td>6GK7 343–2AH00–0XA0</td>
<td>As of product version 2 as of firmware V2.03</td>
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<tr>
<td>Counter module FM 350–1</td>
<td>6ES7 350–1AH01–0AE0 6ES7 350–1AH02–0AE0</td>
<td>As of product version 1</td>
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<tr>
<td>Counter module FM 350–2</td>
<td>6ES7 350–2AH00–0AE0</td>
<td>As of product version 2</td>
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<tr>
<td>Control module FM 355 C</td>
<td>6ES7 355–0VH10–0AE0</td>
<td>As of product version 4</td>
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<tr>
<td>Control module FM 355 S</td>
<td>6ES7 355–1VH10–0AE0</td>
<td>As of product version 3</td>
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<tr>
<td>Module</td>
<td>Order No.</td>
<td>Release</td>
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<tr>
<td>-----------------------------------------</td>
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<tr>
<td>High-speed Boolean processor FM 352–5</td>
<td>6ES7352–5AH00–0AE0</td>
<td>As of product version 1</td>
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<td>As of firmware V1.0.0</td>
</tr>
<tr>
<td>Control module FM 355–2 C</td>
<td>6ES7 355–0CH00–0AE0</td>
<td>As of product version 1</td>
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<td></td>
<td>As of firmware V1.0.0</td>
</tr>
<tr>
<td>Control module FM 355–2 S</td>
<td>6ES7 355–0SH00–0AE0</td>
<td>As of product version 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>As of firmware V1.0.0</td>
</tr>
</tbody>
</table>

**Note**

One-sided or switched function and communication modules are **not** synchronized in the fault-tolerant system if they are in pairs, e.g. two identical FM 450 modules operating in one-sided mode do **not** synchronize their counter states.
Connection examples for redundant I/Os

E.1 SM 321; DI 16 x DC 24 V, 6ES7 321–1BH02–0AA0

The diagram below shows the connection of two redundant encoders to two SM 321; DI 16 x DC 24 V. The encoders are connected to channel 0.

![Diagram of encoder connection](image)
The diagram below shows the connection of two redundant encoder pairs to two redundant SM 321; DI 32 x DC 24 V. The encoders are connected to channel 0 and channel 16 respectively.

Figure E-2 Example of an interconnection with SM 321; DI 32 x DC 24 V
E.3 SM 321; DI 16 x AC 120/230V, 6ES7 321–1FH00–0AA0

The diagram below shows the connection of two redundant encoders to two SM 321; DI 16 x AC 120/230 V. The encoders are connected to channel 0.

Figure E-3 Example of an interconnection with SM 321; DI 16 x AC 120/230 V
E.4 SM 321; DI 8 x AC 120/230 V, 6ES7 321–1FF01–0AA0

The diagram below shows the connection of two redundant encoders to two SM 321; DI 8 AC 120/230 V. The encoders are connected to channel 0.

Figure E-4 Example of an interconnection with SM 321; DI 8 x AC 120/230 V
The diagram below shows the connection of two redundant encoder pairs to two SM 321; DI 16 x DC 24V. The encoders are connected to channels 0 and 8.

Figure E-5  Example of an interconnection with SM 321; DI 16 x DC 24V
E.6 SM 321; DI 16 x DC 24V, 6ES7 321–7BH01–0AB0

The diagram below shows the connection of two redundant encoder pairs to two SM 321; DI 16 x DC 24V. The encoders are connected to channels 0 and 8.

Figure E-6 Example of an interconnection with SM 321; DI 16 x DC 24V
E.7 SM 326; DO 10 x DC 24V/2A, 6ES7 326–2BF01–0AB0

The diagram below shows the connection of an actuator to two redundant SM 326; DO 10 x DC 24V/2A. The actuator is connected to channel 1.

Figure E-7  Example of an interconnection with SM 326; DO 10 x DC 24V/2A
E.8 SM 326; DI 8 x NAMUR, 6ES7 326–1RF00–0AB0

The diagram below shows the connection of two redundant encoders to two redundant SM 326; DI 8 x NAMUR. The encoders are connected to channel 4.

Figure E-8 Example of an interconnection with SM 326; DI 8 x NAMUR
Connection examples for redundant I/Os

E.9 SM 326; DI 24 x DC 24 V, 6ES7 326–1BK00–0AB0

The diagram below shows the connection of one encoder to two redundant SM 326; DI 24 x DC 24 V. The encoder is connected to channel 13.

Figure E-9  Example of an interconnection with SM 326; DI 24 x DC 24 V
E.10  SM 421; DI 32 x UC 120 V, 6ES7 421–1EL00–0AA0

The diagram below shows the connection of a redundant encoder to two SM 421; DI 32 x UC 120 V. The encoder is connected to channel 0.

Figure E-10  Example of an interconnection with SM 421; DI 32 x UC 120 V
E.11 SM 421; DI 16 x DC 24 V, 6ES7 421–7BH01–0AB0

The diagram below shows the connection of two redundant encoders pairs to two SM 421; DI 16 x DC 24 V. The encoders are connected to channel 0 and 8.

Figure E-11 Example of an interconnection with SM 421; DI 16 x DC 24 V
Connection examples for redundant I/Os

E.12 SM 421; DI 32 x DC 24 V, 6ES7 421–1BL00–0AB0

The diagram below shows the connection of two redundant encoders to two SM 421; DI 32 x 24 V. The encoders are connected to channel 0.

Figure E-12 Example of an interconnection with SM 421; DI 32 x 24 V
The diagram below shows the connection of two redundant encoders to two SM 421; DI 32 x 24 V. The encoders are connected to channel 0.

Figure E-13  Example of an interconnection with SM 421; DI 32 x 24 V
E.14 SM 322; DO 8 x DC 24 V/2 A, 6ES7 322–1BF01–0AA0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 8 x DC 24 V. The actuator is connected to channel 0.

Types with $U_r \geq 200$ V and $I_F \geq 2$ A are suitable as diodes.

Figure E-14  Example of an interconnection with SM 322; DO 8 x DC 24 V/2 A
E.15 SM 322; DO 32 x DC 24 V/0,5 A, 6ES7 322–1BL00–0AA0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 32 x DC 24 V. The actuator is connected to channel 1.

Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_r \geq 200\, V$ and $I_F \geq 1\, A$.

Figure E-15 Example of an interconnection with SM 322; DO 32 x DC 24 V/0.5 A
Connection examples for redundant I/Os

E.16 SM 322; DO 8 x AC 230 V/2 A, 6ES7 322–1FF01–0AA0

The diagram below shows the connection of an actuator to two SM 322; DO 8 x AC 230 V/2 A. The actuator is connected to channel 0.

Figure E-16 Example of an interconnection with SM 322; DO 8 x AC 230 V/2 A
E.17  SM 322; DO 4 x DC 24 V/10 mA [EEex ib], 6ES7 322–5SD00–0AB0

The diagram below shows the connection of an actuator to two SM 322; DO 16 x DC 24 V/10 mA [EEex ib]. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with U_r >= 200 V and I_F >= 1 A.

Figure E-17  Example of an interconnection with SM 322; DO 16 x DC 24 V/10 mA [EEex ib]
E.18  SM 322; DO 4 x DC 15 V/20 mA [EEx ib], 6ES7 322–5RD00–0AB0

The diagram below shows the connection of an actuator to two SM 322; DO 16 x DC 15 V/20 mA [EEx ib]. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_r \geq 200$ V and $I_F \geq 1$ A.
E.19 SM 322; DO 8 x DC 24 V/0.5 A, 6ES7 322–8BF00–0AB0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 8 x DC 24 V/0.5 A. The actuator is connected to channel 0.

Figure E-19  Example of an interconnection with SM 322; DO 8 x DC 24 V/0.5 A
E.20 SM 322; DO 16 x DC 24 V/0.5 A, 6ES7 322–8BH01–0AB0

The diagram below shows the connection of an actuator to two redundant SM 322; DO 16 x DC 24 V/0.5 A. The actuator is connected to channel 8.
The diagram below shows the connection of two actuators to two redundant SM 332; AO 8 x 12 Bit. The actuators are connected to channels 0 and 4. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_r \geq 200\, \text{V}$ and $I_F \geq 1\, \text{A}$.

Figure E-21 Example of an interconnection with SM 332, AO 8 x 12 Bit
Connection examples for redundant I/Os

E.22 SM 332; AO 4 x 0/4...20 mA [EEEx ib], 6ES7 332–5RD00–0AB0

The diagram below shows the connection of an actuator to two SM 332; AO 4 x 0/4...20 mA [EEEx ib]. The actuator is connected to channel 0. Suitable diodes are, for example, types from the series 1N4003 ... 1N4007 or any other diode with $U_r \geq 200$ V and $I_F \geq 1$ A.

![Diagram](image)

Figure E-22 Example of an interconnection with SM 332; AO 4 x 0/4...20 mA [EEEx ib]
The diagram below shows the connection of an actuator to two SM 422; DO 16 x 120/230 V/2 A. The actuator is connected to channel 0.

Figure E-23  Example of an interconnection with SM 422; DO 16 x 120/230 V/2 A
The diagram below shows the connection of an actuator to two SM 422; DO 32 x 24 V/0.5 A. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_r \geq 200$ V and $I_F \geq 1$ A.
The diagram below shows the connection of a 2-wire transmitter to two SM 331; AI 4 x 15 Bit [EEx ib]. The transmitter is connected to channel 1. Suitable Zener diode: BZX85C6v2.
The diagram below shows the connection of a transmitter to two SM 331; AI 8 x 12 Bit. The transmitter is connected to channel 0.

Figure E-26  Example of an interconnection with SM 331; AI 8 x 12 Bit
E.27 SM 331; AI 8 x 16 Bit; 6ES7 331–7NF00–0AB0

The figure below shows the connection of a transmitter to two redundant SM 331; AI 8 x 16 Bit. The transmitter is connected to channel 0 and 7 respectively.

Figure E-27 Example of an interconnection with SM 331; AI 8 x 16 Bit
The figure below shows the connection of a transmitter to two redundant SM 331; AI 8 x 16 Bit. The transmitter is connected to channel 0 and 3 respectively.

Figure E-28 Example of an interconnection with SM 331; AI 8 x 16 Bit
The figure below shows the connection of a thermocouple to two redundant SM 331 AI 6xTC 16Bit iso.

Figure E-29  Example of an interconnection AI 6xTC 16Bit iso
E.30  **SM331; AI 8 x 0/4...20mA HART, 6ES7 331-7TF01-0AB0**

The diagram below shows the connection of a 4-wire transmitter to two redundant SM 331; AI 8 x 0/4...20mA HART.

![Diagram of SM331 connection](image)

Figure E-30  Interconnection example 1 SM 331; AI 8 x 0/4...20mA HART
The diagram below shows the connection of a 2-wire transmitter to two redundant SM 331; AI 8 x 0/4...20mA HART.

Figure E-31 Interconnection example 2 SM 331; AI 8 x 0/4...20mA HART
E.31 SM 332; AO 4 x 12 Bit; 6ES7 332–5HD01–0AB0

The diagram below shows the connection of an actuator to two SM 332; AO 4 x 12 Bit. The actuator is connected to channel 0. Suitable diodes are, for example, those of the series 1N4003 ... 1N4007, or any other diode with $U_r \geq 200$ V and $I_F \geq 1$ A.

![Diagram of actuator connection](image-url)

Figure E-32 Example of an interconnection with SM 332, AO 4 x 12 Bit
E.32 SM332; AO 8 x 0/4...20mA HART, 6ES7 332-8TF01-0AB0

The diagram below shows the connection of an actuator to two SM 332; AO 8 x 0/4...20 mA HART.

![Diagram](image)

Figure E-33 Interconnection example 3 SM 332; AO 8 x 0/4...20mA HART
E.33 SM 431; AI 16 x 16 Bit, 6ES7 431–7QH00–0AB0

The diagram below shows the connection of a sensor to two SM 431; AI 16 x 16 Bit. Suitable Zener diode: BZX85C6v2.
Glossary

1-out-of-2 system

See dual-channel fault-tolerant system

Comparison error

An error that may occur while memories are being compared on a fault-tolerant system.

Dual-channel fault-tolerant system

Fault-tolerant system with two central processing units

ERROR-SEARCH

An operating mode of the reserve CPU of a fault-tolerant system in which the CPU performs a complete self-test.

Fail-safe systems

Fail-safe systems are characterized by the fact that, when certain failures occur, they remain in a safe state or go directly to another safe state.

Fault-tolerant station

A fault-tolerant station containing two central processing units (master and reserve).

Fault-tolerant system

A fault-tolerant system consists of at least two central processing units (master and reserve). The user program is processed identically in both the master and reserve CPUs.

Fault-tolerant systems

Fault-tolerant systems are designed to reduce production downtime. Availability can be enhanced, for example, by means of component redundancy.

I/O, one-sided

We speak of a one-sided I/O when an input/output module can be accessed by only one of the redundant central processing units. It may be single-channel or multi-channel (redundant) module.
I/O, redundant
We speak of a redundant I/O when there is more than one input/output module available for a process signal. It may be connected as one-sided or switched module. Terminology: "Redundant one-sided I/O" or "Redundant switched I/O"

I/O, single-channel
When there is only one input/output module for a process signal, in contrast to a redundant I/O, this is known as a single-channel I/O. It may be connected as one-sided or switched module.

I/O, switched
We speak of a switched I/O when an input/output module can be accessed by all of the redundant central processing units of a fault-tolerant system. It may be single-channel or multi-channel (redundant) module.

Link-up
In the link-up system mode of a fault-tolerant system, the master CPU and the reserve CPU compare the memory configuration and the contents of the load memory. If they establish differences in the user program, the master CPU updates the user program of the reserve CPU.

Master CPU
The central processing unit that is the first redundant central processing unit to start up. It continues to operate as the master when the redundancy connection is lost. The user program is processed identically in both the master and reserve CPUs.

Mean Down Time (MDT)
The mean down time MDT essentially consists of the time until error detection and the time required to repair or replace defective modules.

Mean Time Between Failures (MTBF)
The average time between two failures and, consequently, a criterion for the reliability of a module or a system.

Mean Time to Repair (MTTR)
The mean time to repair MTTR denotes the average repair time of a module or a system, in other words, the time between the occurrence of an error and the time when the error has been rectified.
Glossary

Redundancy, functional
Redundancy with which the additional technical means are not only constantly in operation but also involved in the scheduled function. Synonym: active redundancy.

Redundant
In redundant system mode of a fault-tolerant system the central processing units are in RUN mode and are synchronized over the redundant link.

Redundant link
A link between the central processing units of a fault-tolerant system for synchronization and the exchange of data.

Redundant systems
Redundant systems are characterized by the fact that important automation system components are available more than once (redundant). When a redundant component fails, processing of the program is not interrupted.

Reserve CPU
The redundant central processing unit of a fault-tolerant system that is linked to the master CPU. It goes to STOP mode when the redundancy connection is lost. The user program is processed identically in both the master and reserve CPUs.

Self-test
In the case of fault-tolerant CPUs defined self-tests are executed during startup, cyclical processing and when comparison errors occur. They check the contents and the state of the CPUs and the I/Os.

Single mode
An H system changes to single mode, when it was configured to be redundant and only one CPU is in RUN. This CPU is then automatically the master CPU.

Stand-alone operation
Stand-alone mode is the use of a fault-tolerant CPU in a standard SIMATIC-400 station.

Stop
With fault-tolerant systems: In the stop system mode of a fault-tolerant system, the central processing units of the fault-tolerant system are in STOP mode.
**Synchronization module**

An interface module for the redundant link in a fault-tolerant system.

**Update**

In the update system mode of a fault-tolerant system, the master CPU updates the dynamic data of the reserve CPU.
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