S7-400 Instruction List

CPU 412, 414, 416, 417

This Instruction List has the order number:

6ES7498-8AA04-8BN0

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Siemens Aktiengesellschaft

6ES7498-8AA04-8BN0

Contents

Applicability

This list of instructions applies to the CPUs listed below.

Name	Order number	subsequently described as[1)]
CPU 412-1	6ES7412-1XF04-0AB0	CPU 412
CPU 412-2	6ES7412-2XG04-0AB0	
CPU 414-2	6ES7414-2XG04-0AB0	CPU 414
CPU 414-3	6ES7414-3XJ04-0AB0	
CPU 414-4H	6ES7414-4HJ04-0AB0	
CPU 416-2	6ES7416-2XK04-0AB0	CPU 416
CPU 416F-2	6ES7416-2FK04-0AB0	
CPU 416-3	6ES7416-3XL04-0AB0	
CPU 417-4	6ES7417-4XL04-0AB0	CPU 417
CPU 417-4 H	6ES7417-4HL04-0AB0	

1) except in the tables, where a detailled differentiation is necessary

Address Identifier and Parameter Ranges

Addr. ID	Parameter Range				Description
	CPU 412	**CPU 414**	**CPU 416**	**CPU 417**	
Q[2)]	0.0 to 127.7	0.0 to 255.7	0.0 to 511.7	0.0 to 1023.7	Output (in PIQ)
QB[2)]	0 to 127	0 to 255	0 to 511	0 to 1023	Output byte (in PIQ)
QW[2)]	0 to 126	0 to 254	0 to 510	0 to 1022	Output word (in PIQ)
QD[2)]	0 to 124	0 to 252	0 to 508	0 to 1020	Output double word (in PIQ)
DBX	0.0 to 65533.7[1)]	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in data block
DB	1 to 511	1 to 4095	1 to 4095	1 to 8191	Data block
DBB	0 to 65533[1)]	0 to 65533	0 to 65533	0 to 65533	Data byte in DB
DBW	0 to 65532*[1)]	0 to 65532	0 to 65532	0 to 65532	Data word in DB
DBD	0 to 65530[1)]	0 to 65530	0 to 65530	0 to 65530	Data double word in DB
DIX	0.0 to 65533.7[1)]	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in instance DB
DI	1 to 511	1 to 4095	1 to 4095	1 to 8191	Instance data block
DIB	0 to 65533[1)]	0 to 65533	0 to 65533	0 to 65533	Data byte in instance DB
DIW	0 to 65532[1)]	0 to 65532	0 to 65532	0 to 65532	Data word in instance DB
DID	0 to 65530[1)]	0 to 65530	0 to 65530	0 to 65530	Data double word instance DB

1) Also restricted by the size of the working memory.

2) Default setting can be changed, see Technical Specifications

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range				Description
	CPU 412	**CPU 414**	**CPU 416**	**CPU 417**	
I[2)]	0.0 to 127.7	0.0 to 255.7	0.0 to 511.7	0.0 to 1023.7	Input bit (in PII)
IB[2)]	0 to 127	0 to 255	0 to 511	0 to 1023	Input byte (in PII)
IW[2)]	0 to 126	0 to 254	0 to 510	0 to 1022	Input word (in PII)
ID[2)]	0 to 124	0 to 252	0 to 508	0 to 1020	Input double word (in PII)
L[2)]	0.0 to 4095.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 32767.7	Local data
LB[2)]	0 to 4095	0 to 8191	0 to 16383	0 to 32767	Local data byte
LW[2)]	0 to 4094	0 to 8190	0 to 16382	0 to 32766	Local data word
LD[2)]	0 to 4092	0 to 8188	0 to 16380	0 to 32764	Local data double word
M	0.0 to 4095.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 16383.7	Bit memory
MB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	memory byte
MW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	memory word
MD	0 to 4092	0 to 8188	0 to 16380	0 to 16380	memory double word

2) Default setting can be changed, see Technical Specifications

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range				Description
	CPU 412	**CPU 414**	**CPU 416**	**CPU 417**	
PQB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Peripheral output byte (direct I/O access)
PQW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Peripheral output word (direct I/O access)
PQD	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Peripheral output double word (direct I/O access)
PIB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Peripheral input byte (direct I/O access)
PIW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Peripheral input word (direct I/O access)
PID	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Peripheral output double word (direct I/O access)
T	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Timer
C	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Counter

Constants and Ranges

Constant	Range	Description
B(b1,b2) B(b1,b2,b3,b4)	–	Constant, 2 or 4 bytes
D# Date	–	IEC date constant
L# Integer	–	32-bit integer constant
P# Bit pointer	–	Pointer constant
S5T# Time value	–	S7 time constant [1]
T# TIme value	–	Time constant
TOD# Time value	–	IEC time constant
C# Count value	–	Counter constant (BCD code)
2#n	–	Binary constant
W#16# DW#16#	–	Hexadecimal constant

1) For loading of S7 timers.

Abbreviations and Mnemonics

The following abbreviations and mnemonics are used in the Instruction List:

Abbrev.	Description	Example
k8	8-bit constant 0 to 255	32
k16	16-bit constant 256 to 32 767	28 131
k32	32-bit constant 32 768 to 999 999 999	127 624
i8	8-bit integer -128 to +127	-113
i16	16-bit integer -32768 to +32767	+6523
i32	32-bit integer -2 147 483 648 to +2 147 483 647	-2 222 222
m	Pointer constant	P#240.3
n	Binary constant	1001 1100
p	Hexadecimal constant	EA12
Label	Symbolic jump address (max. 4 characters)	DESTINATION
a	Byte address	

Abbreviations and Mnemonics, continued

Abbrev.	Description	Example
b	Bit address	
c	Address area	I, Q, M, L, DBX, DIX
d	Address in: MD, DBD, DID or LD	
e	Number in: MW, DBW, DIW or LW	
f	Timer/counter No.	
g	Address area	IB, QB, PIB, PQB, MB, LB, DBB, DIB
h	Address area	IW, QW, PIW, PQW, MW, LW, DBW, DIW
i	Address area	ID, QD, PID, PQD, MD, LD, DBD, DID
q	Block No.	

Registers

ACCU1 to ACCU4 (32 Bits)

The accumulators are registers for processing bytes, words or double words. The address identifiers are loaded into the accumulators, where they are logically gated. The result of the logic operation (RLO) is in ACCU1 and can be transferred from there to a memory cell.

The accumulators are 32 bits long.

Accumulator designations :

ACCU	Bits
ACCUx (x = 1 to 4)	Bit 0 to 31
ACCUx-L	Bit 0 to 15
ACCUx-H	Bit 16 to 31
ACCUx-LL	Bit 0 to 7
ACCUx-LH	Bit 8 to 15
ACCUx-HL	Bit 16 to 23
ACCUx-HH	Bit 24 to 31

Address Registers AR1 and AR2 (32 Bits)

The address registers contain the area-internal or area-crossing pointers for instructions using indirect addressing. The address registers are 32 bits long.

The area-internal and/or area-crossing pointers have the following syntax:

- Area-internal pointer `00000000 00000bbb bbbbbbbb bbbbbxxx`
- Area-crossing pointer **`yyyyyyyy`** `00000bbb bbbbbbbb bbbbbxxx`

Legend:

`b`	Byte address
`x`	Bit number
`y`	Area identifier (see “Examples of Addressing”)

Status Word (16 Bits)

The status word bits are evaluated or set by the instructions.

The status word is 16 bits long.

Bit	Assignment	Description
0	/FC	First check bit
1	RLO	Result of logic operation
2	STA	Status
3	OR	Or (AND before OR)
4	OS	Stored overflow
5	OV	Overflow
6	CC 0	Condition code 0
7	CC 1	Condition code 1
8	BR	Binary result
9 to 15	Unassigned	–

Examples of Addressing

Addressing Examples	Description
Immediate Addressing	
L +27	Load 16-bit integer constant “27” into ACCU1
L L#-1	Load 32-bit integer constant “-1” into ACCU1
L 2#1010101010101010	Load binary constant into ACCU1
L DW#16#A0F0BCFD	Load hexadecimal constant into ACCU1
L ’ENDE’	Load ASCII character into ACCU1
L T#500 ms	Load time value into ACCU1
L C#100	Load count value into ACCU1
L B#(100,12)	Load 2-byte constant
L B#(100,12,50,8)	Load 4-byte constant
L P#10.0	Load area-internal pointer into ACCU1
L P#E20.6	Load area-crossing pointer into ACCU1
L -2.5	Load real number into ACCU1
L D# 1995-01-20	Load date
L TOD 13:20:33.125	Load time of day

Addressing Examples	Description
Direct Addressing	
A I 0.0	ANDing of input bit 0.0
L IB 1	Load input byte 1 into ACCU1
L IW 0	Load input word 0 into ACCU1
L ID 0	Load input double word 0 into ACCU1
Indirect Addressing of Timers/Counters	
SP T [LW 8]	Start timer; the timer number is in local data word 8
CU C [LW 10]	Count upwards; the counter number is in local data word 10
Area-Internal Memory-Indirect Addressing	
A I [LD 12] Example: L P#22.2 T LD 12 A I [LD 12]	AND operation: The address of the input is in local data double word 12 as pointer
A I [DBD 1]	AND operation: The address of the input is in data double word 1 of the open DB as pointer
A I [DID 12]	AND operation: The address of the output is in data double word 12 of the open instance DB as pointer
A I [MD 12]	AND operation: The address of the output is in memory double word 12 as pointer

Examples of Addressing, continued

Addressing Examples
Area-Internal Register-Indirect Addressing
A I [AR1,P#12.2]
Area-Crossing Register-Indirect Addressing

For area-crossing register-indirect addressing, the address must also contain an area identifier. The address is in the address register. The area identifiers are as follows:

Area identifier	Coding (binary)	hex.	Area
P	1000 0**000**	80	I/O area
I	1000 0**001**	81	Input area
Q	1000 0**010**	82	Output area
M	1000 0**011**	83	Bit memory area
DB	1000 0**100**	84	Data area
DI	1000 0**101**	85	Instance data area
L	1000 0**110**	86	Local data area
VL	1000 0**111**	87	Predecessor local data area (access to local data of invoking block)

L B [AR1,P#8.0]	Load byte into ACCU1: The address is calculated from the “pointer value in AR 1 + P#8.0”
A [AR1,P#32.3]	AND operation: The address of the operand is calculated from the “pointer value in AR 1 + P#32.3”
Addressing Via Parameters	
A Parameter	Addressing via parameters

Examples of how to calculate the pointer

- **Example for sum of bit addresses ≦7:**

  LAR1 P#8.2
  A I [AR1,P#10.2]

Result: Input 18.4 is addressed (by adding the byte and bit addresses)

- **Example for sum of bit addresses＞7:**

  L P#10.5
  LAR1
  A I [AR1,P#10.7]

Result: Input 21.4 is addressed (by adding the byte and bit addresses with carry over)

Execution Times with Indirect Addressing

When using indirect addresses statement consists of two parts:

Part 1: Load the address of the instruction

Part 2: Execute the instruction

In other words, when working with indirect addresses, you must calculate the execution time of an instruction from these two parts.

Calculating the Execution Time

The total execution time is calculated as follows:

	Time required for loading the address
+	execution time of the instruction
=	Total execution time of the instruction

The execution times listed in the chapter entitled “List of Instructions” apply to the execution times of the second part of an instruction, i.e. for the actual execution of an instruction.

You must then add the time required for loading the address of the instruction to this execution time (see following Table).

The execution time for loading the address of the instruction from the various areas is shown in the following table.

Address is in ...	Execution Time in µs			
	CPU 412	**CPU 414**	**CPU 416**	**CPU 417**
Bit memory area M				
Word	0.2	0.12	0.08	0.06
Double word	0.2	0.12	0.08	0.06
Data block DB/DX				
Word	0.3	0.18	0.12	0.12
Double word	0.3	0.18	0.12	0.12
Local data area L				
Word	0.2	0.12	0.08	0.06
Double word	0.2	0.12	0.08	0.06
AR1/AR2 (area-internal)	0.0 [1)]	0.0 [1)]	0.0 [1)]	0.0 [1)]
AR1/AR2 (area-crossing)	0.0 [1)]	0.0 [1)]	0.0 [1)]	0.0 [1)]
Parameter (word) ... for:				
• Timers	0.4	0.24	0.16	0.15
• Counters	0.4	0.24	0.16	0.15
• Block calls	0.4	0.24	0.16	0.15
Parameter (double word) ... for Bits, bytes, words and double words	0.4	0.24	0.16	0.15

1) Address registers AR1/AR2 do not need to be loaded in separate cycles for addressing.

The pages that follow contain examples for calculating the instruction run time for the various indirectly addressed instructions.

Examples of Calculations

You will find a few examples here for calculating the execution times for the various methods of indirect addressing.

Calculating the Execution Times for Area-Internal Memory-Indirect Addressing

Example: A I [DBD 12] with CPU 414

Step 1: Load the contents of DBD 12 (time required is listed in the table on page 20)

Address is in ...	Execution Time in µs
Bit memory area M	
Word	0.2
Double word	0.3
Data block DB/DX	
Word	0.2
Double word	0.3

Step 2: AND the input addressed in this way (you will find the execution time in the tables in the chapter entitled “List of Instructions” on page 25)

Typical Execution Time in µs	
Direct Addressing	**Indirect Addressing**
0.06/0.075	Time for A I **0.06+**
:	**:**

Total execution time:

0.18 µs
+ 0.06 µs
0.24 µs

Execution Time for Area-Crossing Register-Indirect Addressing

Example: A [AR1, P#23.1] ... with I 1.0 in AR1 with CPU 416

Step 1: Load the contents of AR1, and increment them by the offset 23.1 (the time required is in the table on page 20)

Address is in ...	Execution Time in µs
:	:
AR1/AR2 (area-crossing)	0.00
:	:

Step 2: AND link of the input addressed this way (see page 25 for the execution time)

Typical Execution Time in µs	
Direct Addressing	**Indirect Addressing**
0.04/0.05	Time for A I **0.05+**
:	**:**

Total execution time:

0.00 µs
+ 0.05 µs
0.05 µs

List of Instructions

This chapter contains the complete list of instructions for the S7-400 CPUs. The descriptions have been kept as concise as possible. You will find a detailed functional description in the various STEP 7 reference manuals.
Please note that, in the case of indirect addressing (examples see page 16), you must add the time required for loading the address of the particular instruction to the execution times listed (see page 19).

Bit Logic Instructions

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RLO from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the /FC bit is set to zero.

Instr.	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
U/UN							
	I/Q a.b	Input/output	1[1]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	M a.b	Bit memory	1[2]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	L a.b	Local data bit	2	0.125	0.075	0.05	0.042
	DBX a.b	Data bit	2	0.2	0.12	0.08	0.09
	DIX a.b	Instance data bit	2	0.2	0.12	0.08	0.09
	c [d]	Memory-indirect, area-internal[3]	2	0,1+/0,2+	0,06+/0,12+	0,04+/0,08+	0,04+/0,08+
	c [AR1,m]	Register-ind., area-internal (AR1)[3]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,05/0,08
	c [AR2,m]	Register-ind., area-internal (AR2)[3]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,05/0,08
	[AR1,m]	Area-crossing (AR1)***	2	0,125/0,2	0,075/0,12	0,05/0,08	0,05/0,08
	[AR2,m]	Area-crossing (AR2)***	2	0,125/0,2	0,075/0,12	0,05/0,08	0,05/0,08
	Parameter	Via parameter ***	2	0,525/0,6	0,315/0,36	0,21/0,24	0,21/0,24

Statusword for: **U/UN**	BIE	A1	A0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing;Address area 0 to 127
2) With direct instruction addressing;Address area 0 to 255
3) I,Q,M,L / DB, DI

Bit Logic Instructions, continued

Instr.	Address ID	Description	Length in Words	CPU 412	CPU 414	CPU 416	CPU 417
O/ON		OR/OR-NOT					
	I/Q a.b	Input/output	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	M a.b	Bit memory	1[2)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	L a.b	Local da	2	0.125	0.075	0.05	0.042
	DBX a.b	Data bit	2	0.2	0.12	0.08	0.09
	DIX a.b	Instance data bit	2	0.2	0.12	0.08	0.09
	c [d]	Memory-indirect, area-internal [3)]	2	0,1+/0,2+	0,06+/0,12+	0,06+/0,12+	0,03+/0,09+
	c [AR1,m]	Register-ind., area-internal (AR1) [3)]	2	0,125/0,2	0,075/0,12	0,075/0,12	0,042/0,09
	c [AR2,m]	Register-ind., area-internal (AR2) [3)]	2	0,125/0,2	0,075/0,12	0,075/0,12	0,042/0,09
	[AR1,m]	Area-crossing (AR1) ***	2	0,125/0,2	0,075/0,12	0,075/0,12	0,042/0,09
	[AR2,m]	Area-crossing (AR2) ***	2	0,125/0,2	0,075/0,12	0,075/0,12	0,042/0,09
	Parameter	Via parameter ***	2	0,525/0,6	0,315/0,36	0,315/0,36	0,192/0,24

Statusword for: **O, ON**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; Address area 0 to 127

2) With direct instruction addressing; Address area 0 to 255

3) I,Q,M,L / DB, DI

Bit Logic Instructions, continued

Instr.	Address-ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
X/XN		EXKLUSIV-OR/ EXKLUSIV-OR-NOT					
	E/A a.b	Input/output	2	0.125	0.075	0.05	0.042
	M a.b	Bit memory	2	0.125	0.075	0.05	0.042
	L a.b	Local data bit	2	0.125	0.075	0.05	0.042
	DBX a.b	Data bit	2	0.2	0.12	0.08	0.09
	DIX a.b	Instance data bit	2	0.2	0.12	0.08	0.09
	c [d]	Memory-indirect, area-internal. 1)	2	0,1+/0,2+	0,06+/0,12+	0,04+/0,08+	0,03+/0,09+
	c [AR1,m]	Register-ind., area-internal (AR1) 1)	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	c [AR2,m]	Register-ind., area-internal (AR2) 1)	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	[AR1,m]	Area-crossing (AR1) 1)	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	[AR2,m]	Area-crossing (AR2) 1)	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	Parameter	Via parameter 1)	2	0,525/0,6	0,315/0,36	0,21/0,24	0,192/0,24

Status word for: **X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

+Plus time required for loading the address of the instruction (see page 20)

1) I,Q,M,L / DB, DI

Bit Logic Instructions with Parenthetical Expressions

Saving the RLO and OR bits and the relevant function identifier (A, AN, ...) to the nesting stack. Seven nesting levels are possible per block. After the right parenthesis, the logic operation indicated by the function identifier is performed on the saved RLO and the current RLO; the current OR is overwritten with the saved OR.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
U(		AND left parenthesis	1	0.1	0.06	0.04	0.03
UN(		AND NOT left parenthesis	1	0.1	0.06	0.04	0.03
O(		OR left parenthesis	1	0.1	0.06	0.04	0.03
ON(		OR NOT left parenthesis	1	0.1	0.06	0.04	0.03
X(		Exclusive OR left parenthesis	1	0.1	0.06	0.04	0.03
XN(		EXKLUSIV-ODER-NICHT-Klam-parenthesis	1	0.1	0.06	0.04	0.03

Statusword for: **U(, UN(, O(, ON(, X(, XN(**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	1	–	0

Bit Logic Instructions with Parenthetical Expressions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
)		Right parenthesis, removing an entry from the nesting stack.	1	0.1	0.06	0.04	0.03

Statusword for: **)**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	Yes	1	Yes	1

ORing of AND Instructions

The ORing of AND instructions is implemented according to the rule: AND before OR.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
O		ORing of AND operations according to the rule: AND before OR	1	0.1	0.06	0.04	0.03

Status word for: **O**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	1	–	Yes

Logic Instructions with Timers and Counters

Examining the status of the addressed timer/counter and gating the result with the RLO according to the appropriate logic function.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN		AND/AND NOT					
	T f	Timer	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	T [e]	Timer, memory-indirect addressing	2	0.1+	0.06+	0.04+	0.03+
	C f	Counter	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	C [e]	Counter, memory-indirect addressing	2	0.1+	0.06+	0.04+	0.03+
	Timerpara. Counter para.	Timer/counter (addressing via parameter)	2	0.5 0.5	0.3 0.3	0.2 0.2	0.18 0.18

Status word for: **A, AN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing ;Address area 0 to 255

Logic Instructions with Timers and Counters, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
O/ON	T f T [e] C f C [e]	Timer Timer, memory-indirect addr. Counter Counter, memory-indirect addressing	1[1])/2 2 1[1])/2 2	0.1/0.125 0.1+ 0.1/0.125 0.1+	0.06/0.075 0.06+ 0.06/0.075 0.06+	0.04/0.05 0.04+ 0.04/0.05 0.04+	0.03/0.042 0.03+ 0.03/0.042 0.03+
	Timerpara. Counterpara.	Timer/counter (addressing via parameter)	2	0.5 0.5	0.3 0.3	0.2 0.2	0.18 0.18
X/XN		EXCLUSIVE OR/EXCLUSIVE OR NOT					
	T f T [e] C f C [e]	Timer Timer, memory-indirect addr. Counter Counter, mem.-indirect addr.	2 2 2 2	0.125 0.1+ 0.125 0.1+	0.075 0.06+ 0.075 0.06+	0.05 0.04+ 0.05 0.04+	0.042 0.03+ 0.042 0.03+
	Timerpara. Counterpara.	EXCLUSIVE OR timer/counter (addressing via parameter)	2	0.5 0.5	0.3 0.3	0.2 0.2	0.18 0.18

Status word for: **O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; address area 0 to 255

Word Logic Instructions with the Contents of Accumulator 1

Gating the contents of ACCU1 and/or ACCU1-L with a word or double word according to the appropriate function. The word or double word is either specified in the instruction as an address or is in ACCU2. The result is in ACCU1 and/or ACCU1-L.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
AW		AND ACCU2-L	1	0.1	0.06	0.04	0.03
AW	W#16#p	AND 16-bit constant	2	0.125	0.075	0.05	0.042
OW		OR ACCU2-L	1	0.1	0.06	0.04	0.03
OW	W#16#p	OR 16-bit constant	2	0.125	0.075	0.05	0.042
XOW		EXCLUSIVE OR ACCU2-L	1	0.1	0.06	0.04	0.03
XOW	W#16#p	EXKLUSIV-ODER EXCLUSIVE OR 16-bit constant	2	0.125	0.075	0.05	0.042

Status word for: **UW, OW, XOW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	ja	0	0	–	–	–	–	–

Word Logic Instructions with the Contents of Accumulator 1, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
AD		AND ACCU2	1	0.1	0.6	0.04	0.3
AD	DW#16#p	AND 32-bit constant	3	0.185	0.112	0.075	0.062
OD		OR ACCU2	1	0.1	0.06	0.04	0.3
OD	DW#16#p	OR 32-bit constant	3	0.185	0.112	0.075	0.062
XOD		EXCLUSIVE OR ACCU2	1	0.1	0.06	0.04	0.03
XOD	DW#16#p	EXCLUSIVE OR 32-bit constant	3	0.185	0.112	0.075	0.062

Status word for: **UD, OD, XOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Evaluating Conditions Using AND, OR and EXCLUSIVE OR

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RL from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the $\overline{FC}$ bit is set to zero.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN O/ON X/XN	==0	AND/AND NOT OR/OR-NOT EXCLUSIVE OR/ EXCLUSIVE-OR-NOT Result=0 (A1=0 and A0=0)	1	0.1	0.06	0.04	0.03
	>0	Result>0 (CC1=1 and CC0=0)	1	0.1	0.06	0.04	0.03
	<0	Result<0 (CC1=0 and CC0=1)	1	0.1	0.06	0.04	0.03
	<>0	Result≠0 ((CC1=0 and CC0=1) or (CC1=1 and CC0=0))	1	0.1	0.06	0.04	0.03

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN O/ON X/XN	>=0	Result>=0 ((CC1=1 and CC0=0) or (CC1=0 and CC0=0))	1	0.1	0.06	0.04	0.03
	<=0	Result<=0 ((CC1=0 and CC0=1) or (CC1=0 and CC0=0))	1	0.1	0.06	0.04	0.03

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN O/ON X/XN	UO	AND/AND-NOT OR/OR-NOT EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT Unordered math instruction (CC1=1 and CC0=1)	1	0.1	0.06	0.04	0.03
	OS	AND OS=1	1	0.1	0.06	0.04	0.03
	BR	AND BR=1	1	0.1	0.06	0.04	0.03
	OV	AND OV=1	1	0.1	0.06	0.04	0.03

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	Yes	Yes	Yes	Yes	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Edge-Triggered Instructions

The current RLO is compared with the status of the instruction or “edge bit memory”. FP detects a change from “0” to “1”; FN detects a change from “1” to “0”.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
FP/FN	I/Q a.b	The positive/negative edge is indicated by RLO = 1. The bit addressed in the instruction is the auxiliary edge bit memory.	2	0.2	0.12	0.08	0.06
	M a.b		2	0.2	0.12	0.08	0.06
	L a.b1)		2	0.2	0.12	0.08	0.06
	DBX a.b		2	0.3	0.18	0.12	0.12
	DIX a.b		2	0.3	0.18	0.12	0.12
	c [d]		2	0,2+/0,3+	0,12+/0,18+	0,08+/0,12+	0,06+/0,12+
	c [AR1,m] 2)		2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	c [AR2,m] 2)		2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	[AR1,m] 2)		2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	[AR2,m] 2)		2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	Parameter 2)		2	0,6/0,7	0,36/0,42	0,24/0,28	0,21/0,27

Status word for: **FP, FN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)
1) Unnecessary if the bit being monitored is in the process image (local data of a block are only valid while the block is running).
2) I, Q, M, L /DB, DI

Setting/Resetting Bit Addresses

Assigning the value “1” or “0” to the addressed instruction when RLO = 1. The instructions can be dependent on the MCR (see page 97).

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
S		Set addressed bit to “1”					
R		Set addressed bit to “0”					
	I/Q a.b	Input/output	1[1]/2	0.2	0.12	0.08	0.06
	M a.b	Bit memory	1[2]/2	0.2	0.12	0.08	0.06
	L a.b	Local data bit	2	0.2	0.12	0.08	0.06
	DBX a.b	Data bit	2	0.3	0.18	0.12	0.12
	DIX a.b	Instance data bit	2	0.3	0.18	0.12	0.12
	c [d]	Memory-indirect, area-internal [3]	2	0,2+/0,3+	0,12+/0,18+	0,08+/0,12+	0,06+/0,12+
	c [AR1,m]	Register-indirect, area-internal (AR1) [3]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	c [AR2,m]	Register-indirect, area-internal (AR2) [3]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	[AR1,m]	Area-crossing (AR1) [3]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	[AR2,m]	Area-crossing (AR2) [3]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	Parameter	Via parameter	2	0,6/0,7	0,36/0,42	0,24/0,28	0,21/0,27

Status word for: **S, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) With direct instruction addressing; Address area 0 to 255
3) I, Q, M, L / DB, DI

Setting/Resetting Bit Addresses, continued

The RLO is written to the address of the instruction. The instructions can be dependent on the MCR (see page 97).

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
=		Assign RLO					
	I/Q a.b	To input/output	1[1)]/2	0.2	0.12	0.08	0.06
	M a.b	To bit memory	1[2)]/2	0.2	0.12	0.08	0.06
	L a.b	To local data bit	2	0.2	0.12	0.08	0.06
	DBX a.b	To data bit	2	0.3	0.18	0.12	0.12
	DIX a.b	To instance data bit	2	0.3	0.18	0.12	0.12
	c [d]	Memory-indirect, area-internal [3)]	2	0,2+/0,3+	0,12+/0,18+	0,08+/0,12+	0,06+/0,12+
	c [AR1,m]	Register-indirect, area-internal (AR1) [3)]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	c [AR2,m]	Register-indirect, area-internal (AR2) [3)]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	[AR1,m]	Area-crossing (AR1) [3)]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	[AR2,m]	Area-crossing (AR2) [3)]	2	0,2/0,3	0,12/0,18	0,08/0,12	0,06/0,12
	Parameter	Via parameter [3)]	2	0,6/0,7	0,36/0,42	0,24/0,28	0,21/0,27

Status word for: =	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) With direct instruction addressing; Address area 0 to 255
3)I, Q, M, L / DB, DI

Instructions Directly Affecting the RLO

The following instructions have a direct effect on the RLO.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
CLR		Set RLO to “0”	1	0.1	0.06	0.04	0.03

Status word for: **CLR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	0	0	0

SET		Set RLO to “1”	1	0.1	0.06	0.04	0.03

Status word for: **SET**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	1	0

NOT		Negate RLO	1	0.1	0.06	0.04	0.03

Status word for: **NOT**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	–
Instruction affects:	–	–	–	–	–	–	1	Yes	–

SAVE		Save RLO to the BR bit	1	0.1	0.06	0.04	0.03

Status word for: **SAVE**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	Yes	–	–	–	–	–	–	–	–

Timer Instructions

Starting or resetting a timer. The time value must be in ACCU1-L. The instructions are triggered by an edge transition in the RLO; that is, when the status of the RLO has changed between two calls.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
SP	T f T [e]	Start timer as pulse on edge change from “0” to “1”	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21
SE	T f T [e]	Start timer as extended pulse on edge change from “0” to “1”	1[1)]/2	0.2 0.2+	0.12 0.2+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21
SD	T f T [e]	Start timer as ON delay on edge change from “0” to “1”	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21

Status word for **SP, SE, SD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Timer Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
SS	T f T [e]	Start timer as retentive ON delay on edge change from “0” to “1”	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21
SF	T f T [e]	Start timer as OFF delay on edge change from “0” to “1”	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21

Status word for **SS, SF**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

Timer Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
FR	T f T [e]	Enable timer for restarting on edge change from “0” to “1” (reset edge bit memory for starting timer)	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21
R	T f T [e]	Reset timer	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Timer para.		2	0.6	0.36	0.24	0.21

Status word for: **FR, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Counter Instructions

The count value must be in ACCU1-L in the form of a BCD number (0 - 999).

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
S	C f C [e]	Presetting of counter on edge change from “0” to “1”	1[1)]/2	0.2 0.4+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Counter para.		2	0.6	0.36	0.24	0.21
R	C f C [e]	Reset counter to “0” when RLO = “1”	1[1)]/2	0.2 0.4+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Counter para.		2	0.6	0.36	0.24	0.21
CU	C f C [e]	Increment counter by 1 on edge change from “0” to “1”	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Counter para.		2	0.6	0.36	0.24	0.21

Status word for: **S, R, CU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Counter No.: 0 to 255

Counter Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
CD	C f C [e]	Decrement counter by 1 on edge change from “0” to “1”	1[1)]/2	0.2 0..2+	0.12 0.2+	0.08 0.08+	0.06 0.06+
	Counter para.		2	0.6	0.36	0.24	0.21
FR	C f C [e]	Enable counter on edge change from “0” to “1” (reset edge bit memory for up and down counting and setting the counter)	1[1)]/2	0.2 0.2+	0.12 0.12+	0.08 0.08+	0.06 0.06+
	Counter para.		2	0.6	0.36	0.24	0.21

Status word for: **CD, FR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Counter No.: 0 to 255

Load Instructions

Loading address identifiers into ACCU1. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	IB a	Input byte	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	QB a	Output byte	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	PIB a	Peripheral input byte [2)]	2	0.125	0.075	0.05	0.042
	MB a	Bit memory byte	1[3)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	LB a	Local data byte	2	0.125	0.075	0.05	0.042
	DBB a	Data byte	2	0.2	0.12	0.08	0.09
	DIB a	Instance data byte	2	0.2	0.12	0.08	0.09
		... into ACCU1					
	g [d]	Memory-indirect, area-internal [4)]	2	0.1+/0.2+	0.06+/0.12+	0.04+/0.08+	0.03+/0.09+
	g [AR1,m]	Register-indirect, area-internal (AR1) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,42/0,09
	g [AR2,m]	Register-indirect, area-internal (AR2) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,42/0,09
	B[AR1,m]	Area-crossing (AR1) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,42/0,09
	B[AR2,m]	Area-crossing (AR2) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,42/0,09
	Parameter	Via parameter [4)]	2	0,525/0,6	0,315/0,36	0,21/0,24	0,57/0,24

\+ Plus time required for loading the address of the instruction (see page 20)

1) With indirect instruction addressing; Address area 0 to 127

2) The following peripheral acknowledgement time must be observed with CPU 414-4H: solo 33 µs, redundant 77 µs with CPU 417-4H: solo 21 µs, redundant 45 µs

3) With direct instruction addressing; Address area 0 to 255

4) I, Q, P, M, L / DB, DI

Load Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	IW a	Input word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	QW	Output word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	PIW a	Peripheral input word [2)]	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	MW a	Bit memory word	1[3)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	LW a	Local data word	2	0.125	0.075	0.05	0.042
	DBW a	Data word	2	0.2	0.12	0.08	0.09
	DIW a	Instance data word	2	0.2	0.12	0.08	0.09
		... into ACCU1-L					
	h [d]	Memory-indirect, area-internal[4)]	2	0.1+/0.2+	0.06+/0.12+	0.04+/0.08+	0.03+/0.09+
	h [AR1,m]	Register-indirect, area-internal (AR1) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	h [AR2,m]	Register-indirect, area-internal (AR2) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	W[AR1,m]	Area-crossing (AR1) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	W[AR2,m]	Area-crossing (AR2) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	Parameter	Via parameter [4)]	2	0,525/0,6	0,315/0,36	0,21/0,24	0,192/0,24

\+ Plus time required for loading the address of the instruction (see page 20)

1) With indirect instruction addressing; Address area 0 to 127

2) The following peripheral acknowledgement time must be observed with CPU 414-4H: solo 36 µs, redundant 80 µs
with CPU 417-4H: solo 23 µs, redundant 47 µs

3) With direct instruction addressing; Address area 0 to 255

4) I, Q, P, M, L / DB, DI

Load Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	IDa	Input double word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	QD a	Output double word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	PID a	Peripheral input double word [2)]	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	MD a	Bit memory double word	1[3)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	LD a	Local data double word	2	0.125	0.075	0.05	0.042
	DBD a	Data double word	2	0.2	0.12	0.08	0.09
	DID a	Instance data double word	2	0.2	0.12	0.08	0.09
		... in ACCU1					
	i [d]	Memory-indirect, area internal [4)]	2	0.1+/0.2+	0.06+/0.12+	0.04+/0.08+	0.03+/0.09+
	i [AR1,m]	Register-ind., area internal (AR1) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	i [AR2,m]	Register-ind., area internal (AR2) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	D[AR1,m]	Area-crossing (AR1) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	D[AR2,m]	Area-crossing (AR2) [4)]	2	0,125/0,2	0,075/0,12	0,05/0,08	0,042/0,09
	Parameter	Via parameter [4)]	2	0,525/0,6	0,315/0,36	0,21/0,24	0,192/0,24

\+ Plus time required for loading the address of the instruction (see page 20)

1) With indirect instruction addressing; Address area 0 to 127

2) The following peripheral acknowledgement time must be observed with CPU 414-4H: solo 40 µs, redundant 84 µs with CPU 417-4H: solo 26 µs, redundant 50 µs

3) With direct instruction addressing; Address area 0 to 255

4) I, Q, P, M, L / DB, DI

Load Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	k8	8-bit constant into ACCU1-LL	2	0.125	0.075	0.05	0.042
	k16	16-bit constant into ACCU1-L	2	0.125	0.075	0.05	0.042
	k32	32-bit constant into ACCU1	3	0.185	0.112	0.075	0.062
	Parameter	Load constant into ACCU1 (addressed via parameter)	2	0,3+	0.18+	0.12+	0.12+
L	2#n	Load 16-bit binary constant into ACCU1-L	2	0.125	0.075	0.05	0.042
		Load 32-bit binary constant into ACCU1	3	0.185	0.112	0.075	0.062
	B#16#p	Load 8-bit-hexadecimal constant into ACCU1-L	1	0.1	0.06	0.04	0.03
L	W#16#p	Load 16-bit hexadecimal constant into ACCU1-L	2	0.125	0.075	0.05	0.042
	DW#16#p	Load 32-bit hexadecimal constant into ACCU1	3	0.185	0.112	0.075	0.065

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L	'x'	Load 1 character	2	0.125	0.075	0.05	0.042
	'xx'	Load 2 characters	2	0.125	0.075	0.05	0.042
	'xxx'	Load 3 characters	3	0.185	0.112	0.075	0.062
	'xxxx'	Load 4 characters	3	0.185	0.112	0.075	0.062
L	D# time value	Load IEC date	3	0.185	0.112	0.075	0.062
L	S5T# time value	Load S7 time constant (16 bits)	2	0.125	0.075	0.05	0.042
L	TOD# time value	Load IEC time constant	3	0.185	0.112	0.075	0.062
L	T# time value	Load 16-bit time constant	2	0.125	0.075	0.05	0.042
		Load 32-bit time constant	3	0.185	0.112	0.075	0.062
L	C# count value	Load counter constant (BCD code)	2	0.125	0.075	0.05	0.042
L	B# (b1, b2)	Load constant as byte (b1, b2)	2	0.125	0.075	0.05	0.042
	B# (b1, b2, b3, b4)	Load constant as 4 bytes (b1, b2, b3, b4)	3	0.185	0.112	0.075	0.062

Load Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L	P# bit pointer	Load bit pointer	3	0.185	0.112	0.075	0.062
L	L# integer	Load 32-bit integer constant	3	0.185	0.112	0.075	0.062
L	Real number	Load floating-point number	3	0.185	0.112	0.075	0.062

Load Instructions for Timers and Counters

Loading a time value or count value into ACCU1. The contents of ACCU1 are first saved to ACCU2. The bits of the status word are not affected.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L	T f T (e)	Load time value	1[1)]/2 2	0.1/0.125 0.1+	0.06/0.075 0.06+	0.04/0.05 0.04+	0.03/0.042 0.03+
	Timer para.	Load time value (addressed via parameter)	2	0.5	0.3	0.2	0.18
L	C f C (e)	Load count value	1[1)]/2 2	0.1/0.125 0.1+	0.06/0.075 0.06+	0.04/0.05 0.04+	0.03/0.042 0.03+
	Counter para.	Load count value (addressed via parameter)	2	0.5	0.3	0.2	0.18
LC	T f T (e)	Load time value in BCD	1[1)]/2 2	0.3 0.3+	0.18 0.18+	0.12 0.12+	0.09 0.09+
	Timer para.	Load time value in BCD (addressed via parameter)	2	0.7	0.42	0.28	0.24
LC	C f C (e)	Load count value in BCD	1[1)]/2 2	0.3 0.3+	0.18 0.18+	0.12 0.12+	0.09 0.09+
	Counter para.	Load count value in BCD (addressed via parameter)	2	0.7	0.42	0.28	0.24

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Timer/counter No.: 0 to 255

Transfer Instructions

Transferring the contents of ACCU1 to the addressed operand. Note that some instructions are affected by the MCR (see page 97). The status word is not affected.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
T		Transfer contents of ACCU1-LL to ...					
	IB a	input byte	1[1])/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	QB a	output byte	1[1])/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	PQB a	peripheral output byte[2)]	2	0.125	0.075	0.05	0.042
	MB a	bit memory byte	1[3])/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	LB a	local data byte	2	0.125	0.075	0.05	0.042
	DBB a	data byte	2	0.335	0.075	0.05	0.042
	DIB a	instance data byte	2	0.335	0.075	0.05	0.042
	g [d]	Memory-indirect, area internal	2	0.1+	0.06+	0.04+	0.03+
	g [AR1,m]	Register-ind., area internal (AR1)	2	0.125	0.075	0.05	0.042
	g [AR2,m]	Register-ind., area internal (AR2)	2	0.125	0.075	0.05	0.042
	B[AR1,m]	Area-crossing (AR1)	2	0.125	0.075	0.05	0.042
	B[AR2,m]	Area-crossing (AR2)	2	0.125	0.075	0.05	0.042
	Parameter	Via parameter	2	0.525	0.315	0.21	0.192

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; Address area 0 to 127

2) The following peripheral acknowledgement time must be observed with CPU 414-4H: solo 32 µs, redundant 77 µs with CPU 417-4H: solo 20 µs, redundant 46 µs

3) With direct instruction addressing; Address area 0 to 255

Transfer Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
T		Transfer contents of ACCU1-L to ...					
		input word					
	IW a	output word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	QW a	peripheral output word[2)]	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	PQW a		1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	MW a	bit memory word	1[3)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	LW a	local data word	2	0.125	0.075	0.05	0.042
	DBW a	data word	2	0.335	0.075	0.05	0.042
	DIW a	instance data word	2	0.335	0.075	0.05	0.042
	h [d]	Memory-indirect, area internal	2	0.1+	0.06+	0.04+	0.03+
	h [AR1,m]	Register-ind., area internal (AR1)	2	0.125	0.075	0.05	0.042
	h [AR2,m]	Register-ind., area internal (AR2)	2	0.125	0.075	0.05	0.042
	W[AR1,m]	Area-crossing (AR1)	2	0.125	0.075	0.05	0.042
	W[AR2,m]	Area-crossing (AR2)	2	0.125	0.075	0.05	0.042
	Parameter	Via parameter	2	0.525	0.315	0.21	0.192

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; Address area 0 to 127

2) The following peripheral acknowledgement time must be observed with CPU 414-4H: solo 35 µs, redundant 80 µs with CPU 417-4H: solo 22 µs, redundant 48 µs

3) With direct instruction addressing; Address area 0 to 255

Transfer Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
T		Transfer contents of ACCU1 to ...					
	ED a	Input double word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	AD a	Output double word	1[1)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	PAD a	periph. output double word [2)]	2	0.125	0.075	0.05	0.042
	MD a	Bit memory double word	1[3)]/2	0.1/0.125	0.06/0.075	0.04/0.05	0.03/0.042
	LD a	Local data double word	2	0.125	0.075	0.05	0.042
	DBD a	Data double word	2	0.11	0.075	0.05	0.042
	DID a	Instance data double word	2	0.11	0.075	0.05	0.042
T	i [d]	Memory-indirect, area internal	2	0.1+	0.06+	0.04+	0.03+
	i [AR1,m]	Register-ind., area internal (AR1)	2	0.125	0.075	0.05	0.042
	i [AR2,m]	Register-ind., area internal (AR2)	2	0.125	0.075	0.05	0.042
	D[AR1,m]	Area-crossing (AR1)	2	0.125	0.075	0.05	0.042
	D[AR2,m]	Area-crossing (AR2)	2	0.125	0.075	0.05	0.042
	Parameter	Via parameter	2	0.525	0.315	0.21	0.192

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) The following peripheral acknowledgement time must be observed with CPU 414-4H: solo 39 µs, redundant 48 µs with CPU 417-4H: solo 25 µs, redundant 51 µs
3) With direct instruction addressing; Address area 0 to 255

Load and Transfer Instructions for Address Registers

Loading a double word from a memory area or register into address register 1 (AR1) or address register 2 (AR2). The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
LAR1		Load contents from ...					
	–	ACCU1	1	0.2	0.12	0.08	0.06
	AR2	Address register 2	1	0.2	0.12	0.08	0.06
	DBD a	Data double word	2	0.3	0.18	0.12	0.12
	DID a	Instance data double word	2	0.3	0.18	0.12	0.12
	m	32-bit constant as pointer	3	0.2	0.12	0.08	0.062
	LD a	Local data double word	2	0.2	0.12	0.08	006
	MD a	Bit memory double word	2	0.2	0.12	0.08	006
		... into AR1					
LAR2		Load contents from ...					
	–	ACCU1	1	0.2	0.12	0.08	0.06
	DBD a	Data double word	2	0.3	0.18	0.12	0.12
	DID a	Instance data double word	2	0.3	0.18	0.12	0.12
	m	32-bit constant as pointer	3	0.2	0.12	0.08	0.062
	LD a	Local data double word	2	0.2	0.12	0.08	0.06
	MD a	Bit memory double word	2	0.2	0.12	0.08	0.06
		... into AR2					

Load and Transfer Instructions forAddress Registers, continued

Transferring a double word from address register 1 (AR1) or address register 2 (AR2) to a memory area or register. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
TAR1		Transfer contents from AR1 in ...					
	–	ACCU1	1	0.1	0.06	0.04	0.03
	AR2	Address register 2	1	0.2	0.12	0.08	0.06
	DBD a	Data double word	2	0.125	0.075	0.05	0.042
	DID a	Instance data double word	2	0.125	0.075	0.05	0.042
	LD a	Local data double word	2	0.125	0.075	0.05	0.042
	MD a	Bit memory double word	2	0.125	0.075	0.05	0.042
TAR2		Transfer contents from AR2 in ...					
	–	ACCU1	1	0.1	0.06	0.04	0.03
	DBD a	Data double word	2	0.125	0.075	0.05	0.042
	DID a	Instance data double word	2	0.125	0.075	0.05	0.042
	LD a	Local data double word	2	0.125	0.075	0.05	0.042
	MD a	Bit memory double word	2	0.125	0.075	0.05	0.042
CAR		Exchange the contents of AR1 and AR2	1	0.2	0.12	0.08	0.06

Load and Transfer Instructions for the Status Word

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L	STW	Load status word into ACCU1		0.1	0.06	0.04	0.3

Status word for: **L STW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction affects:	–	–	–	–	–	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
T	STW	Transfer ACCU1 (bits 0 to 8) to the status word		0.1	0.06	0.04	0.03

Status word for: **T STW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Load Instructions for DB Number and DB Length

Loading the number/length of a data block into ACCU1. The old contents of ACCU1 are saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
L	DBNO	Load number of data block	1	0.1	0.06	0.04	0.03
L	DINO	Load number of instance data block	1	0.1	0.06	0.04	0.03
L	DBLG	Load length of data block into byte	1	0.1	0.06	0.04	0.03
L	DILG	Load length of instance data block into byte	1	0.1	0.06	0.04	0.03

Integer Math (16 Bits)

Math instructions on two 16-bit words. The result is written to ACCU1 and/or ACCU1-L. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
+I		Add 2 integers (16 bits) (ACCU1-L)=(ACCU1-L)+(ACCU2-L)	1	0.1	0.06	0.04	0.03
–I		Subtract 1 integer from another (16 bits) (ACCU1-L)=(ACCU2-L)-(ACCU1-L)	1	0.1	0.06	0.04	0.03

Status word for: **+I, –I,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
*I		Multiply 1 integer by another (16 bits) (ACCU1)=(ACCU2-L)*(ACCU1-L)	1	0.1	0.06	0.04	0.03
/I		Divide 1 integer by another (16 bits) (ACCU1-L)=(ACCU2-L):(ACCU1-L) The remainder is in ACCU1-H	1	0.1	0.24	0.16	0.12

Status word for: ***I, /I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Integer Math (32 Bits)

Math instructions on two 32-bit words. The result is written to ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
+D		Add 2 integers (32-bit) (ACCU1)=(ACCU2)+(ACCU1)	1	0.1	0.06	0.04	0.03
–D		Subtract 2 integer from another (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	0.1	0.06	0.04	0.03
*D		Multiply 2 integer by another (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	0.1	0.06	0.04	0.03

Status word for: **+D, –D,*D, /D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
/D		Divide 2 integer by another (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	0.6	0.36	0.24	0.18
MOD		Divide 2 integer by another (32 bits) and load the remainder into ACCU1: (ACCU1)=remainder of [(ACCU2):(ACCU1)]	1	0.6	0.36	0.24	0.18

Status word for: **/D, MOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Floating-Point Math (32 Bits)

The result of the math instruction is in ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
+R		Add 2 real numbers (32 bits) (ACCU1)=(ACCU2)+(ACCU1)	1	0.4	0.24	0.16	0.12
–R		Subtract 1 real number from another (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	0.4	0.24	0.16	0.12
*R		Multiply 1 real number by another (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	0.2	0.12	0.08	0.06
/R		Divide 1 real number by another (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	0.7	0.42	0.28	0.21

Status word for: **+R, –R, *R, /R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Floating-Point Math (32 Bits), continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
NEGR		Negate the real number in ACCU1	1	0.1	0.06	0.04	0.03
ABS		Form the absolute value of the real number in ACCU1	1	0.1	0.06	0.04	0.03

Status word for: **NEGR, ABS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Square Root and Square Instructions (32 Bits)

The result of the instruction is in ACCU1. The SQRT instruction can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
SQRT		Calculate the square root of a real number in ACCU1	1	1.7	1.02	0.68	0.51
SQR		Form the square of the real number in ACCU1	1	0.2	0.12	0.08	0.06

Status word for: **SQRT, SQR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Logarithmic Function (32 Bits)

The result of the logarithmic function is in ACCU1. The instructions can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
LN		Form the natural logarithm of a real number in ACCU1	1	20	13	9	7
EXP		Calculate the exponential value of a real number in ACCU1 to the base e (= 2.71828)	1	21	15	10	8

Status word for: **LN, EXP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Trigonometrical Functions (32 Bits)

The result of the instruction is in ACCU1. The instructions can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
SIN		Calculate the sine of a real number	1	6,6	3,96	2,64	1,98
ASIN		Calculate the arcsine of a real number	1	33 – 38	22 – 24	15 – 17	13
COS		Calculate the cosine of a real number	1	6,6	3,96	2,64	1,98
ACOS		Calculate the arccosine of a real number	1	36 – 40	25 – 27	16 – 18	12 – 14
TAN		Calculate the tangent of a real number	1	20	14	10	7
ATAN		Calculate the arctangent of a real number	1	14 – 18	10 – 13	6 – 9	5 – 7

Status word for: **SIN, ASIN, COS, ACOS, TAN, ATAN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Adding Constants

Adding integer constants and storing the result in ACCU1. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
+	i8	Add an 8-bit integer constant	1	0.1	0.06	0.04	0.03
+	i16	Add a 16-bit integer constant	2	0.125	0.075	0.05	0.042
+	i32	Add a 32-bit integer constant	3	0.185	0.11	0.075	0.062

Adding Using Address Registers

Adding a 16-bit integer to the contents of the address register. The value is either specified as an address in the instruction or is in ACCU1-L. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
+AR1		Add the contents of ACCU1-L to those of AR1	1	0.2	0.12	0.08	0.06
+AR1	m (0 to 4095)	Add a pointer constant to the contents of AR1	2	0.2	0.12	0.08	0.06
+AR2		Add the contents of ACCU1-L to those of AR2	1	0.2	0.12	0.08	0.06
+AR2	m (0 to 4095)	Add pointer constant to the contents of AR2	2	0.2	0.12	0.08	0.06

Comparison Instructions (16-Bit Integers)

Comparing the 16-bit integers in ACCU1-L and ACCU2-L. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
==I		ACCU2-L=ACCU1-L	1	0.1	0.06	0.04	0.03
<>I		ACCU2-L ≠ ACCU1-L	1	0.1	0.06	0.04	0.03
<I		ACCU2-L<ACCU1-L	1	0.1	0.06	0.04	0.03
<=I		ACCU2-L<=ACCU1-L	1	0.1	0.06	0.04	0.03
>I		ACCU2-L>ACCU1-L	1	0.1	0.06	0.04	0.03
>=I		ACCU2-L>=ACCU1-L	1	0.1	0.06	0.04	0.03

Status word for: **==I, <>I, <I, <=I, >I, >=I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	0	–	0	Yes	Yes	1

Comparison Instructions (32-Bit Integers)

Comparing the 32-bit integers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
==D		ACCU2=ACCU1	1	0.1	0.06	0.04	0.03
<>D		ACCU2≠ACCU1	1	0.1	0.06	0.04	0.03
<D		ACCU2<ACCU1	1	0.1	0.06	0.04	0.03
<=D		ACCU2<=ACCU1	1	0.1	0.06	0.04	0.03
>D		ACCU2>ACCU1	1	0.1	0.06	0.04	0.03
>=D		ACCU2>=ACCU1	1	0.1	0.06	0.04	0.03

Status word for: **==D,< >D, <D, <=D, >D, >=D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	0	–	0	Yes	Yes	1

Comparison Instructions (32-Bit Real Numbers)

Comparing the 32-bit real numbers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
==R		ACCU2=ACCU1	1	0.1	0.06	0.04	0.03
<>R		ACCU2≠ACCU1	1	0.1	0.06	0.04	0.03
<R		ACCU2<ACCU1	1	0.1	0.06	0.04	0.03
<=R		ACCU2<=ACCU1	1	0.1	0.06	0.04	0.03
>R		ACCU2>ACCU1	1	0.1	0.06	0.04	0.03
>=R		ACCU2>=ACCU1	1	0.1	0.06	0.04	0.03

Status word for: **==R, <>R, <R, <=R, >R, >=R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	0	Yes	Yes	1

Shift Instructions

Shifting the contents of ACCU1 and ACCU1-L to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC 1.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
SLW[1)]		Shift the contents of ACCU1-L to the left. Positions that become free are provided with zeros.	1	0.1	0.06	0.04	0.03
SLW	0 ... 15						
SLD		Shift the contents of ACCU1 to the left. Positions that become free are provided with zeros.	1	0.1	0.06	0.04	0.03
SLD	0 ... 32						
SRW[1)]		Shift the contents of ACCU1-L to the right. Positions that become free are provided with zeros.	1	0.1	0.06	0.04	0.03
SRW	0 ... 15						

Status word for: **SLW, SLD, SRW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

1) No. of places shifted: 0 to 16

Shift Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
SRD		Shift the contents of ACCU1 to the right. Positions that become free are provided with zeros.	1	0.1	0.06	0.04	0.03
SRD	0 ... 32						
SSI[1)]		Shift the contents of ACCU1-L with sign to the right. Positions that become free are provided with with the sign (bit 15).	1	0.1	0.06	0.04	0.03
SSI	0 ... 15						
SSD		Shift the contents of ACCU1 with sign to the right. Positions that become free are provided with with the sign (bit 31).	1	0.1	0.06	0.04	0.03
SSD	0 ... 32						

Status word for: **SRD,SSI, SSD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

1) No. of places shifted: 0 to 16

Rotate Instructions

Rotate the contents of ACCU1 to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC1.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
RLD		Rotate the contents of ACCU1 to the left	1	0.1	0.06	0.04	0.03
RLD	0 ... 32						
RRD		Rotate the contents of ACCU1 to the right	1	0.1	0.06	0.04	0.03
RRD	0 ... 32						

Status word for: **RLD, RRD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Rotate Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
RLDA		Rotate the contents of ACCU1 one bit position to the left through condition code bit CC 1		0.1	0.06	0.04	0.03
RRDA		Rotate the contents of ACCU1 one bit position to the right through condition code bit CC 1		0.1	0.06	0.04	0.03

Status word for: **RLDA, RRDA**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Accumulator Transfer Instructions, Incrementing and Decrementing

The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
CAW		Reverse the order of the bytes in ACCU1-L.	1	0.1	0.06	0.04	0.03
CAD		Reverse the order of the bytes in ACCU1.	1	0.1	0.06	0.04	0.03
TAK		Swap the contents of ACCU1 and ACCU2	1	0.1	0.06	0.04	0.03
ENT		The contents of ACCU2 and ACCU3 are transferred to ACCU3 and ACCU4.	1	0.1	0.06	0.04	0.03
LEAVE		The contents of ACCU3 and ACCU4 are transferred to ACCU2 and ACCU3.	1	0.1	0.06	0.04	0.03
PUSH		The contents of ACCU1, ACCU2 and ACCU3 are transferred to ACCU2, ACCU3 and ACCU4	1	0.1	0.06	0.04	0.03
POP		The contents of ACCU2, ACCU3 and ACCU4 are transferred to ACCU1, ACCU2 and ACCU3	1	0.1	0.06	0.04	0.03

Accumulator Transfer Instructions, Incrementing and Decrementing, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
INC	k8	Increment ACCU1-LL	1	0.1	0.06	0.04	0.03
DEC	k8	Decrement ACCU1-LL	1	0.1	0.06	0.04	0.03

Program Display and Null Operation Instructions

The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
BLD	k8	Program display instruction: Is treated by the CPU as a null operation instruction.	1	0.1	0.06	0.04	0.03
NOP	0 1	Null operation instruction	1	0.1	0.06	0.04	0.03

Data Type Conversion Instructions

The results of the conversion are in ACCU1.

Instruction	Addr. ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
BTI		Convert contents of ACCU1-L from BCD (0 to +/- 999) to integer (16 bits) (**B**CD **T**o **I**nt)	1	0.1	0.06	0.04	0.03
BTD		Convert contents of ACCU1 from BCD (0 to +/-9 999 999) to double integer (32 bits) (**B**CD **T**o **D**oubleint)	1	0.1	0.06	0.04	0.03
DTR		Convert contents of ACCU1 from double integer (32 bits) to real number (32 bits) (**D**oubleint **T**o **R**eal)	1	0.3	0.18	0.12	0.09
ITD		Convert contents of ACCU1 from integer (16 bits) to double integer (32 bits) (**I**nt **T**o **D**oubleint)	1	0.3	0.06	0.04	0.03

Status word for: **BTI, BTD, DTR, ITD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Data Type Conversion Instructions, continued

Instruction	Addr. ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
ITB		Convert contents of ACCU1-L from integer (16 bits) to BCD from 0 to +/- 999 (**I**nt **T**o **B**CD)	1	0.1	0.06	0.04	0.03
DTB		Convert contents of ACCU1 from double integer (32 bits) to BCD from 0 to +/- 9 999 999 (**D**oubleint **T**o **B**CD)	1	0.2	0.12	0.08	0.06

Status word for: **ITB, DTB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	Yes	Yes	–	–	–	–

Data Type Conversion Instructions, continued

The real number to be converted is in ACCU1.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
RND+		Convert a real number into a 32-bit integer. The number is rounded up to the next whole number.	1	0.4	0.24	0.16	0.12
RND		Convert a real number into a 32-bit integer.	1	0.4	0.24	0.16	0.12
RND-		Convert a real number into a 32-bit integer. The number is rounded down to the next whole number.	1	0.4	0.24	0.16	0.12
TRUNC		Convert a real number into a 32-bit integer. The places after the decimal point are truncated.	1	0.4	0.24	0.16	0.12

Status word for: **RND, RND-, RND+, TRUNC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	Yes	Yes	–	–	–	–

Forming the Ones and Twos Complements

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
INVI		Form the ones complement of ACCU1-L	1	0.1	0.06	0.04	0.03
INVD		Form the ones complement of ACCU1	1	0.1	0.06	0.04	0.03

Status word for: **INVI, INVD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

NEGI		Form the twos complement of ACCU1-L (integer)	1	0.1	0.06	0.04	0.03
NEGD		Form the twos complement of ACCU1 (double integer)	1	0.1	0.06	0.04	0.03

Status word for: **NEGI, NEGD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Block Call Instructions

The runtimes of the System Functions are specified in the chapter entitled “System Functions” as of page 106.

The information on the status word only relates to the block call itself and not to the commands called in this block.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
CALL	FB q, DB q	Unconditional call of an FB, with parameter transfer	15/17[1)]	4.0 [2)]	2.4 [2)]	1.6 [2)]	1.26 [2)]
CALL	SFB q, DB q	Unconditional call of an SFB, with parameter transfer	16/17[1)]	4.0 [2)]	2.4 [2)]	1.6 [2)]	1.26 [2)]
CALL	FC q	Unconditional call of a function, with parameter transfer	7/8[1)]	3.2 [2)]	1.92 [2)]	1.28 [2)]	1.02 [2)]
CALL	SFC q	Unconditional call of an SFC, with parameter transfer	8	3.2 [2)]	1.92 [2)]	1.28 [2)]	1.02 [2)]

Status word for: **CALL**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

1) The instruction length depends on the block number from (0...255 or more)
2) Plus time required for supplying parameters

Block Call Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
UC	FB q	Unconditional call of blocks,	1[1)]/2	2.2	1.32	0.88	0.72
	FC q	without parameter transfer		2.2	1.32	0.88	0.72
	FB [e]	Memory-indirect FB call	2	2.2+	1.32+	0.88+	0.72+
	FC [e]	Memory-indirect FC call	2	2.2+	1.32+	0.88+	0.72+
	Parameter	FB/FC call via parameter	2	2.6	1.56	1.04	0.87
CC	FB q	Conditional call of blocks, without	1[1)]/2	2.2/0.5 [3)]	1.32/0.3 [3)]	0.88/0.2 [3)]	0.72/0.18 [3)]
	FC q	parameter transfer		2.2/0.5 [3)]	1.32/0.3 [3)]	0.88/0.2 [3)]	0.72/0.18 [3)]
	FB [e]	Memory-indirect FB call	2	2.2+/0.5 [3)]	1.32+/0.3 [3)]	0.88+/0.2 [3)]	0.72+/0.18 [3)]
	FC [e]	Memory-indirect FC call	2	2.2+/0.5 [3)]	1.32+/0.3 [3)]	0.88+/0.2 [3)]	0.72+/0.18 [3)]
	Parameter	FB/FC call via parameter	2	2.6/0.5 [3)]	1.56/0.3 [3)]	1.04/0.2 [3)]	0.87/0.18 [3)]

Status word for: **UC, CC [2)]**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction (DB) addressing; Block No. 0 to 255
2) Depending on RLO, sets RLO = 1
3) If call is not executed

Block Call Instructions, continued

In-struc-tion	Ad-dress ID	Description	Length in Words	Execution Time in µs							
				CPU 412		CPU 414		CPU 416		CPU 417	
				1. open	2. - n. open 1)	1. open	2. - n. open 1)	1. open	2. - n. open 1)	1. open	2. - n. open 1)
OPN		Select a data block									
	DB q	Direct data block, DB no. 1 to 255	1	0.5	0.1	0.3	0.06	0.2	0.04	0.21	0.03
	DB q DI q	Direct data block, DB Direct instance DB	2	0.5	0.125	0.3	0.075	0.2	0.05	0.210	0.042
	DB [e]	Data block, indirect save Bit memory area M Local data area L Data block DB/DI	2	 0.7 0.7 0.8	 0.325 0.325 0.425	 0.420 0.420 0.480	 0.195 0.195 0.255	 0.280 0.280 0.320	 0.130 0.130 0.170	 0.270 0.270 0.330	 0.102 0.102 0.162
	DI [e]	Instance DB, indirect save Bit memory area M Local data area L Data block DB/DI	2	 0.7 0.7 0.8	 0.325 0.325 0.425	 0.420 0.420 0.480	 0.195 0.195 0.255	 0.280 0.280 0.320	 0.130 0.130 0.170	 0.270 0.270 0.330	 0.102 0.102 0.162
	Param.	Data block via parameters	2	0.9	0.525	0.54	0.315	0.36	0.21	0.36	0.192

Status word for: **OPN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

1) if the same DB or DI is already selected

Block End Instructions

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
BE		End block	1	4.0	2.4	1.6	1.62
BEU		End block unconditionally	1	4.0	2.4	1.6	1.62

Status word for: **BE, BEU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

BEC		End block conditionally if RLO = “1”		4.2 0.5[1)]	2.52 0.3[1)]	1.78 0.2[1)]	1.68 0.18[1)]

Status word for: **BEC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	Yes	0	1	1	0

1) If jump is not executed

Exchanging Shared Data Block and Instance Data Block

Exchanging the two current data blocks. The current shared data block becomes the current instance data block, and vice versa. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
CDB		Exchange shared data block and instance data block	1	0.2	0.12	0.08	0.06

Jump Instructions

Jumping as a function of conditions.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
JU	LABEL	Jump unconditionally	2	0.6	0.36	0.24	0.21

Status word for: **JU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

JC	LABEL	Jump if RLO = “1”	2	0.6; 0.1251)	0.36; 0.0751)	0.24; 0.051)	0.21; 0.0421)
JCN	LABEL	Jump if RLO = “0”	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)

Status word for: **JC, JCN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	1	1	0

1) If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
JCB	LABEL	Jump if RLO = “1”. Save the RLO in the BR bit	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)
JNB	LABEL	Jump if RLO = “0”. Save the RLO in the BR bit	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)

Status word for: **JCB, JNB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	Yes	–	–	–	–	0	1	1	0

JBI	LABEL	Jump if BR = “1”	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)
JNBI	LABEL	Jump if BR = “0”	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)

Status word for: **JBI, JNBI**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	–	0

1) If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
JO	LABEL	Jump on stored overflow (OV = “1”)	2	0.6; 0.125[1)]	0.36; 0.075[1)]	0.24; 0.05[1)]	0.21; 0.042[1)]

Status word for: **JO**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	Yes	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

JOS	LABEL	Jump on stored overflow (OS = “1”)	2	0.6/0.125 [1)]	0.36/0.075 [1)]	0.24/0.05 [1)]	0.21/0.042 [1)]

Status word for: **JOS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	Yes	–	–	–	–
Instruction affects:	–	–	–	–	0	–	–	–	–

[1)] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
JUO	LABEL	Jump if “unordered math instruction” (CC1=1 and CC0=1)	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)
JZ	LABEL	Jump if result = 0 (CC1=0 and CC0=0)	2	0.6; 0.125 1)	0.36; 0.075 1)	0.24; 0.05 1)	0.24; 0.05 1)
JP	LABEL	Jump if result > 0 (CC1=1 and CC0=0)	2	0.6; 0.125 1)	0.36; 0.075 1)	0.24; 0.05 1)	0.24; 0.05 1)
JM	LABEL	Jump if result < 0 (CC1=0 and CC0=1)	2	0.6; 0.125 1)	0.36; 0.075 1)	0.24; 0.05 1)	0.24; 0.05 1)
JN	LABEL	Jump if result ≠ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=1)	2	0.6; 0.125 1)	0.36; 0.075 1)	0.24; 0.05 1)	0.24; 0.05 1)

Status word for: **JUO, JZ, JP, JM, JN,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

1) If jump is not executed

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	**CPU 414**	**CPU 416**	**CPU 417**
JMZ	LABEL	Jump if result ≤ 0 (CC1=0 and CC0=1) or (CC1=0 and CC0=0)	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)
JPZ	LABEL	Jump if result ≥ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=0)	2	0.6/0.125 1)	0.36/0.075 1)	0.24/0.05 1)	0.21/0.042 1)

Status word for: **JUO, JZ, JP, JM, JN, JMZ, JPZ**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

1) If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
JL	LABEL	Jump distributor This instruction is followed by a list of jump instructions. The address identifier is a jump label to subsequent instructions in this list. ACCU1-LL contains the number of the jump instruction to be executed (max. 254). The number of the first jump instruction is 0.	2	0.7	0.42	0.28	0.24
LOOP	LABEL	Decrement ACCU1-L and jump if ACCU1-L ≠ 0 (loop programming)	2	0.6/0.125 [1]	0.36/0.075 [1]	0.24/0.05 [1]	0.21/0.042 [1]

Status word for: **JL, LOOP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

1) If jump is not executed

Instructions for the Master Control Relay (MCR)

MCR=1→MCR is deactivated
MCR=0→MCR is activated; “T” and “=” instructions write zeros to the

corresponding address identifiers if RLO = “0”; “S” and ”R” instructions leave the memory contents unchanged.

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
MCR(		Open an MCR zone. Save the RLO to the MCR stack.	1	0.1	0.06	0.04	0.03

Status word for: **MCR(**	CC1	BR	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	1	–	0

)MCR		Close an MCR zone. Pop an entry off the MCR stack.	1	0.1	0.06	0.04	0.03

Status word for: **)MCR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	–	0

Instructions for the Master Control Relay (MCR), continued

Instruction	Address ID	Description	Length in Words	Execution Time in µs			
				CPU 412	CPU 414	CPU 416	CPU 417
MCRA		Activate the MCR	1	0.1	0.06	0.04	0.03
MCRD		Deactivate the MCR	1	0.1	0.06	0.04	0.03

Status word for: **MCRA, MCRD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Oganization Blocks (OB)

A user program for the S7-400 is made up of blocks containing the statements, parameters and data for the relevant CPU. The number of blocks you can create or which are provided by the operating system is different for each of the S7-400 CPUs. You will find a detailed description of the OBs and their use in the *STEP 7 Programming Manual*.

Organization Blocks	CPU 412	CPU 414	CPU 414-4H	CPU 416	CPU 417	CPU 417-4H	Start Events (Hexadecimal Values)
Free cycle							
OB 1	x	x	x	x	x	x	1101, 1102, 1103, 1104, 1105
Time-of-day interrupts							
OB 10	x	x	x	x	x	x	1111
OB 11	x	x	x	x	x	x	1112
OB 12		x	x	x	x	x	1113
OB 13		x	x	x	x	x	1114
OB 14				x	x	x	1115
OB 15				x	x	x	1116
OB 16				x	x	x	1117
OB 17				x	x	x	1118

Organization Blocks (OB), continued

Organization Blocks	CPU 412	CPU 414	CPU 414-4H	CPU 416	CPU 417	CPU 417-4H	Start Events (Hexadecimal Values)
Time-delay interrupts							
OB 20	x	x	x	x	x	x	1121
OB 21	x	x	x	x	x	x	1122
OB 22		x	x	x	x	x	1123
OB 23		x	x	x	x	x	1124
Timed interrupts [1)]							
OB 30				x	x	x	1131
OB 31				x	x	x	1132
OB 32	x	x	x	x	x	x	1133
OB 33		x	x	x	x	x	1134
OB 34		x	x	x	x	x	1135
OB 35	x	x	x	x	x	x	1136
OB 36				x	x	x	1137
OB 37				x	x	x	1138
OB 38				x	x	x	1139

[1)] Further start events of H-CPUs for OB 30 to OB 38: 1130_H

Organization Blocks (OB), continued

Organization Blocks	CPU 412	CPU 414	CPU 414-4H	CPU 416	CPU 417	CPU 417-4H	Start Events (Hexadecimal Values)
Hardware interrupts							
OB 40	x	x	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 41	x	x	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 42		x	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 43		x	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 44				x	x	x	1141, 1142, 1143, 1144, 1145
OB 45				x	x	x	1141, 1142, 1143, 1144, 1145
OB 46				x	x	x	1141, 1142, 1143, 1144, 1145
OB 47				x	x	x	1141, 1142, 1143, 1144, 1145
Interrupt OBs for DPV1:							
OB 55	x	x	x	x	x	x	1155
OB 56	x	x	x	x	x	x	1156
OB 57	x	x	x	x	x	x	1157

Organization Blocks (OB), continued

Organization Blocks	CPU 412	CPU 414	CPU 414-4H	CPU 416	CPU 417	CPU 417-4H	Start Events (Hexadecimal Values)
Multicomputing interrupts							
OB 60	x	x		x	x		1161, 1162
Synchronous cycle interrupt:							
OB 61	x	x		x	x		1164
OB 62	x	x		x	x		1165
OB 63	x	x		x	x		1166
OB 64	x	x		x	x		1167
Redundancy error interrupts:							
OB 70			x			x	73A2, 73A3, 72A3
OB 72			x			x	7301, 7302, 7303, 7320, 7321, 7322, 7323, 7331, 7333, 7334, 7335, 7340, 7341, 7342, 7343, 7344, 7950, 7951, 7952, 7852, 7953, 7954, 7955, 7855, 7956, 73C1, 73C2
Asynchronous error interrupts:							
OB 80	x	x	x	x	x	x	3501, 3502, 3505, 3506, 3507, 350A
OB 81	x	x	x	x	x	x	3821, 3822, 3823, 3825, 3826, 3827, 3831, 3832, 3833, 3921, 3922, 3923, 3925, 3926, 3927, 3931, 3932, 3933
OB 82	x	x	x	x	x	x	3842, 3942

Organization Blocks	CPU 412	CPU 414	CPU 414-4H	CPU 416	CPU 417	CPU 417-4H	Start Events (Hexadecimal Values)
OB 83	x	x	x	x	x	x	3267, 3367, 3861, 3863, 3864, 3865, 3961, 3968
OB 85	x	x	x	x	x		35A1, 35A2, 35A3, 38B3, 38B4, 39B1, 39B2, 39B3, 39B4
OB 86	x	x	x	x	x	x	38C1, 38C2, 39C1, 38C6, 38C7, 38C8 38C4[1)], 38C5[1)], 39C3[1)], 39C4[1)], 39C5[1)]
OB 87	x	x	x	x	x	x	35D2, 35D3, 35D4, 35D5, 35E1, 35E2, 35E3, 35E4, 35E5, 35E6
OB 88	x	x	x	x	x	x	3571, 3572, 3573, 3574, 3575, 3576, 3578, 357A
Background:							
OB 90	x	x		x	x		1191, 1192, 1193, 1195
Warm restart: [1)]							
OB 100	x	x	x	x	x	x	1381, 1382, 138A, 138B
Hot restart:							
OB 101	x	x		x	x		1383, 1384
Cold restart:							
OB 102	x	x	x	x	x	x	1385, 1386, 1387, 1388
Synchronous error interrupts:							
OB 121	x	x	x	x	x	x	2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 253A, 253C, 253D, 253E, 253F
OB 122	x	x	x	x	x	x	2942, 2943, 2944, 2945

[1)] Further start events of H-CPUs for OB 100: $138C_H$, $138D_H$

Function Blocks (FB)

The following tables list the quantities, numbers and maximum sizes of the function blocks you can create for the various S7-400 CPUs.

Function Blocks	CPU 412-1	CPU 412-2	CPU 414	CPU 416	CPU 417
Quantity	256	256	1024	2048	6144
Permissible numbers	0 to 255	0 to 255	0 to 1023	0 to 2047	0 to 6143
Maximum size of a function block (code required for execution)	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes

Functions (FC) and Data Blocks

The following tables list the quantities, numbers and maximum sizes of the functions and data blocks you can create for the various S7-400 CPUs.

Functions	CPU 412-1	CPU 412-2	CPU 414	CPU 416	CPU 417
Quantity	256	256	2048	2048	6144
Permissible numbers	0 to 255	0 to 255	0 to 2047	0 to 2047	0 to 6143
Maximum size of a function (code required for execution)	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes

Data Blocks	CPU 412-1	CPU 412-2	CPU 414	CPU 416	CPU 417
Quantity	511	511	4095	4095	8191
Permissible numbers	1 to 511	1 to 511	1 to 4095	1 to 4095	1 to 8191
Maximum size of a data block (number of data bytes)	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes

System Functions

The following tables show the system functions which are provided by the operating system of the S7-400 CPUs and the execution times for the various CPUs. (X: function available, execution times not yet available before printing).

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
0	SET_CLK	Set clock	195	111	75	66	267	647	170	507
1	READ_CLK	Read clock	31	18	13	10	19	55	11	37
2	SET_RTM	Set run-time meter	27	16	11	9	16	16	10	10
3	CTRL_RTM	Start and stop run-time meter	23	14	10	8	13	13	8	8
4	READ_RTM	Read run-time meter	29	18	12	10	18	51	11	30
5	GADR_LGC	Find logical address of a channel Rack 0	38	23	15	13	23	23	13	13
		internal DP	51	31	21	18	31	31	18	18
6	RD_SINFO	Read start information of current OB	33	20	14	11	20	20	11	11
7	DP_PRAL	Trigger a process interrupt at the DP master First call	275	170	113	106	--	--	--	--
		Intermediate call	25	15	10	8	--	--	--	--
		Last call	25	15	10	8	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
9	EN_MSG	Enable block-related, symbol-related, and group status messages. First call, REQ = 1	182	103	69	59	116	231	68	144
		Last call	41	24	16	13	25	61	15	40
10	DIS_MSG	Disable block-related, symbol-related, and group status messages. First call, REQ = 1	183	104	70	60	117	240	68	145
		Last call	41	24	16	13	25	60	15	40

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
11	DPSYC_FR	Synchronize groups of DP Slaves First call, internal DP interface, REQ = 1	158	90	60	52	--	--	--	--
		Intermediate call, internal DP interface, BUSY = 1 [1]	40+ n* 4	23+ n* 3	16+ n* 2	13+ n* 2	--	--	--	--
		Last call, internal DP interface, BUSY=0 [1]	42+ n* 4	24+n *3	17+ n* 2	14+ n* 2	--	--	--	--
11	DPSYC_FR	First call, external DP interface, REQ=1	76	51	40	36	--	--	--	--
		Intermediate call, external DP interface, BUSY = 1 [1]	56+ n* 4	35+ n* 3	26+ n* 2	52+ n* 2	--	--	--	--
		Last call, external DP interface, BUSY= 0 [1]	56+ n* 4	35+ n* 3	26+ n* 2	23+ n* 2	--	--	--	--

[1] n = number of active jobs with the same logic address

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 414-7H solo	CPU 417-4H redun-dant
12	D_ACT_DP	Deactivate and activate DP slaves via integrated DP interface, MODE = 0	86	50	34	29	--	--	--	--
12	D_ACT_DP	Deactivate and activate DP slaves via integrated DP interface, MODE = 1 First call	265	149	102	89	--	--	--	--
		Intermediate call	81	48	33	28	--	--	--	--
		Last call	103	61	41	36	--	--	--	--
12	D_ACT_DP	Deactivate and activate DP slaves via integrated DP interface, MODE = 2 First call	485	290	193	170	--	--	--	--
		Intermediate call	81	48	32	28	--	--	--	--
		Last call	101	60	40	35	--	--	--	--
12	D_ACT_DP	Deactivate and activate DP slaves via external DP interface, MODE = 0	86	51	34	29	--	--	--	--
12	D_ACT_DP	Deactivate and activate DP slaves via external DP interface, MODE = 1 First call	259	144	99	85	--	--	--	--
		Intermediate call	81	48	33	28	--	--	--	--
		Last call	103	61	41	36	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 414-7H solo	CPU 417-4H redun-dant
12	D_ACT_DP	Deactivate and activate DP slaves via external DP interface, MODE = 2 First call	472	280	186	169	--	--	--	--
		Intermediate call	80	48	32	28	--	--	--	--
		Last call	101	60	41	35	--	--	--	--
13	DP_NRMDG	Read slave diagnostic data First call	240	141	95	83	155	200	90	122
		Intermediate call	88	53	36	30	59	59	35	35
		Last call (28 bytes)	122	72	48	42	79	79	45	45

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
14	DPRD_DAT	Read consistent user data (n bytes) via integrated DP interface 3 bytes	56	36	24	21	47	86	29	51
		via integrated DP interface 32 bytes	60	37	25	22	50	98	30	57
		via external DP interface 3 bytes	71	45	32	27	71	90	31	57
		via external DP interface 32 bytes	187	146	115	107	145	192	112	135
15	DPWR_DAT	Write consistent user data (n bytes) via integrated DP interface 3 bytes	60[1]/ 62[2]	36[1]/ 37[2]	25[1]/ 25[2]	21[1]/ 21[2]	42[1] 49[2]	78[1] 82[2]	27[1] 29[2]	45[1] 48[2]
		via integrated DP interface 32 bytes	64[1]/ 66[2]	37[1]/ 41[2]	25[1]/ 26[2]	21[1]/ 22[2]	48[1] 53[2]	80[1] 86[2]	27[1] 31[2]	49[1] 54[2]
		via external DP interface 3 bytes	66[1]/ 68[2]	42[1]/ 43[2]	30[1]/ 31[2]	27[1]/ 27[2]	72[1] 79[2]	89[1] 93[2]	34[1] 37[2]	50[1] 53[2]
		via external DP interface 32 bytes	125[1]/ 128[2]	96[1]/ 98[2]	83[1]/ 85[2]	79[1]/ 80[2]	164[1] 189[2]	175[1] 205[2]	81[1] 91[2]	98[1] 104[2]
17	ALARM_SQ	Generate acknowledgeable block-related messages. First call, SIG = 0 –> 1	276	165	116	98	222	319	107	187
		Empty call	123	72	48	41	74	154	43	93
18	ALARM_S	Generate unacknowledgeable block-related messages. First call, SIG = 0 –> 1	263	155	108	88	214	329	102	184
		Empty call	111	64	43	36	66	151	38	87

[1] without data transmission to the process image

[2] with data transmission to the process image

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
19	ALARM_SC	Acknowledgment status of the last ALARM_SQ entering state message.	81	45	30	25	48	144	27	75
20	BLKMOV	Copy variable within the work memory (n = number of bytes to be copied)	58 + n * 0,08	36 + n * 0,046	23 + n * 0,03	19 + n * 0,03	36 + n * 0,046	36 + n * 0,046	18 + n * 0,03	18 + n * 0,03
		Source = Load memory	610 + n * 0,79	400 + n * 0,48	339 + n * 0,47	386 + n * 0,47	610 + n * 1,6	1058 + n * 1,6	473 + n * 1,2	921 + n * 1,2
21	FILL	Set array default variables within the work memory (n = length of target variables in bytes)	43 + n * 0,024	26 + n * 0,016	17 + n * 0,012	13 + n * 0,01	28 + n * 0,016	28 + n * 0,016	15 + n * 0,01	15 + n * 0,01
22	CREAT_DB	Create data block n = DB length [bytes]	111	65	43	38	100 + n * 0,07	283 + n * 0,07	59 + n * 0,04	169 + n * 0,04
		Occupy last free DB No. from a field of 100 DBs	517	294	196	164	685	859	397	507
23	DEL_DB	Delete data block	112	67	45	39	160	624	95	371
24	TEST_DB	Test data block	35	21	14	12	50	233	30	139
25	COM-PRESS	Compress user memory First call (trigger)	112	64	43	38	77	167	46	97

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
		Intermediate call (active)	24	14	10	8	14	14	8	8
26	UPDAT_PI	Update process image input table (run-time entry for 1 DI 32 in the central rack)	43	28	21	18	49	98	31	58
		AI 8* 13Bit	67	50	42	39	124	173	81	109
27	UPDAT_PO	Update process image output table (run-time entry for 1 DO 32 in the central rack)	39	27	21	18	42	74	27	45
		AO 8* 13Bit	62	46	39	36	97	130	65	83
28	SET_TINT	Set time-of-day interrupt	92	54	36	32	54	92	32	56
29	CAN_TINT	Cancel time-of-day interrupt	30	17	12	10	119	374	74	234
30	ACT_TINT	Activate time-of-day interrupt	63	35	24	21	36	72	22	48
31	QRY_TINT	Query time-of-day interrupt	16	10	7	5	9	9	6	6
32	SRT_DINT	Start time-delay interrupt	49	28	19	17	28	28	17	17
33	CAN_DINT	Cancel time-delay interrupt	33	19	13	11	25	25	15	15
34	QRY_DINT	Query time-delay interrupt	16	10	7	5	10	10	6	6
35	MP_ ALM	Trigger multicomputing interrupt	368	209	142	130	--	--	--	--
36	MSK_FLT	Mask synchronous faults	19	12	8	7	12	12	7	7

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
37	DMSK_FLT	Demask synchronous faults	23	14	10	8	14	14	8	8
38	READ_ERR	Read error register	23	14	9	8	14	14	8	8
39	DIS_IRT	Discard new events Block all events (MODE = 0)	254	126	85	78	128	128	75	75
		Block all events of a priority class (MODE = 1)	55	31	21	18	31	31	18	18
		Block one event (MODE = 2)	31	18	13	11	18	18	11	11
40	EN_IRT	Stop discarding events Enable all events (MODE = 0)	205	121	82	71	129	129	75	75
		Enable all events in a priority class (MODE = 1)	54	30	20	17	30	30	17	17
		Enable an event (MODE = 2)	29	17	12	10	17	17	10	10

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
41	DIS_AIRT	Delay interrupt events the first time delay is activated[1)]	215	129	86	77	140	140	83	83
		if the delay is already activated	18	10	8	6	10	10	6	6

[1)] When activating the delay for the first time, the SFC 41 runtime depends on the priority class in which the SFC 41 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
42	EN_AIRT	if other delays are present	18	11	7	6	11	11	6	6
		Stop delaying interrupt eventswhen can-celing the last delay 1)	437	272	193	171	272	272	172	172
43	RE_TRIGR	Retrigger watchdog monitoring	221	123	82	75	114	339	70	204
44	REPL_VAL	Transfer substitute value to ACCU1	22	13	9	7	13	13	8	8
46	STP	Force CPU into STOP mode cannot be measured	--	--	--	--	--	--	--	--
47	WAIT	Delay program execution in addition to waiting time	15	8	7	5	6 - 9	6 - 9	3 - 5	3 - 5
48	SNC_RTCB	Synchronize slave clocks	19	12	8	7	12	45	7	32
49	LGC_GADR	Find slot with logical address	40	25	17	14	25	25	14	14
50	RD_LGADR	Find all logical addresses of a block (run-time entry for 1 DI 32 in the central rack)	103	61	41	34	62	62	35	35

1) When cancelling the last delay, the SFC 42 runtime depends on the priority class in which the SFC 42 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“Module identification” partial list Display one data record (0111)	125	79	51	46	71	71	47	47
51	RDSYSST	”Module Identification” partial list Display all data records (0012)	256	154	102	89	150	150	96	96
		Display one data record (0112)	156	94	62	55	86	86	56	56
		Display header information (0F12)	111	66	43	39	57	57	40	40
51	RDSYSST	“Save” partial list Display header information (0F13)	135	90	59	53	81	81	54	54

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"System Areas" partial list Display all data records (0014)	146	91	60	52	83	83	53	53
		Display header information (0F14)	100	66	43	38	56	56	38	38
51	RDSYSST	"Block Types" partial list Display all data records (0015)	145	86	57	51	77	77	51	52
51	RDSYSST	"Status of Module LEDs" partial list Display status of all LEDs (0019)	264	157	121	108	163	--	113	--
		Display header information (0F19)	182	113	80	69	126	--	72	--
51	RDSYSST	"Component Identification" partial list Display all components (001C)	199	118	77	70	124	275	74	164
		Display one of the components (011C)	136	84	56	49	91	241	53	136
		Display all components of a H–system CPU (021C)	–	–	–	–	126	276	76	154
		Display a component of all redundant CPUs of the H-system (031C)	–	–	–	–	92	257	54	142
		Display header information (0F1C)	99	69	45	40	75	99	44	99
51	RDSYSST	"Interrupt status" partial list Display one data record (0222)	171	103	68	60	95	95	63	63

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"TPA /CPU assignment" partial list Assignment between all process image partitions and OBs (0025)	344	209	128	120	207	207	118	118
		Assignment between a process image partition and the corresponding OB (0125)	121	78	51	45	81	81	42	42
51	RDSYSST	Assignment between an OB and corresponding process image partitions (0225)	228	173	106	95	-	-	-	-
		Auslesen der Kopfinfo (0F25)	118	70	46	41	-	-	-	-
51	RDSYSST	"Status information communication" partial list Display status information of a communication unit (0132)	165 - 291	97 - 174	64 - 116	57 - 102	108 - 184	133 - 543	63 - 107	88 - 323
51	RDSYSST	"Status information communication" partial list Display status information of a communication unit (0232)	166	100	66	59	152	299	97	186
51	RDSYSST	"H-CPU group information" partial list Current status of the H system (0071)	-	-	-	-	-	122	-	77
		Header information (0F71)	-	-	-	-	-	64	-	15

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“Modules LEDs” partial list Status of an LED (0174)	182	124	88	77	139	165	80	160
51	RDSYSST	“Switched DP slaves in the H system” partial list Communication status between the H system and a switched DP slave (0C75)	-	-	-	-	-	131	-	76

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redundant	CPU 417-4H solo	CPU 417-4H redundant
51	RDSYSST	"DP master system information" partial list All known DP master systems of the CPU (0090)	258	158	105	92	209	209	127	127
		A DP master system (0190)	134	80	53	47	72	72	48	49
		Header information (0F90)	112	67	44	39	59	59	40	40
51	RDSYSST	"Module status information" partial list Display status information of all inserted modules (n=number of DR) (0091)	561 + n * 22	329 + n * 19	218 + n * 16	180 + n * 14	--	--	--	--
		Display status information of all modules /racks with incorrect type indentification (0191)	546 + n * 70	381 + n * 60	230 + n * 40	220 + n * 35	--	--	--	--
		All faulty modules (0291)	515 + n * 99	371 + n * 22	246 + n * 18	213 + n * 18	--	--	--	--
		All unavailable modules (0391)	517 + n * 69	376 + n * 60	249 + n * 40	216 + n * 35	--	--	--	--
		All submodules of the host module (0591)	169	102	67	59	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	Display the status information of all submodules of the host module in the specified rack (0991)	299 + n * 12	179 + n * 7	118 + n * 5	103 + n * 4	--	--	--	--
		Central a module with logical basic address (0C91)	182	118	78	69	121	182	70	125
		Distributed a module with logical basic address (0C91)	236	150	99	87	154	232	89	145
51	RDSYSST	“Module status information” partial list of a module (distributed) with logical basic address (4C91) First call	116	95	63	55	202	250	133	150
		“Module status information” partial list of a module (distributed) with logical basis address (4C91) Intermediate call	--	--	--	--	122	122	85	85

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
		"Module status information" partial list of a module (distributed) with logical basic address (4C91) Last call	--	--	--	--	138	138	92	92
51	RDSYSST	Central all modules in the specified rack (n=number DR) (0D91)	303 + n* 23	178 + n* 16	118 + n* 10	88 + n * 8	178 + n * 18	291 + n * 20	101 + n * 10	178 + n * 12
		Distributed all modules in the specified DP station (0D91)	235 - 274	138 - 161	91 - 107	80 - 94	141 – 168	276 - 293	81 - 95	169 - 183
		all assigned modules (0E91)	854	505	335	289	--	--	--	--
51	RDSYSST	"Rack/station status information" partial list central Display setpoint status of rack 0 (0092)	128	87	57	51	89	114	52	78
		distributed Display setpoint status of DP system 1 (0092)	694	387	257	219	389	421	222	247

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	Display setpoint value of DP system1 (via external DP interface) (4092)	248	146	96	86	158	222	92	140
51	RDSYSST	Display activation status of DP master system 1 (via integrated DP interface) (0192)	676	398	264	226	442	464	238	247
51	RDSYSST	central Display the actual status of rack 0 (0292)	129	87	57	51	89	115	53	61
		distributed Display the actual status of DP system 1 (0292)	677	417	277	239	398	431	242	254
51	RDSYSST	Display the actual status of the stations of a DP master system (via external DP interface) (4292)	250	147	97	86	159	231	93	141
51	RDSYSST	Display the status of rack 0 battery buffer if at least one battery has failed (0392)	144	87	57	51	89	113	52	77
51	RDSYSST	Display the status of the entire battery buffer of a CPU (0492)	129	87	57	51	89	114	52	78

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	Display the status of the 24 V supply of all racks of a CPU (0592)	144	87	57	51	89	114	52	78
51	RDSYSST	Central Display the diagnostic status of the expansion devices (0692)	280	168	111	96	170	195	96	121
51	RDSYSST	Distributed Display the diagnostic status of the DP system 1 stations (via integrated DP interface) (0692)	811	487	323	273	497	531	288	314
51	RDSYSST	Diagnostic status of the stations of a DP master system connected via an external DP interface (4692) First call	252	148	97	87	160	224	94	142
		Intermediate call	140	84	55	49	91	91	53	53
		Last call	157	94	62	55	101	101	59	59
51	RDSYSST	“Advanced DP master system information” partial list Display advanced information via a DP master system (0195)	156	93	61	55	87	87	56	56
		Display header information (0F95)	114	69	45	40	60	60	41	41

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"Diagnostic buffer" partial list Display all deliverable event information in the current operating mode (max. 21) (00A0)	135 - 314	86 - 188	60 - 125	45 - 111	86 - 188	86 - 188	51 - 112	51 - 112
		Display the latest entries (n = 1-23) (01A0)	135 + n* 7,8	86 + n* 4,4	57 + n* 3	50 + n* 3	86 + n* 4,4	86 + n* 4,4	51 + n* 3	51 + n* 3
		Display the header information (0FA0)	115	75	49	43	75	75	45	45
51	RDSYSST	"Diagnostic data DS 0" partial list Display via logical basic address (00B1) Central	342	212	148	133	232	282	138	146
51	RDSYSST	Distributed (00B1) first call	313	184	123	109	194	278	113	151
		Distributed (00B1) intermediate call, REQ = 0	172	103	68	60	105	105	63	63
		Distributed (00B1) last call	195	116	77	68	120	120	73	73

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“Diagnostic data DR 1” partial list Display via physical address (00B2) Display a 16–byte long DR 1	247	147	100	89	158	184	98	135
51	RDSYSST	“Diagnostic data DR 1” partial list Display via logical basic address (00B3) Display a 16–byte long DR 1 central	383	245	178	162	257	307	172	203
		distributed first call (00B3)	312	183	122	108	185	231	112	151
		distributed intermediate call (00B3)	173	102	68	59	104	104	61	61
		distributed last call (00B3)	214	127	84	74	131	131	76	76

DR = Data record

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	”Diagnostic Data DP Slave” partial list Display via configured diagnostic address (00B4) First call	311	182	122	108	197	233	115	147
		Intermediate call, REQ = 0 (00B4)	174	101	67	59	109	109	64	64
		Last call (6 - 240 bytes) (00B4)	263	157	106	94	160	160	96	96
52	WR_USMSG	Write user entry in diagnostic buffer write with message	151	93	66	54	76	101	33	59
		without message	87	53	36	30	56	91	32	58
54	RD_DPARAM	Read dynamic parameters local AI 8*13 bits	154	85	57	50	94	127	55	74
		distributed AI 8*12 bits (DS1 = 14 bytes)	167	101	68	59	107	107	62	62
55	WR_PARM	Write dynamic parameters local AI 8*13 bits	359	228	164	146	243	309	156	194
		distributed First call AI 8*12 bits (14 - 240 bytes)	308	182	123	107	195	242	114	145
		distributed Intermediate/last call, REQ = 0	138	82	55	48	89	89	51	51

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
56	WR_DPARM	Write predefined dynamic parameters AI 8*13 bits local	404	272	203	184	280	348	196	232
		distributed First call AI 8*12 bits (2 - 240 bytes)	248	146	98	85	158	204	93	124
		Intermediate/last call	121	72	48	41	79	79	46	46
57	PARM_MOD	Assign module parameters local Module/DS number/DS lengths in bytes AI 8*13 bits	695	459	349	318	480	582	332	390
		distributed AO 8*12 bits First call (16 - 240 bytes)	245	144	97	84	156	204	92	123
		distributed Intermediate/last call	118	70	47	41	77	77	46	46

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
58	WR_REC	Write parameter data record local (n = number of bytes)	279 + n * 3	170 + n * 2,5	120 + n * 2,3	107 + n * 2,2	183 + n * 2,6	246 + n * 2,6	109 + n * 2,2	120 + n * 2,2
		First call, integrated DP interface module (n = number of bytes)	283 + n * 0,1	168 + n * 0,04	113 + n * 0,03	97 + n * 0,03	180 + n * 0,06	226 + n * 0,06	104 + n * 0,06	136 + n * 0,06
		Intermediate call, REQ = 0 integrated DP interface module	112	66	45	38	74	74	42	42
		Last call, integrated DP interface module	114	67	45	38	75	75	43	43
		First call, external DP interface module (n = number of bytes)	277 + n * 0,06	163 + n * 0,06	109 + n * 0,04	96 + n * 0,03	185 + n * 0,06	185 + n * 0,06	98 + n * 0,03	98 + n * 0,03
		Intermediate call, REQ = 0 external DP interface module	113	67	45	40	71	71	42	42
		Last call, external DP interface module	115	68	46	40	72	72	42	42

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
59	RD_REC	Read data record local (n = number of bytes)	278 + n * 3,2	169 + n * 2,7	119 + n * 2,4	106 + n * 2,3	220 + n * 2,8	280 + n *2,9	116 + n * 2,3	132 + n * 2,4
		First call, integrated DP interface module	264	156	105	91	167	224	97	129
		Intermediate call, REQ = 0 integrated DP interface module	112	66	45	38	74	74	42	42
		Last call, integrated DP interface module (n = number of bytes)	201 + n * 0,04	119 + n * 0,04	81 + n * 0,03	70 + n * 0,03	125 + n * 0,13	125 + n * 0,13	73 + n * 0,13	73 + n * 0,13
		First call, external DP interface module	255	151	101	88	164	164	96	96
		Intermediate call, REQ = 0 external DP interface module	113	67	45	40	74	74	45	45
		Last call, external DP interface module (n = number of bytes)	196 + n * 0,06	116 + n * 0,06	78 + n * 0,03	68 + n * 0,03	121 + n * 0,1	121 + n * 0,1	71 + n * 0,05	71 + n * 0,05
60	GD_SND	Send GD packet 1 byte	207	124	83	72	--	--	--	--
		32 bytes	553	331	212	183	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
61	GD_RCV	Receive GD package (1 - 32 Byte)	100	60	41	35	--	--	--	--
62	CONTROL	Check status of the connection belonging to a local communication-SFB-instance	104	63	44	35	74	112	40	69
64	TIME_TCK	Display millisecond timer	19	11	8	6	11	45	7	27
65	X_SEND	Transmit data to external partner First call, establish a connection (1 - 76 bytes) REQ = 1	641	458	412	355	--	--	--	--
		First call, connection present (1-76 bytes)	509	293	195	168	--	--	--	--
		Intermediate call (1-76 bytes)	150	87	58	49	--	--	--	--
		Last call, BUSY = 0	254	150	100	87	--	--	--	--
66	X_RCV	Receive data from external partner Test reception (1-76 bytes)	89	49	33	28	--	--	--	--
		Read data (1-76 bytes)	270	155	107	87	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
67	X_GET	Read data from external partner First call, establish a connection (1-76 bytes) REQ = 1	572	416	384	332	--	--	--	--
		First call, connection present (1-76 bytes)	444	252	167	144	--	--	--	--
		Intermediate call (1-76 bytes)	153	89	60	50	--	--	--	--
		Last call BUSY = 0	364	214	142	123	--	--	--	--
68	X_PUT	Write data to external partner First call, establish a connection (1-76 bytes) REQ = 1	651	462	415	357	--	--	--	--
		First call, connection present (1-76 bytes)	519	297	198	170	--	--	--	--
		Intermediate call (1-76 bytes)	155	89	60	51	--	--	--	--
		Last call, BUSY = 0	259	151	101	87	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
69	X_ABORT	Abort connection to external partner First call, REQ = 1	239	139	88	78	--	--	--	--
		Intermediate call	109	64	43	36	--	--	--	--
		Last call, BUSY = 0	228	219	254	219	--	--	--	--
72	I_GET	Read data from internal partner First call, establish a connection (1-76 bytes) REQ = 1	732	442	401	346	--	--	--	--
		First call, connection present (1-76 bytes)	425	225	170	153	--	--	--	--
		Intermediate call (1-76 bytes)	175	93	62	53	--	--	--	--
		Last call, BUSY = 0	407	218	145	126	--	--	--	--
73	I_PUT	Write data to internal partner First call, establish a connection (1-76 bytes) REQ = 1	539 - 843	304 - 486	204 - 431	172 - 372	--	--	--	--
		First call, connection present (1-76 bytes)	539	301	201	178	--	--	--	--
		Intermediate call (1-76 bytes)	172	94	63	53	--	--	--	--
		Last call, BUSY = 0	252	155	103	90	--	--	--	--

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
74	I_ABORT	Abort connection to internal partner First call, REQ = 1	192	131	88	82	--	--	--	--
		Intermediate call	103	62	42	35	--	--	--	--
		Last call, without / with connection BUSY = 0	226	62 / 217	48 / 253	37 / 217	--	--	--	--
79	SET [1]	Set bit array in I/O area n = number of bits to set at 1	31 + n * 0,25	20 + n * 0,2	14 + n * 0,2	11 + n * 0,2	37 + n * 1,0	75 + n * 1,1	22 + n * 0,7	44 + n * 0,7
80	RSET [1]	Delete bit array in I/O area n = number of bits to set at 0	31 + n * 0,25	19 + n * 0,2	14 + n * 0,2	11 + n * 0,2	38 + n * 1,0	76 + n * 1,1	23 + n * 0,7	44 + n * 0,7
81	UBLKMOV	Copy variable without interruption n = number of bytes to copy	39 + n* 0,08	23 + n* 0,05	16 + n* 0,03	12 + n* 0,03	24 + n* 0,05	24 + n* 0,05	13 + n* 0,03	13 + n* 0,03
87	C_DIAG	Determine current connection status MODE = 0	28	17	12	9	22	69	13	44
		Mode = 1, 2, 3	129	136	167	146	185	567	206	664
90	H_CTRL	Influence processes involving fault-tolerant systems	--	--	--	--	12	12	8	8

[1] Measured with I/O modules of the type “Binary Simulator C79459-A1002-A1, Release 1” in the central rack

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
100	SET_CLKS	Set time-of-day and clock status MODE = 1	192	112	75	66	266	828	169	501
		MODE = 2	109	62	41	36	166	431	102	264
		MODE = 3	189	115	75	69	270	842	171	506
103	DP_TOPOL	Detemine bus topology in a DP master system first call, REQ = 1	272	160	109	96	174	319	103	184
		Intermediate call	46	27	19	16	28	28	17	17
		Last call BUSY = 0	49	28	20	17	31	31	18	18
104	CIR	Controls the CiR procedure MODE = 0, information	19	11	8	6	15	–	9	–
		MODE = 1, Enable CiR procedure	19	11	8	6	15	–	9	–
		MODE = 2, Disable CiR procefure entirely	19	11	8	6	15	–	9	–
		MODE = 3, Disable CiR procedure partially	19	11	8	6	15	–	9	–

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
105	READ_SI	Read dynamically assigned system resources MODE = 0	132 - 1185 0)	80 - 988 0)	53 - 1291 0)	45 - 1168 0)	81 - 1022 0)	81 - 1026 0)	47 - 1182 0)	47 - 1187 0)
		MODE = 1	161 - 1455 1)	93 - 1185 1)	62 - 1535 1)	53 - 1392 1)	110 - 1250 1)	284 - 1426 1)	47 - 1188 1)	187 - 1557 1)
		MODE = 2	161 - 1273 1)	94 - 1026 1)	63 - 1322 1)	53 - 1201 1)	111 - 1055 1)	285 - 1231 1)	65 - 1197 1)	188 - 1326 1)
		MODE = 3	163 - 1459 2)	94 - 1179 2)	63 - 1526 2)	54 - 1390 2)	112 - 1241 2)	275 - 1417 2)	64 - 1418 2)	187 - 1546 2)

0) Depending on the size of the SYS_INST target area and on the number of the system resources to be read

1) Depending on the number of active messages (assigned system resources)

2) Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
106	DEL_SI	Enable dynamically assigned system resources MODE = 1	198 - 1016 1)	111 - 821 1)	75 - 1035 1)	65 - 923 1)	145 - 2442 1)	492 - 12556 1)	85 - 2817 1)	332 - 14262 1)
		MODE = 2	201 - 970 1)	113 - 824 1)	76 - 1035 1)	67 - 925 1)	147 - 875 1)	496 - 1226 1)	86 - 930 1)	334 - 1179 1)
		MODE = 3	198 - 1012 2)	112 - 826 2)	75 - 1043 2)	65 - 927 2)	146 - 2466 2)	494 - 12571 2)	86 - 2854 2)	334 - 14315 2)
107	ALARM_DQ	Acknowledgeable block-related messages create first call, SIG = 0 -> 1	285	170	120	101	221	326	110	191
		Call (without message)	133	79	53	44	82	162	46	96

1) Depending on the number of active messages (assigned system resources)

2) Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPUs 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
108	ALARM_D	Not acknowledgeable block-related messages create first call, SIG = 0 -> 1	273	163	108	91	223	336	106	187
		Call (without message)	122	71	47	39	74	168	42	91
126	SYNC_PI	Update the process image partition of the inputs in a synchronous cycle	61	37	25	21	–	–	–	–
127	SYNC_PO	Update the process image partition of the outputs in a synchronous cycle	60	36	24	20	–	–	–	–

System Function Blocks

The following table lists the system function blocks provided with the operating system of the S7-400 CPUs as well as the execution times of the individual CPUs (X: function exists, execution times were not available when manual was printed).

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
0	CTU	Count up	4	3	1	1	4	4	1	1
1	CTD	Count down	4	2	1	1	2	2	2	2
2	CTUD	Count up and down	4	2	1	1	2	2	2	2
3	TP	Generate pulse	26	15	10	8	16	49	9	28
4	TON	Generate on-delay	25	15	10	8	16	48	10	29
5	TOF	Generate off-delay	19	11	7	6	11	11	6	7
8	USEND	Send data without coordination (one send parameter supplied) JOB activated (1 - 440 bytes)	426 - 448	245 - 260	164 - 174	139 - 153	256 - 282	375 - 408	147 - 165	216 - 233
		JOB checked	147	86	57	49	88	122	50	73
		JOB finished (DONE = 1)	147	84	56	48	85	125	48	72

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
9	URCV	Receive data without coordination (one receive parameter supplied) JOB activated	136	77	50	44	79	119	45	72
		JOB checked	133	78	50	43	79	109	45	68
		JOB finished (NDR = 1; 1 - 440 bytes)	280 - 316	165 - 186	108 - 121	92 - 106	160 - 197	203 - 237	92 - 113	115 - 137
12	BSEND	Send data block by block JOB activated (1 - 3000 bytes)	386	220	148	129	220	293	129	168
		JOB checked	164	95	63	54	95	126	55	78
		JOB finished (DONE = 1)	161	92	62	54	92	132	54	76
13	BRCV	Receive data block by block JOB activated (1 - 3000 bytes)	187	108	71	62	112	153	65	88
		JOB checked	186	109	71	61	111	142	65	87
		JOB finished	163	94	61	53	94	131	53	76

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
14	GET	Read data from remote CPU (one area specified) JOB activated	335	186	129	113	192	269	113	157
		JOB checked	149	86	57	49	88	121	51	74
		JOB finished (NDR = 1; 1 - 450 bytes)	282 - 316	163 - 183	108 - 121	92 - 106	163 - 197	200 - 239	92 - 115	114 - 138
15	PUT	Write data to remote CPU JOB activated (1 - 404 bytes)	445 - 478	257 - 277	173 - 180	147 - 160	267 - 299	386 - 410	154 - 174	222 - 239
		JOB checked	149	86	57	49	88	120	51	74
		JOB finished (DONE = 1)	147	85	56	48	85	125	48	72
16	PRINT	Send data to a printer JOB activated, REQ = 1	462 - 502	260 - 284	174 - 186	150 - 162	279 - 310	399 - 433	159 - 179	227 - 247
		JOB checked	153	88	58	50	91	131	52	75
		JOB finished, DONE = 1	152	86	57	49	87	127	50	73

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
19	START	Start remote device JOB activated, REQ = 1	443	251	164	147	261	330	148	191
		JOB checked	155	90	60	52	92	122	53	76
		JOB finished, DONE = 1	153	89	59	51	90	130	52	77
20	STOP	Stop remote device JOB activated, REQ = 1	411	242	157	136	244	319	143	187
		JOB checked	156	90	59	51	92	132	53	76
		JOB finished, DONE = 1	153	89	58	51	89	128	51	75
21	RESUME	Restart remote device JOB activated, REQ = 1	434	246	159	142	249	330	148	193
		JOB checked	157	90	59	52	92	124	53	76
		JOB finished, DONE = 1	153	90	59	52	90	131	52	75
22	STATUS	Query status of remote partner JOB activated, REQ = 1	279	160	109	97	164	233	97	135
		JOB checked	153	88	58	50	91	123	53	75
		JOB finished, NDR = 1	464	269	177	151	269	301	151	171

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
23	USTATUS	Receive status of remote device without coordination JOB activated, NDR = 1	135	79	50	44	79	119	46	69
		JOB checked	133	77	50	43	78	111	45	68
		JOB finished	462	266	176	150	266	297	150	169
31	NOTIFY_8P	Generate block–related message without acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	543 - 588	309 - 331	207 - 220	178 - 191	315 - 349	470 - 506	181 - 202	273 - 293
		JOB checked	206	118	78	67	118	155	67	89
		JOB finished, DONE = 1	215	123	81	70	123	156	70	90
32	DRUM	Implement sequencer	39	21	14	13	21	55	13	39
33	ALARM	Generate block-related message with acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	552 - 588	312 - 331	209 - 223	183 - 195	314 - 348	468 - 501	183 - 202	277 - 291
		JOB checked	208	119	79	68	119	156	68	89
		JOB finished, DONE = 1	215	123	81	70	123	156	70	89

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
34	ALARM_8	Generate block-related message without accompanying values for 8 signals First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	433	246	165	144	246	359	144	208
		JOB checked	206	118	78	68	118	152	68	89
		JOB finished, DONE = 1	213	121	80	70	121	157	70	89
35	ALARM_8P	Generate block-related message with accompanying values for 8 signals First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	549 - 582	306 - 326	209 - 222	182 - 190	316 - 347	468 - 502	182 - 202	270 - 292
		JOB checked	205	118	78	68	118	156	68	89
		JOB finished, DONE = 1	213	122	81	70	122	156	70	90
36	NOTIFY	Generate block-related message without acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	547 - 586	305 - 329	203 - 216	181 - 189	313 - 345	469 - 503	181 - 200	276 - 289
		JOB checked	204	117	78	67	117	155	67	88
		JOB finished, DONE = 1	213	121	81	70	121	157	70	90

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
37	AR_SEND	Send archive data First call or JOB activated, REQ = 1 (1 - 3000 bytes)	372	215	145	127	229	302	132	183
		JOB checked	160	92	62	54	102	140	57	81
		JOB finished, DONE = 1	160	91	61	54	102	140	57	81
52	RDREC	Read data record from a DP slave via integrated DP interface, First call (2-16 bytes)	289	167	111	97	178	224	106	131
		Intermediate call	128	74	49	43	80	80	47	47
		Last call	221	127	86	76	131	131	78	78
52	RDREC	Read data record from a DP slave via external DP interface, First call (4-16 bytes)	291	167	108	94	179	223	105	132
		Intermediate call	128	74	49	43	80	80	46	46
		Last call	218	123	82	71	131	131	78	78

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
53	WRREC	Write data record in a DP slalve via integrated DP interface, First call (1-10 bytes)	314	182	119	105	190	235	111	136
		Intermediate call	130	76	50	43	81	81	47	47
		Last call	132	77	51	45	83	83	48	48
53	WRREC	Write data record in a DP slave via external DP interface, First call (2-14 bytes)	312	176	116	101	194	225	111	136
		Intermediate call	130	76	50	43	80	80	47	47
		Last call	134	77	51	45	82	82	48	48
54	RALRM	Receive interrupt from a DP slave Runtime measurement for non-I/O-dependent OBs, MODE = 1, OB 1	118	73	48	42	76	76	44	44
54	RALRM	Receive interrupt from a DP slave Runtime measurement at integrated DP interface, MODE = 1, OB 40, OB 83, OB 86	242	141	92	81	230	230	123	123
		OB 55 to OB 57, OB 82	245	145	95	83	238	238	128	128
		OB 70	--	--	--	--	228	228	121	121

SFC No.	SFC Name	Function	Execution Time in µs							
			CPU 412	CPU 414	CPU 416	CPU 417	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
54	RALRM	Receive interrupt from a DP slave Runtime measurement at external DP interface, MODE = 1, OB 40, OB 83, OB 86	404	239	156	137	359	359	208	208
		OB 55 to OB 57, OB 82	675	431	281	246	647	647	368	368
		OB 70	--	--	--	--	412	412	211	211
54	RALRM	Receive interrupt from a DP slave Runtime measurement at central I/O, MODE = 1, OB 40, OB 82, OB 83, OB 86	195	117	77	67	123	123	71	71
		OB 55 to OB 57	583	435	283	248	522	522	298	298

Sublist of the System Status List (SSL)

SSL-ID	Information Functions
	Module Identification
0111	One ident. data record only
	CPU Characteristics
0012	CPU features, all features
0112	Features of a group
0F12	Only SSL partial list header information
	User Memory Area
0F12	Only partial list header information
	User Memory Area
0113	Data record for specified memory area
	Work memory

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	System Areas
0014	System areas, all system areas
0F14	Only partial list header information
	Block Types
0015	Block types, data records for all block types
	Status Module LEDs
0019	Status of all module LEDs
0F19	Only partial list header information
	Component Identification
001C	Identification of all components
011C	Identification of one component
021C	Identification of all components of an H–system CPU
031C	Identification of a component of all redundant CPUs of an H-system
0F1C	Only SSL partial list header information
	Interrupt Status
0222	Data record for specified interrupt

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Assignment between process image partitions and OBs
0025	Assignment betweeen all process image partitions and OBs within the CPU
0125	Assignment between a process image partition and the corresponding OB
0225	Assignment between an OB and the corresponding process image partitions
0F25	Only SSL partial list header information
	Communication Status Data
0132	Status data for a communication unit
0232	Status data for a communication unit
	H CPU Group Information
0071	Information on the current status of the H system
0F71	Only partial list header information
	Status of the Module LEDs
0174	Status of one LED
	Switched DP Slaves in the H System
0C75	Communication status between the H system and a switched DP slave

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	DP Master System Information
0090	Information about all the DP master systems known to the CPU
0190	Information about a DP master system
0F90	Only SSL partial list header information
	Module Status Information (A maximum of 27 data records are supplied)
0091	Module status information of all inserted modules/submodules
0191	Status information of all modules/racks with incorrect type IDs.
0291	Module status information of all faulty modules
0391	Module status information of all unavailable modules
0591	Module status information of all submodules of the host module
0991	Status information of all submodules in the host module in the rack
0C91	Status information of a module in the central rack or connected to an integrated DP interface module via the logical base address
4C91	Status information of a module connected to an external DP interface module via the logical base address
0D91	Status information of all modules in the specified rack
0E91	Status information of all assigned modules

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Rack/Station Status Information
0092	Expected status of the central racks/stations of a DP master system
4092	Expected status of the stations of a DP master system which is connected via an external DP interface module
0192	Activation status of the stations of a DP master system which is connected via an external DP interface module
0292	Actual status of the central racks/stations of a DP master system
4292	Actual status of the stations of a DP master system which is connected via an external DP interface module
0392	Status of the back–up battery of a CPU rack if at least one battery fails
0492	Status of the entire back–up batteries of all racks of the a CPU
0592	Actual status of the racks in the central configuration/stations of DP master system which is connected via an external DP interface module.
0692	OK status of the expansion units in the central configuration/stations of a DP master system which is connected via an integrated DP interface module.
4692	OK status of the stations of a DP master system which is connected via an external DP interface module.
	Addtional DP Master System Information
0195	Additional information on a DP master system
0F95	Only partial list header information

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Diagnostic Buffer (A maximum of 21 data records are supplied)
00A0	All current diagnostic entries available in current operating mode
01A0	Last x entries. X is listed in index
0FA0	Only partial list header information
	Module Diagnostic Data
00B1	First four diagnostic bytes of a module (DS0)
00B2	All diagnostic data of a module ($\leq$ 220 bytes, DS1) (no DP module)
00B3	All diagnostic data of a module ($\leq$ 220 bytes, DS1)
00B4	Diagnostic data of a DP slave with logical base address

Alphabetical Index of Instructions