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S7-400
S7-400 V7.0 instruction list

Parameter Manual

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indicates that minor personal injury can result if proper precautions are not taken.

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indicates that property damage can result if proper precautions are not taken.

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Siemens AG
Division Process Industries and Drives
Postfach 48 48
90026 NÜRNBERG
GERMANY

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Overview

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1.1 Validity Range of the Instructions List

Table 1- 1 This instruction list applies to the CPUs listed below:

Name	Article number
CPU 412	
CPU 412-1	6ES7412-1XJ07-0AB0
CPU 412-2	6ES7412-2XK07-0AB0
CPU 412-2 PN	6ES7412-2EK07-0AB0
CPU 414	
CPU 414-2	6ES7414-2XL07-0AB0
CPU 414-3	6ES7414-3XM07-0AB0
CPU 414-3 PN/DP	6ES7414-3EM07-0AB0
CPU 414F-3 PN/DP	6ES7414-3FM07-0AB0
CPU 416	
CPU 416-2	6ES7416-2XP07-0AB0
CPU 416F-2	6ES7416-2FP07-0AB0
CPU 416-3	6ES7416-3XS07-0AB0
CPU 416-3 PN/DP	6ES7416-3ES07-0AB0
CPU 416F-3 PN/DP	6ES7416-3FS07-0AB0
CPU 417	
CPU 417-4	6ES7417-4XT07-0AB0

1.2 Address Identifiers and Parameter Ranges

Address	Parameter ranges				Description
	412	414	416	417	
Q [1)]	0.0 to 127.7	0.0 to 255.7	0.0 to 511.7	0.0 to 1023.7	Output (in PIQ)
QB [1)]	0 to 127	0 to 255	0 to 511	0 to 1023	Output byte (in PIQ)
QW [1)]	0 to 126	0 to 254	0 to 510	0 to 1022	Output word (in PIQ)
QD [1)]	0 to 124	0 to 252	0 to 508	0 to 1020	Output double word (in the PIQ)
DBX	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in DB
DB max. Number	1 to 16000 3000	1 to 16000 6000	1 to 16000 10000	1 to 16000 16000	Data block
DBB	0 to 65533	0 to 65533	0 to 65533	0 to 65533	Data byte in DB
DBW	0 to 65532	0 to 65532	0 to 65532	0 to 65532	Data word in DB
DBD	0 to 65530	0 to 65530	0 to 65530	0 to 65530	Data double word in DB
DIX	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in instance DB
DI max. Number	1 to 16000 3000	1 to 16000 6000	1 to 16000 10000	1 to 16000 16000	Instance data block
DIB	0 to 65533	0 to 65533	0 to 65533	0 to 65533	Data byte in instance DB
DIW	0 to 65532	0 to 65532	0 to 65532	0 to 65532	Data word in instance DB
DID	0 to 65530	0 to 65530	0 to 65530	0 to 65530	Data double word in instance DB

[1)] Default setting can be changed, see Technical specifications

Address	Parameter ranges				Description
	412	414	416	417	
I [1)]	0.0 to 127.7	0.0 to 255.7	0.0 to 511.7	0.0 to 1023.7	Inputs (in PII)
IB [1)]	0 to 127	0 to 255	0 to 511	0 to 1023	Input byte (in PII)
IW [1)]	0 to 126	0 to 254	0 to 510	0 to 1022	Input word (in PII)
ID [1)]	0 to 124	0 to 252	0 to 508	0 to 1020	Input double word (in PII)
L [1)]	0.0 to 4095.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 32767.7	Local data
LB [1)]	0 to 4095	0 to 8191	0 to 16383	0 to 32767	Local data byte
LW [1)]	0 to 4094	0 to 8190	0 to 16382	0 to 32766	Local data word
LD [1)]	0 to 4092	0 to 8188	0 to 16380	0 to 32764	Local data double word
M	0.0 to 4095.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 16383.7	Bit memory
MB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Memory byte
MW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Memory word
MD	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Bit memory double word

[1)] Default setting can be changed, see Technical specifications

Address	Parameter ranges				Description
	412	414	416	417	
PQB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Peripheral output byte (direct I/O access)
PQW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Peripheral output word (direct I/O access)
PQD	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Peripheral output double word (direct I/O access)
PIB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Peripheral input byte (direct I/O access)
PIW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Peripheral input word (direct I/O access)
PID	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Peripheral input double word (direct I/O access)
T	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Timer
C	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Counters

1.3 Constants

Table 1- 2 The following constants are used:

Constant	Description
B#16# W#16# DW#16#	Hexadecimal constant
D#Date	IEC date constant
L#Integer	32-bit integer constant
P#Bitpointer	Pointer constant
S5T#Time	S7 time constant [1)]
T#Time	Time constant
TOD#Time value	IEC time constant
C#Count value	Counter constant (BCD coded)
2#n	Binary constant
B (b1, b2) or B (b1, b2, b3, b4)	Constant, 2 or 4 byte

[1)] For loading the S7 timers

1.4 Abbreviations

Table 1- 3 The abbreviations are used:

Abbreviation	... Description	Example
k8	8-bit constant 0 to 255	32
k16	16-bit constant 256 to 32 767	28 131
k32	32-bit constant 32 768 to 4 294 967 295	127 624
i8	8-bit integer -128 to +127	-113
i16	16-bit integer -32768 to +32767	+6523
i32	32-bit integer -2 147 483 648 to +2 147 483 647	-2 222 222
m	Pointer constant	P#240.3
n	Binary constant	1001 1100
p	Hexadecimal constant	EA12
LABEL	Symbolic jump address (max. 4 letters)	DEST
a	Byte address	
b	Bit address	
c	Address area (bit)	I, Q, M, L, DBX, DIX
d	Address is in: MD, DBD, DID, or LD	
e	Number is in: MW, DBW, DIW, or LW	
f	Timer/counter number	
g	Address area	IB, QB, PIB, PQB MB, LB, DBB, DIB
h	Address area	IW, QW, PIW, PQW, MW, LW, DBW, DIW
i	Address area	ID, QD, PID, PAD MD, LD, DBD, DID
q	Block number	

1.5 Registers

ACCU1 and ACCU4 (32-bit)

The accumulators are registers for processing bytes, words or double words. The addresses are loaded into the accumulators, where they are logically gated. The result of the operation is always located in ACCU 1 and can be transferred to a memory cell from there.

The accumulators are 32 bit long.

Table 1- 4 Designations:

Accumulator	Bit
ACCUx (x = 1 to 4)	Bit 0 to 31
ACCUx-L	Bit 0 to 15
ACCUx-H	Bit 16 to 31
ACCUx-LL	Bit 0 to 7
ACCUx-LH	Bit 8 to 15
ACCUx-HL	Bit 16 to 23
ACCUx-HH	Bit 24 to 31

Address Registers AR1 and AR2 (32 bit)

The address registers contain the areainternal or areacrossing addresses for instructions using indirect addressing. The address registers are 32 bit long.

The areainternal and/or areacrossing addresses have the following syntax:

- Areainternal address:

  00000000 00000bbb bbbbbbbb bbbbbxxx

- Areacrossing address:

  yyyyyyyy 00000bbb bbbbbbbb bbbbbxxx

Legend for structure of addresses:

- b: Byte address
- x: Bit number
- y: Area identifier (see section: Examples of addressing (Page 15))

1.6 Status Word

Status word (16 bits)

The status word bits are evaluated or set by the instructions.
The status word is 16 bits long.

Bit	Assignment	Description
0	/FC	First input bit scan
1	RLO	Result of logic operation
2	STA	Status
3	OR	Or (AND before OR)
4	OS	Stored overflow
5	OV	Overflow
6	CC0	Condition code
7	CC1	Condition code 1
8	BR	Binary result
9 to 15	Unassigned	-

Addressing

2

2.1 Address types

The following address types are used:

		1st access								2nd access							
	Commands	I	Q	M	P	L	DB	DI	V	I	Q	M	P	L	DB	DI	V
	A, AN, O, ON, X, XN, =, R, S, FP, FN -																
Direct	c 0.0	–	–	–	–	–	–	–	–	c	c	c	–	c	c	c	–
Memory indirect	c [AC D 0]	–	–	AC	–	AC	AC	AC	–	c	c	c	–	c	c	c	–
Memory indirect via block parameter	[#par]	–	–	–	–	–	–	–	–	c	c	c	RE	RE	c	c	c
Register indirect, area-internal	c[AR1, P#..] c[AR2, P#..]	–	–	–	–	–	–	–	–	c	c	c	–	c	c	c	–
Register indirect, area-crossing	[AR1, P#..] [AR2, P#..]	–	–	–	–	–	–	–	–	c	c	c	RE	c	c	c	c
	L, T -																
Direct	cB 0. cW 0. cD 0	–	–	–	–	–	–	–	–	c	c	c	c	c	c	c	–
Memory indirect	cB[AC D 0] cW[AC D 0] cD]AC D 0]	–	–	AC	–	AC	AC	AC	–	c	c	c	c	c	c	c	–
Memory indirect via block parameter	Bpar, Wpar, Dpar	–	–	–	–	–	–	–	–	c	c	c	c	RE	c	c	c
Register indirect, area-internal	cB[AR1, P#..] cW[AR1, P#..] cD[AR1, P#..] cB[AR2, P#..] cW[AR2, P#..] cD[AR2, P#..]	–	–	–	–	–	–	–	–	c	c	c	c	c	c	c	–
Register indirect, area-crossing	B[AR1, P#..] W[AR1, P#..] D[AR1, P#..] B[AR2, P#..] W[AR2, P#..] D[AR2, P#..]	–	–	–	–	–	–	–	–	c	c	c	c	c	c	c	c

		1st access								2nd access							
	Commands	I	Q	M	P	L	DB	DI	V	I	Q	M	P	L	DB	DI	V
	SP, SE, SD, SS, SF, R, FR, L, LC, A, AN, O, ON, X, XN -																
Direct	T 0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Memory indirect	T[AC W 0]	–	–	AC	–	AC	AC	AC	–	–	–	–	–	–	–	–	–
Memory indirect via block parameter	#Tpar	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	S, CU, CD, R, FR, L, LC, A, AN, O, ON, X, XN -																
Direct	C 0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Memory indirect	C[AC W 0]	–	–	AC	–	AC	AC	AC	–	–	–	–	–	–	–	–	–
Memory indirect via block parameter	#Zpar	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	UC, CC -																
Direct	FB 0. FC 0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Memory indirect	FB[AC W 0], FC[AC W 0]	–	–	AC	–	AC	AC	AC	–	–	–	–	–	–	–	–	–
Memory indirect via block parameter	FBpar, #FCpar	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	OPN -																
Direct	DB 0, DI 0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Memory indirect	DB[AC W 0], DI[AC W 0]	–	–	AC	–	AC	AC	AC	–	–	–	–	–	–	–	–	–
Memory indirect via block parameter	DBpar, #FCpar [1)]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

[1)] The STL syntax prohibits opening the 2nd data block as block parameter.

Definition of abbreviations

- c= address range (bit)
- AC= range of address memory cell;
- RE= Range error (invalid range)

See also

Abbreviations (Page 9)

Examples of addressing (Page 15)

2.2 Examples of addressing

Examples of Addressing	Description
Immediate Addressing	
L +27	Load 16bit integer constant "27" into ACCU1
L L#–1	Load 32bit integer constant "-1" into ACCU1
L 2#1010101010101010	Load binary constant into ACCU1
L DW#16#A0F0BCFD	Load hexadecimal constant into ACCU1
L 'END'	Load ASCII character into ACCU1
L T#500 ms	Load time value into ACCU1
L C#100	Load count value into ACCU1
L B#(100,12)	Load 2-byte constant
L B#(100,12,50,8)	Load 4-byte constant
L P#10.0	Load areainternal pointer into ACCU1
L P#E20.6	Load cross-area pointer into ACCU1
L -2.5	Load real number into ACCU1
L D#1995–01–20	Load date
L TOD#13:20:33.125	Load time of day
Direct Addressing	
A I 0.0	ANDing of input bit 0.0
L IB1	Load input byte 1 into ACCU1
L IW 0	Load input word 0 into ACCU1
L ID 0	Load input double word 0 into ACCU1
Indirect Addressing of Timers/Counters	
SP T [LW 8]	Start timer; the timer number is in local data word 8
CU C [LW 10]	Start counter; the counter number is in local data word 10
AreaInternal MemoryIndirect Addressing	
A I [LD 12] **Example:** L P#22.2 T LD 12 A I [LD 12]	AND instruction: The address of the input is in local data double word 12 as pointer
A I [DBD 1]	AND instruction: The address of the input is in data double word 1 of the open DB as pointer
A Q [DID 12]	AND instruction: The address of the output is in data double word 12 of the open instance DB as pointer
A Q [MD 12]	AND instruction: The address of the output is in memory double word 12 as pointer

Examples of Addressing	Description			
Area-Internal Register-Indirect Addressing				
A I [AR1,P#12.2]	AND operation: The address of the input is calculated from the “pointer value in address register 1+ pointer P#12.2"			
Cross-area, register-indirect addressing [1]				
	For cross-area registerindirect addressing, bit 24 to 26 of the address must also contain an area identifier. The address is in the address register.			
	Area ID	**Coding binary**	**Coding hexadecimal**	**Area**
	P	1000 0**000**	80	I/O area
	I	1000 0**001**	81	Input area
	Q	1000 0**010**	82	Output area
	M	1000 0**011**	83	Bit memory area
	DB	1000 0**100**	84	Data area
	DI	1000 0**101**	85	Instance data area
	L	1000 0**110**	86	Local data area
	VL	1000 0**111**	87	Predecessor local data area (access to local data of invoking block)
L B [AR1,P#8.0]	Load byte into ACCU1: The address is calculated from the "pointer value in AR1 + pointer P#8.0"			
A [AR1,P#32.3]	AND operation: The address is calculated from the "pointer value in address register 1+ pointer P#32.3"			
Addressing Via Parameters				
A Parameter	Addressing via parameters			

[1] Logic Instructions with timers and counters (Page 26)

2.3 Examples of how to calculate the pointer

Example for sum of bit addresses ≤7:

```
LAR1 P#8.2
A I [AR1,P#10.2]
```

Result: Input 18.4 is addressed (by adding the byte and bit addresses)

Example for sum of bit addresses >7:

```
L P#10.5
LAR1
A I [AR1,P#10.7]
```

Result: Input 21.4 is addressed (by adding the byte and bit addresses with carry)

2.4 Execution Times with Indirect Addressing

An instruction using indirect operand addressing consists of 2 parts:
1st part: Loading the operand address
2. part: Executing the instruction
This means that when you are working with indirect addresses, you must also calculate the execution time of an instruction from these two parts.

Calculating the Execution Time

The total execution time is calculated as follows:
Execution time for loading the instruction address
+ Execution time of the instruction
= Total execution time of the instruction

The execution times given in the "Instruction list" section are the execution times for the 2nd part of an instruction, i.e., for the actual
execution of an instruction.
You must then add the time required for loading the address to this execution time (see following table).

The following table indicates the execution times for loading the address depending on the location of the address.

Address is in ...	Execution time in ns			
	412	414	416	417
Bit memory address area M				
Word	62.5	37.5	25	15
Double word	62.5	37.5	25	15
Data block DB/DI				
Word	78.13	46.88	31.25	18.75
Double word	78.13	46.88	31.25	18.75
Local data area L				
Word	62.5	37.5	25	15
Double word	62.5	37.5	25	15
AR1/AR2 (area-internal)	0.0 [1)]	0.0 [1)]	0.0 [1)]	0.0 [1)]
AR1/AR2 (cross-area)	0.0 [1)]	0.0 [1)]	0.0 [1)]	0.0 [1)]
Parameter (word) for:				
• Timers	78.13	46.88	31.25	18.75
• Counters	78.13	46.88	31.25	18.75
• Block calls	78.13	46.88	31.25	18.75
Parameter (double word) for				
Bits, bytes, words, and double words	78.13	46.88	31.25	18.75

[1)] Address registers AR1/AR2 do not need to be loaded in separate cycles for addressing

You will find a few examples here for calculating the execution times for the various methods of indirect addressing.

- Calculating the execution time for memory-indirect, area-internal addressing
  Example: A I [DBD 12] ... with CPU 417

Step 1: Loading of the content of DBD 12 (time required is in the above table)

Address is in ...	Execution time in ns
Bit memory address area M	
Word	18.75
Double word	18.75
Data block DB/DI	
Double word	46.88

Step 2: ANDing of the addressed input

Execution time in ns	
Direct addressing	Indirect addressing
18.75 :	Time for AI 46.88+

Total execution time
46.88 ns
+ 18.75 ns
= 65.63 ns

- Calculating the execution time for register-indirect, cross-area addressing
  Example: A [AR1, P#23.1] with I 1.0 in AR1 with CPU 416

Step 1: Loading of the content of AR1 and increasing it by offset 23.1 (time required is in the table above)

Address is in ...	Execution time in ns
:	:
AR1/AR2 (cross-area)	0.00
:	:

Step 2: ANDing of the addressed input

Execution time in ns	
Direct addressing	Indirect addressing
13.25 :	Time for AI 0+

Total execution time
0 ns
+ 13.25 ns
= 13.25 ns

See also

Bit logic instructions (Page 22)

Instruction list

3

This section contains the list of instructions for the S7-400 CPUs. The descriptions have been kept as concise as possible.

Note

Execution times

For indirect addressing and special addresses, you have to also add to the execution times a time for loading of the address or the respective address.

See also:

- Examples of addressing (Page 15)
- Address types (Page 13)

Additional information

Detailed descriptions of the function are included in the STEP 7 reference manuals.

3.1 Logic instructions

3.1.1 Bit logic instructions

All logic operations generate a result of logic operation (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic operations generate the new RLO from the signal state scanned and the old RLO. The logic string ends with an instruction that limits the RLO (e.g., a memory instruction); that is, the /FC bit is set to zero.

Instruc-tion	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
A/ AN		AND/AND-NOT					
	I/Q a.b	Input/output	1 [2] /2	31.25	18.75	12.5	7.5
	M a.b	Bit memory	1 [3] /2	31.25	18.75	12.5	7.5
	L a.b	Local data bit	2	31.25	18.75	12.5	7.5
	DBX a.b	Data bit	2	46.88	28.13	18.75	11.25
	DIX a.b	Instance data bit	2	46.88	28.13	18.75	11.25
	c [d]	Memory-indirect, area-internal [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	c [AR1,m]	Register-indirect, areainternal (AR1) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	c [AR2,m]	Register-indirect, areainternal (AR2) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	[AR1,m]	Cross-area (AR1) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	[AR2,m]	Cross-area (AR2) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	Parameter	Via parameter [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+

[1] I, Q, M, L, DB, DI

[2] With direct operand addressing; address range 0 to 127

[3] With direct addressing; address range 0 to 255

+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: A, AN	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
O/ON		OR/OR-NOT					
	I/Q a.b	Input/output	1 [2] /2	31.25	18.75	12.5	7.5
	M a.b	Bit memory	1 [3] /2	31.25	18.75	12.5	7.5
	L a.b	Local data bit	2	31.25	18.75	12.5	7.5
	DBX a.b	Data bit	2	46.88	28.13	18.75	11.25
	DIX a.b	Instance data bit	2	46.88	28.13	18.75	11.25
	c [d]	Memory-indirect, area-internal [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	c [AR1,m]	Register-indirect, areainternal (AR1) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	c [AR2,m]	Register-indirect, areainternal (AR2) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	[AR1,m]	Cross-area (AR1) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	[AR2,m]	Cross-area (AR2) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	Parameter	Via parameter [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+

[1] I, Q, M, L, DB, DI

[2] With direct operand addressing; address range 0 to 127

[3] With direct operand addressing; address range 0 to 255

+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: O, ON	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

Instruc-tion	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
X/XN		EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT					
	I/Q a.b	Input/output	2	31.25	18.75	12.5	7.5
	M a.b	Bit memory	2	31.25	18.75	12.5	7.5
	L a.b	Local data bit	2	31.25	18.75	12.5	7.5
	DBX a.b	Data bit	2	46.88	28.13	18.75	11.25
	DIX a.b	Instance data bit	2	46.88	28.13	18.75	11.25
	c [d]	Memory-indirect, area-internal [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	c [AR1,m]	Register-indirect, areainternal (AR1) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	c [AR2,m]	Register-indirect, areainternal (AR2) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	[AR1,m]	Cross-area (AR1) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	[AR2,m]	Cross-area (AR2) [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	Parameter	Via parameter [1]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+

[1] I, Q, M, L, DB, DI

+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: X, XN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

See also

Address types (Page 13)

Logic Instructions with Timers and Counters (Page 26)

3.1.2 Bit logic instructions with parenthetical expressions

Saving of the RLO and OR bits and the relevant function identifier (A, AN, ...) to the nesting stack. Seven nesting levels are possible per block. After the right parenthesis, the logic operation indicated by the function identifier is performed on the saved RLO and the current RLO; the current OR is overwritten with the saved OR.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
A(		AND left parenthesis	1	31.25	18.75	12.5	7.5
AN(		AND NOT left parenthesis	1	31.25	18.75	12.5	7.5
O(		OR left parenthesis	1	31.25	18.75	12.5	7.5
ON(		OR NOT left parenthesis	1	31.25	18.75	12.5	7.5
X(		EXCLUSIVE OR left parenthesis	1	31.25	18.75	12.5	7.5
XN(		EXCLUSIVE OR NOT left parenthesis	1	31.25	18.75	12.5	7.5

Status word for: A(, AN(, O(, ON(, X(, XN(,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	1	-	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
)		Right parenthesis, removing an entry from the nesting stack.	1	31.25	18.75	12.5	7.5

Status word for:),	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	Yes	1	Yes	1

3.1.3 ORing of AND functions

ORing of AND operations according to the rule: AND before OR

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
O		ORing of AND operations according to the rule: AND before OR	1	31.25	18.75	12.5	7.5

Status word for: O,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	1	-	Yes

3.1.4 Logic Instructions with Timers and Counters

Querying the status of the addressed timer/counter. The result of the query is linked with the RLO according to the corresponding logic function.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
A/AN		AND/AND-NOT					
	T f	Timer	1[1)]/2	31.25	18.75	12.5	7.5
	T [e]	Timer, memory-indirect addressing	2	31.25+	18.75+	12.5+	7.5+
	C f	Counters	1[1)]/2	31.25	18.75	12.5	7.5
	C [e]	Counter, memory-indirect addressing	2	31.25+	18.75+	12.5+	7.5+
	Timer para. Counter para.	Timer/counter (addressing via parameter)	2	31.25+ 31.25+	18.75+ 18.75+	12.5+ 12.5+	7.5+ 7.5+

[1)] With direct operand addressing; address range 0 to 255

+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: A, AN	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
O/ON		OR/OR-NOT	1[1)]/2				
	T f	Timer	2	31.25	18.75	12.5	7.5
	T [e]	Timer, memory-indirect addressing	1[1)]/2	31.25+	18.75+	12.5+	7.5+
	C f	Counters	2	31.25	18.75	12.5	7.5
	C [e]	Counter, memory-indirect addressing	2	31.25+	18.75+	12.5+	7.5+
	Timer para. Counter para.	Timer/counter (addressing via parameter)	2	31.25+ 31.25+	18.75+ 18.75+	12.5+ 12.5+	7.5+ 7.5+
X/XN		EXCLUSIVE-OR/EXCLUSIVE-OR-NOT					
	T f	Timer	2	31.25	18.75	12.5	7.5
	T [e]	Timer, memory-indirect addressing	2	31.25+	18.75+	12.5+	7.5+
	C f	Counters	2	31.25	18.75	12.5	7.5
	C [e]	Counter, memory-indirect addressing	2	31.25+	18.75+	12.5+	7.5+
	Timer para. Counter para.	EXCLUSIVE-OR timer/counter (addressing via parameter)	2	31.25+ 31.25+	18.75+ 18.75+	12.5+ 12.5+	7.5+ 7.5+

[1)] With direct operand addressing; address range 0 to 255

+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: O, ON, X, XN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

See also

Address types (Page 13)

3.1.5 Word Logic Instructions with the Contents of Accumulator 1

Gating the contents of ACCU1 and/or ACCU1L with a word or double word according to the appropriate function. The word or double word
is either specified in the instruction as an address or is in ACCU2. The result is in ACCU1 or ACCU1-L.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
AW		AND ACCU2L	1	31.25	18.75	12.5	7.5
AW	W#16#p	AND 16-bit constant	2	31.25	18.75	12.5	7.5
OW		OR ACCU2L	1	31.25	18.75	12.5	7.5
OW	W#16#p	OR 16-bit constant	2	31.25	18.75	12.5	7.5
XOW		EXCLUSIVE-OR ACCU2L	1	31.25	18.75	12.5	7.5
XOW	W#16#p	EXCLUSIVE-OR 16-bit constant	2	31.25	18.75	12.5	7.5

Status word for: AW, OW, XOW,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
AD		AND ACCU2	1	31.25	18.75	12.5	7.5
AD	DW#16#p	AND 32-bit constant	3	31.25	18.75	12.5	7.5
OD		OR ACCU2	1	31.25	18.75	12.5	7.5
OD	DW#16#p	OR 32-bit constant	3	31.25	18.75	12.5	7.5
XOD		EXCLUSIVE-OR ACCU2	1	31.25	18.75	12.5	7.5
XOD	DW#16#p	EXCLUSIVE-OR 32-bit constant	3	31.25	18.75	12.5	7.5

Status word for: AW, OW, XOW,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

3.1.6 Logic Instructions Using AND, OR and EXCLUSIVE OR

All logic operations generate a result of logic operation (new RLO). The first instruction in a logic string generates the new RLO from the
signal state scanned. The subsequent logic operations generate the new RLO from the signal state scanned and the old RLO. The logic string ends with an instruction that limits the RLO (e.g., a memory instruction); that is, the /FC bit is set to zero.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
A/AN O/ON X/XN	==0	AND/AND-NOT OR/OR-NOT EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT Result=0 (CC1=0 and CC0=0)	1	31.25	18.75	12.5	7.5
	>0	Result>0 (CC1=1 and CC0=0)	1	31.25	18.75	12.5	7.5
	<0	Result<0 (CC1=0 and CC0=1)	1	31.25	18.75	12.5	7.5
	<>0	Result≠0 ((CC1=0 and CC0=1) or (CC1=1 and CC0=0))	1	31.25	18.75	12.5	7.5

Status word for: A, AN, O, ON, X, XN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
A/AN O/ON X/XN	<=0	Result<=0 ((CC1=0 and CC0=1) or (CC1=0 and CC0=0))	1	31.25	18.75	12.5	7.5
	>=0	Result>=0 ((CC1=1 and CC0=0) or (CC1=0 and CC0=0))	1	31.25	18.75	12.5	7.5

Status word for: A, AN, O, ON, X, XN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Instruc-tion	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
A/AN O/ON X/XN	AO	AND/AND-NOT OR/OR-NOT EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT unordered/invalid math instruction (CC1=1 and CC0=1)	1	31.25	18.75	12.5	7.5
	OS	AND OS=1	1	31.25	18.75	12.5	7.5
	BR	AND BR=1	1	31.25	18.75	12.5	7.5
	OV	AND OV=1	1	31.25	18.75	12.5	7.5

Status word for: A, AN, O, ON, X, XN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

3.2 EdgeTriggered Instructions

The current RLO is compared with the status of the address or "edge bit memory". FP detects a change in the RLO from "0" to "1". FN detects an edge change from "1" to "0".

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
FP/FN		The rising/falling edge is indicated by RLO=1. Auxiliary edge bit memory is the bit addressed in the instruction.					
	I/Q a.b		2	31.25	18.75	12.5	7.5
	M a.b		2	31.25	18.75	12.5	7.5
	L a.b [1]		2	31.25	18.75	12.5	7.5
	DBX a.b		2	78.13	46.88	31.25	18.75
	c [d] [2]		2	78.13	46.88	31.25	18.75
	c [AR1,m] [2]		2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	c [AR2,m] [2]		2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	[AR1,m] [2]		2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	[AR2,m] [2]		2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	Parameter [2]		2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+

[1] Unnecessary if the edge bit memory is in the process image (local data of a block is only valid while the block is running).

[2] I, Q, M, L, DB, DI

+ Plus time for loading the addresses

Status word for: FP, FN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

See also

Address types (Page 13)

Execution Times with Indirect Addressing (Page 18)

3.3 Setting/Resetting Bit Addresses

Assign the value "1" or "0" to the specified address, if RLO = 1. Note MCR dependency

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
S		Set addressed bit to "1"					
R		Set addressed bit to "0"					
	I/Q a.b	Input/output	1[2]/2	31.25	18.75	12.5	7.5
	M a.b	Bit memory	1[3]/2	31.25	18.75	12.5	7.5
	L a.b	Local data bit	2	31.25	18.75	12.5	7.5
	DBX a.b	Data bit	2	78.13	46.88	31.25	18.75
	DIX a.b	Instance data bit	2	78.13	46.88	31.25	18.75
	c [d]	Memory-indirect, area-internal[1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	c [AR1,m]	Register-indirect, areainternal (AR1) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	c [AR2,m]	Register-indirect, areainternal (AR2) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	[AR1,m]	Cross-area (AR1) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	[AR2,m]	Cross-area (AR2) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	Parameter	Via parameter [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+

[1] I, Q, M, L, DB, DI
[2] With direct operand addressing; address range 0 to 127
[3] With direct operand addressing; address range 0 to 255
+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: S, R,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:		-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-		-	0	Yes	-	0

The RLO value is written to the specified address identifier. Note the MCR dependency (see Instructions for the Master Control Relay (MCR) (Page 70)).

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
=		Assign RLO					
	I/Q a.b	Input/output	1[2]/2	31.25	18.75	12.5	7.5
	M a.b	Bit memory	1[3]/2	31.25	18.75	12.5	7.5
	L a.b	Local data bit	2	31.25	18.75	12.5	7.5
	DBX a.b	Data bit	2	78.13	46.88	31.25	18.75
	DIX a.b	Instance data bit	2	78.13	46.88	31.25	18.75
	c [d]	Memory-indirect, area-internal[1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	c [AR1,m]	Register-indirect, areainternal (AR1) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	c [AR2,m]	Register-indirect, areainternal (AR2) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	[AR1,m]	Cross-area (AR1) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	[AR2,m]	Cross-area (AR2) [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+
	Parameter	Via parameter [1]	2	31.25+/78.13+	18.75+/46.88+	12.5+/31.25+	7.5+/18.75+

[1] I, Q, M, L, DB, DI
[2] With direct operand addressing; address range 0 to 127
[3] With direct operand addressing; address range 0 to 255
+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Status word for: =,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	Yes	-	0

See also

Address types (Page 13)

3.4 Instructions Directly Affecting the RLO

The following instructions have a direct effect on the RLO.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
CLR		Set RLO to "0"	1	31.25	18.75	12.5	7.5

Status word for: CLR,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	0	0	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SET		Set RLO to "1"	1	31.25	18.75	12.5	7.5

Status word for: SET,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	1	1	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
NOT,		Negate RLO	1	31.25	18.75	12.5	7.5

Status word for: NOT,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	-
Instruction affects:	-	-	-	-	-	-	1	Yes	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SAVE		Retain the RLO in the Bit BR	1	31.25	18.75	12.5	7.5

Status word for: SAVE,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	Yes	-	-	-	-	-	-	-	-

3.5 Timer Instructions

Starting or resetting a timer. The time value must be in ACCU1L. The instructions are triggered by an edge transition in the RLO. That is, when the status of the RLO has changed between two calls, the instruction is initiated.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SP	T f T [e]	Start timer as pulse on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+
SE	T f T [e]	Start timer as extended pulse on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+
SD	T f T [e]	Start timer as ON delay on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+

Status word for: SP, SE, SD,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

[1)] With direct addressing; timer no.: 0 to 255
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SS	T f T [e]	Start timer as retentive ON delay on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+
SF	T f T [e]	Start timer as OFF delay on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+

Status word for: SS, SF,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct addressing; timer no.: 0 to 255
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

Instruc-tion	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
FR	T f T [e]	Enable timer for restarting on edge change from "0" to "1" (reset edge bit memory for starting timer)	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+
R	T f T [e]	Reset timer	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Timer para.		2	78.13+	46.88+	31.25+	18.75+

Status word for: FR, R,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct addressing; timer no.: 0 to 255
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

See also

Address types (Page 13)

3.6 Counter Instructions

The count value must be in ACCU1-L in the form of a BCD number (0 - 999).

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
S	C f C [e]	Preset counter on edge change from "0" to "1"	1[1)]/2	62.5 62.5+	37.5 37.5+	25.0 25.0+	15 15+
	Counter para.		2	62.5+	37.5+	25.0+	15+
R	C f C [e]	Reset of counter to "0" when RLO = "1"	1[1)]/2	62.5 62.5+	37.5 37.5+	25.0 25.0+	15 15+
	Counter para.		2	62.5+	37.5+	25.0+	15+
CU	C f C [e]	Increment counter by 1 on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Counter para.		2	78.13+	46.88+	31.25+	18.75+

Status word for: S, R, CU,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct addressing; counter no.: 0 to 255

\+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
CD	C f C [e]	Decrement counter by 1 on edge change from "0" to "1"	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Counter para.		2	78.13+	46.88+	31.25+	18.75+
FR	C f C [e]	Enable counter on edge change from "0" to "1" (reset edge bit memory for up and down counting and set a counter)	1[1)]/2	78.13 78.13+	46.88 46.88+	31.25 31.25+	18.75 18.75+
	Counter para.		2	78.13+	46.88+	31.25+	18.75+

Status word for: CD, FR,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct addressing; counter no.: 0 to 255

\+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

3.7 Load Instructions

Loading address identifiers into ACCU1. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
L		Load ...					
	IB a	Input byte	1[2]/2	31.25	18.75	12.5	7.5
	QB a	Output byte	1[2]/2	31.25	18.75	12.5	7.5
	PIB a	Peripheral input byte [1]	1[2]/2	31.25	18.75	12.5	7.5
	MB a	Memory byte	1[3]/2	31.25	18.75	12.5	7.5
	LB a	Local data byte	2	31.25	18.75	12.5	7.5
	DBB a	Data byte	2	31.25	18.75	12.5	7.5
	DIB a	Instance data byte	2	31.25	18.75	12.5	7.5
		... in ACCU1					
	g [d]	Memory-indirect, area-internal [4]	2	31.25+	18.75+	12.5+	7.5+
	g [AR1,m]	Register-indirect, areainternal (AR1) [4]	2	31.25+	18.75+	12.5+	7.5+
	g [AR2,m]	Register-indirect, areainternal (AR2) [4]	2	31.25+	18.75+	12.5+	7.5+
	B[AR1,m]	Cross-area (AR1) [4]	2	31.25+	18.75+	12.5+	7.5+
	B[AR2,m]	Cross-area (AR2) [4]	2	31.25+	18.75+	12.5+	7.5+
	Parameter	Via parameter [4]	2	31.25+	18.75+	12.5+	7.5+

[1] Plus acknowledgment time of the I/O module (> 1 µs) and bus runtimes
[2] With direct addressing; address range 0 to 127
[3] With direct addressing; address range 0 to 255
[4] I, Q, P, M, L, DB, DI
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

If there is remainder of 3 following an integral division of the used address by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
L		Load ...					
	IW a	Input word	1[2]/2	31.25	18.75	12.5	7.5
	QW a	Output word	1[2]/2	31.25	18.75	12.5	7.5
	PIW a	Peripheral input word 1)	1[2]/2	31.25	18.75	12.5	7.5
	MW a	Memory word	1[3]/2	31.25	18.75	12.5	7.5
	LW a	Local data word	2	31.25	18.75	12.5	7.5
	DBW a	Data word	2	31.25	18.75	12.5	7.5
	DIW a	Instance data word	2	31.25	18.75	12.5	7.5
		... in ACCU1-L					
	h [d]	Memory-indirect, area-internal [4]	2	31.25+	18.75+	12.5+	7.5+
	h [AR1,m]	Register-indirect, areainternal (AR1) [4]	2	31.25+	18.75+	12.5+	7.5+
	h [AR2,m]	Register-indirect, areainternal (AR2) [4]	2	31.25+	18.75+	12.5+	7.5+
	W[AR1,m]	Cross-area (AR1) [4]	2	31.25+	18.75+	12.5+	7.5+
	W[AR2,m]	Cross-area (AR2) [4]	2	31.25+	18.75+	12.5+	7.5+
	Parameter	Via parameter [4]	2	31.25+	18.75+	12.5+	7.5+

[1] Plus acknowledgment time of the I/O module (> 1 µs) and bus runtimes
[2] With indirect addressing; address range 0 to 127
[3] With direct addressing; address range 0 to 255
[4] I, Q, P, M, L, DB, DI
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

If the address used cannot be evenly divided by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
L	ID a	Load ...					
	QD a	Input double word	1[2]/2	31.25	18.75	12.5	7.5
	PID a	Output double word	1[2]/2	31.25	18.75	12.5	7.5
		Peripheral input double word [1]	2	31.25	18.75	12.5	7.5
	MD a	Memory double word	1[3]/2	31.25	18.75	12.5	7.5
	LD a	Local data double word	2	31.25	18.75	12.5	7.5
	DBD a	Data double word	2	46.88	28.13	18.75	11.25
	DID a	Instance data double word	2	46.88	28.13	18.75	11.25
		... in ACCU1					
	i [d]	Memory-indirect, area-internal [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	i [AR1,m]	Register-indirect, areainternal (AR1) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	i [AR2,m]	Register-indirect, areainternal (AR2) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	D[AR1,m]	Cross-area (AR1) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	D[AR2,m]	Cross-area (AR2) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	Parameter	Via parameter [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+

[1] Plus acknowledgment time of the I/O module (> 1 µs) and bus runtimes
[2] With indirect addressing; address range 0 to 127
[3] With direct addressing; address range 0 to 255
[4] I, Q, P, M, L, DB, DI
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
L		Load ...					
	k8	8bit constant in ACCU1-LL	2	31.25	18.75	12.5	7.5
	k16	16bit constant in ACCU1-L	2	31.25	18.75	12.5	7.5
	k32	32bit constant in ACCU1	3	31.25	18.75	12.5	7.5
	Parameter	Load constant into ACCU1 (from parameter)	2	46.88+	28.13+	18.75	11.25+
L	2#n	Load 16bit binary constant into ACCU1-L	2	31.25	18.75	12.5	7.5
		Load 32bit binary constant into ACCU1	3	31.25	18.75	12.5	7.5
	B#16#p	Load 8bit hexadecimal constant into ACCU1-L	1	31.25	18.75	12.5	7.5

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
L	W#16#p	Load 16bit hexadecimal constant into ACCU1-L	2	31.25	18.75	12.5	7.5
	DW#16#p	Load 32bit hexadecimal constant into ACCU1	3	31.25	18.75	12.5	7.5

+ Plus time for loading the operand address (see Execution Times with Indirect Addressing (Page 18))

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
L	'x'	Load 1 character	2	31.25	18.75	12.5	7.5
	'xx'	Load 2 characters	2	31.25	18.75	12.5	7.5
	'xxx'	Load 3 characters	3	31.25	18.75	12.5	7.5
	'xxxx'	Load 4 characters	3	31.25	18.75	12.5	7.5
L	D# time value	Load IEC date constant	3	31.25	18.75	12.5	7.5
L	S5T# time value	Load S7 time constant (16 bits)	2	31.25	18.75	12.5	7.5
L	TOD# time value	Load IEC time constant	3	31.25	18.75	12.5	7.5
L	T# time value	Load 16-bit time constant	2	31.25	18.75	12.5	7.5
		Load 32-bit time constant	3	31.25	18.75	12.5	7.5
L	C# Count value	Load counter constant (BCD code)	2	31.25	18.75	12.5	7.5
L	B# (b1, b2)	Load constant as bytes (b1, b2)	2	31.25	18.75	12.5	7.5
	B# (b1, b2, b3, b4)	Load constant as 4 bytes (b1, b2, b3, b4)	3	31.25	18.75	12.5	7.5

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
L	P# bit pointer	Load bit pointer	3	31.25	18.75	12.5	7.5
L	L# integer	Load 32-bit integer constant	3	31.25	18.75	12.5	7.5
L	Real number	Load floating-point number	3	31.25	18.75	12.5	7.5

See also

Constants (Page 8)

Address types (Page 13)

3.8 Load Instructions for Timers and Counters

Loading a time value or count value into ACCU1. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
L	T f T [e]	Load time value	1[1)]/2 2	31.25 31.25+	18.75 18.75+	12.5 12.5+	7.5 7.5+
	Timer para.	Load time value (addressed via parameter)	2	31.25+	18.75+	12.5+	7.5+
L	C f C [e]	Load count value	1[1)]/2 2	31.25 31.25+	18.75 18.75+	12.5 12.5+	7.5 7.5+
	Counter para.	Load count value (addressed via parameter)	2	31.25+	18.75+	12.5+	7.5+
LC	T f T [e]	Load time value BCD-coded	1[1)]/2 2	31.25 31.25+	18.75 18.75+	12.5 12.5+	7.5 7.5+
	Timer para.	Load time value in BCD (addressed via parameter)	2	31.25+	18.75+	12.5+	7.5+
LC	C f C [e]	Load count value in BCD	1[1)]/2 2	31.25 31.25+	18.75 18.75+	12.5 12.5+	7.5 7.5+
	Counter para.	Load count value in BCD (addressed via parameter)	2	31.25+	18.75+	12.5+	7.5+

[1)] With direct addressing, timer/counter no.: 0 to 255
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

See also

Address types (Page 13)

3.9 Transfer Instructions

Transferring the contents of ACCU1 to the specified address identifier. Note that some instructions are affected by the MCR. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
T		Transfer contents of ACCU1-LL to ...					
	IB a	Input byte	1[2]/2	31.25	18.75	12.5	7.5
	QB a	Output byte	1[2]/2	31.25	18.75	12.5	7.5
	PQB	Peripheral output byte [1]	1[2]/2	31.25	18.75	12.5	7.5
	MB a	Memory byte	1[3]/2	31.25	18.75	12.5	7.5
	LB a	Local data byte	2	31.25	18.75	12.5	7.5
	DBB a	Data byte	2	46.88	28.13	18.75	11.25
	DIB a	Instance data byte	2	46.88	28.13	18.75	11.25
	g [d]	Memory-indirect, area-internal [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	g [AR1,m]	Register-indirect, area-internal (AR1) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	g [AR2,m]	Register-indirect, area-internal (AR2) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	B[AR1,m]	Cross-area (AR1) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	B[AR2,m]	Cross-area (AR2) [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+
	Parameter	Via parameter [4]	2	31.25+/46.88+	18.75+/28.13+	12.5+/18.75+	7.5+/11.25+

[1] Plus acknowledgment time of the I/O module (> 1 µs) and bus runtimes
[2] With direct addressing; address range 0 to 127
[3] With direct addressing; address range 0 to 255
[4] I, Q, P, M, L, DB, DI
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

If there is remainder of 3 following an integral division of the used address by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
T		Transfer contents of ACCU1-L to ...					
	IW a	Input word	1[2]/2	31.25	18.75	12.5	7.5
	QW a	Output word	1[2]/2	31.25	18.75	12.5	7.5
	PQW a	Peripheral output word [1]	1[2]/2	31.25	18.75	12.5	7.5
	MW a	Memory word	1[3]/2	31.25	18.75	12.5	7.5
	LW a	Local data word	2	31.25	18.75	12.5	7.5
	DBW a	Data word	2	93.75	56.26	37.5	22.5
	DIW a	Instance data word	2	93.75	56.26	37.5	22.5
	h [d]	Memory-indirect, area-internal [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	h [AR1,m]	Register-indirect, area-internal (AR1) [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	h [AR2,m]	Register-indirect, area-internal (AR2) [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	W[AR1,m]	Cross-area (AR1) [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	W[AR2,m]	Cross-area (AR2) [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	Parameter	Via parameter [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+

[1] Plus acknowledgment time of the I/O module (> 1 µs) and bus runtimes
[2] With direct addressing; address range 0 to 127
[3] With direct addressing; address range 0 to 255
[4] I, Q, P, M, L, DB, DI
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

If the address used cannot be evenly divided by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address	Description	Length in words	Execution time in µs			
				412	414	416	417
T		Transfer contents of ACCU1-L to ...					
	ID a	Input double word	1[2]/2	31.25	18.75	12.5	7.5
	QD a	Output double word	1[2]/2	31.25	18.75	12.5	7.5
	PQD a	Peripheral output double word [1]	2	31.25	18.75	12.5	7.5
	MD a	Memory double word	1[3]/2	31.25	18.75	12.5	7.5
	LD a	Local data double word	2	31.25	18.75	12.5	7.5
	DBD a	Data double word	2	93.75	56.26	37.5	22.5
	DID a	Instance data double word	2	93.75	56.26	37.5	22.5
T	i [d]	Memory-indirect, area-internal [4]	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	i [AR1,m]	Register-indirect, area-internal (AR1) 4)	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	i [AR2,m]	Register-indirect, area-internal (AR2) 4)	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	D[AR1,m]	Cross-area (AR1) 4)	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	D[AR2,m]	Cross-area (AR2) 4)	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+
	Parameter	Via parameter 4)	2	31.25+/93.75+	18.75+/56.26+	12.5+/37.5+	7.5+/22.5+

[1] Plus acknowledgment time of the I/O module (> 1 µs) and bus runtimes
[2] With direct addressing; address range 0 to 127
[3] With direct addressing; address range 0 to 255
[4] I, Q, P, M, L, DB, DI
+ Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))

See also

Address types (Page 13)

3.10 Load and Transfer Instructions for Address Registers

Loading a double word from a memory area or register into address register 1 (AR1) or address register 2 (AR2). The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
LAR1		Load contents from ...					
	-	ACCU1	1	31.25	18.75	12.5	7.5
	AR2	Address register 2	1	31.25	18.75	12.5	7.5
	DBD	Data double word	2	46.88	28.13	18.75	11.25
	DID a	Instance data double word	2	46.88	28.13	18.75	11.25
	m	32bit constant as pointer	3	31.25	18.75	12.5	7.5
	LD a	Local data double word	2	31.25	18.75	12.5	7.5
	MD a	Memory double word	2	31.25	18.75	12.5	7.5
		... in AR1					
LAR2		Load contents from ...					
	-	ACCU1	1	31.25	18.75	12.5	7.5
	DBD a	Data double word	2	46.88	28.13	18.75	11.25
	DID a	Instance data double word	2	46.88	28.13	18.75	11.25
	m	32bit constant as pointer	3	31.25	18.75	12.5	7.5
	LD a	Local data double word	2	31.25	18.75	12.5	7.5
	MD a	Memory double word	2	31.25	18.75	12.5	7.5
		... in AR2					

Transfer a double word from address register 1 (AR1) or address register 2 (AR2) to a memory or a register. The contents of ACCU1
are first saved to ACCU2. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
TAR1		Transfer contents from AR1 to ...					
	-	ACCU1	1	31.25	18.75	12.5	7.5
	AR2	Address register 2	1	31.25	18.75	12.5	7.5
	DBD a	Data double word	2	93.75	56.26	37.5	22.5
	DID a	Instance data double word	2	93.75	56.26	37.5	22.5
	LD a	Local data double word	2	31.25	18.75	12.5	7.5
	MD a	Memory double word	2	31.25	18.75	12.5	7.5
TAR2		Transfer contents from AR2 to ...					
	-	ACCU1	1	31.25	18.75	12.5	7.5
	DBD a	Data double word	2	93.75	56.26	37.5	22.5
	DID a	Instance data double word	2	93.75	56.26	37.5	22.5
	LD a	Local data double word	2	31.25	18.75	12.5	7.5
	MD a	Memory double word	2	31.25	18.75	12.5	7.5
TAR		Exchange the contents of AR1 and AR2	1	31.25	18.75	12.5	7.5

3.11 Load and Transfer Instructions for the Status Word

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
L	STW	Load status word into ACCU1	1	31.25	18.75	12.5	7.5

Status word for: L,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction affects:	-	-	-	-	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
T	STW	Transfer ACCU1 (bits 0 to 8) to the status word	1	31.25	18.75	12.5	7.5

Status word for: T,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

See also

Status Word (Page 11)

3.12 Load Instructions for DB Number and DB Length

Loading the number/length of a data block into ACCU1. The old contents of ACCU1 are saved to ACCU2. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
L	DBNO	Load number of data block	1	31.25	18.75	12.5	7.5
L	DINO	Load number of instance data block	1	31.25	18.75	12.5	7.5
L	DBLG	Load length of data block in bytes	1	31.25	18.75	12.5	7.5
L	DILG	Load length of instance data block in bytes	1	31.25	18.75	12.5	7.5

3.13 Fixedpoint arithmetic (16/32 bit) / Floatingpoint arithmetic (32 bit)

Integer Math (16 bits)

Math instructions on two 16-bit numbers. The result is written to ACCU1 or ACCU1-L. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
+I		Add 2 integers (16 bits) (ACCU1-L)=(ACCU1-L)+ (ACCU2-L)	1	31.25	18.75	12.5	7.5
-I		Subtract 2 integers (16 bits) (ACCU1-L)=(ACCU2-L)- (ACCU1-L)	1	31.25	18.75	12.5	7.5

Status word for: +I, -I,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
*I		Multiply 2 integers (16 bits) (ACCU1)=(ACCU2-L)* (ACCU1-L)	1	31.25	18.75	12.5	7.5
/I		Divide 2 integers (16 bits) (ACCU1-L)=(ACCU2-L): (ACCU1-L) The remainder is in ACCU1-H.	1	125	75	50	30

Status word for: *I, /I,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Integer Math (32 bits)

Math instructions on two 32-bit numbers. The result is written to ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address	Description	Length in words	Execution time in ns			
				412-2 P	414	416	417
+D		Add 2 integers (32 bits) (ACCU1)=(ACCU2)+(ACCU1)	1	31.25	18.75	12.5	7.5
-D		Subtract 2 integers (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	31.25	18.75	12.5	7.5
*D		Multiply 2 integers (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	31.25	18.75	12.5	7.5

Status word for: +D, -D, *D,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Instruc struction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
/D		Divide 2 integers (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	187.5	112.5	75	45
MOD		Divide 2 integers (32 bits) and load the remainder into ACCU1: (ACCU1)=remainder of [(ACCU2):(ACCU1)]	1	187.5	112.5	75	45

Status word for: /D, MOD,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Floating-Point Math (32 bits)

The result of the math instruction is in ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
+R		Add 2 real numbers (32 bits) (ACCU1)=(ACCU2)+(ACCU1)	1	62.5	37.5	25	15
-R		Subtract 2 real numbers (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	62.5	37.5	25	15
*R		Multiply 2 real numbers (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	62.5	37.5	25	15
/R		Divide 2 real numbers (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	187.5	112.5	75	45

Status word for: +R, -R, *R, /R,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
NEGR		Negate the real number in ACCU1	1	31.25	18.75	12.5	7.5
ABS		Form the absolute value of the real number in ACCU1	1	31.25	18.75	12.5	7.5

Status word for: NEGR, ABS,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

3.14 Square root, Square (32bit) / Logarithm function (32bit)

Square Root, Square (32 Bits)

The result of the instruction is in ACCU1. The SQRT instruction can be interrupted.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SQRT		Calculate the square root of a real number in ACCU1	1	250	150	100	60
SQR		Form the square of a real number in ACCU1	1	62.5	37.5	25	15

Status word for: SQRT, SQR,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Logarithmic Functions (32-bit)

The result of the logarithmic function is in ACCU1. The instructions can be interrupted.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
LN		Form the natural logarithm of a real number in ACCU1	1	656.25	393.75	262.5	157.5
EXP		Calculate the exponential value of a real number in ACCU1 to the base e (= 2.71828)	1	656.25	393.75	262.5	157.5

Status word for: LN, EXP,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

3.15 Trigonometrical Functions (32 Bits)

The result of the instruction is in ACCU1. The instructions can be interrupted.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SIN		Calculate the sine of a real number	1	625	375	250	150
ASIN		Calculate the arcsine of a real number	1	2031.25	1218.75	812.5	487.5
COS		Calculate the cosine of a real number	1	625	375	250	150
ACOS		Calculate the arccosine of a real number	1	2062.5	1237.5	825	495
TAN		Calculate the tangent of a real number	1	843.75	506.25	337.5	202.5
ATAN		Calculate the arctangent of a real number	1	593.75	356.25	237.5	142.5

Status word for: SIN, ASIN, COS, ACOS, TAN, ATAN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

3.16 Adding Constants

Adding integer constants and storing the result in ACCU1. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
+	i8	Add an 8bit integer constant	1	31.25	18.75	12.5	7.5
+	i16	Add a 16bit integer constant	2	31.25	18.75	12.5	7.5
+	i32	Add a 32bit integer constant	3	31.25	18.75	12.5	7.5

3.17 Adding Using Address Registers

Adding a 16bit integer to the contents of the address register. The value is either specified as an address in the instruction or is in ACCU1-L. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
+AR1		Add the contents of ACCU1L to those of AR1	1	31.25	18.75	12.5	7.5
+AR1	m (0 to 4095)	Add a pointer constant to the contents of AR1	2	31.25	18.75	12.5	7.5
+AR2		Add the contents of ACCU1L to those of AR2	1	31.25	18.75	12.5	7.5
+AR2	m (0 to 4095)	Add a pointer constant to the contents of AR2	2	31.25	18.75	12.5	7.5

3.18 Comparison Instructions with Integers (16/32 bit) or with 32-bit real numbers

Comparison Instructions (16-bit Integers)

Comparing 16-bit integers in ACCU1-L and ACCU2-L. RLO=1 if the condition is satisfied.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
==I		ACCU2-L=ACCU1-L	1	31.25	18.75	12.5	7.5
<>I		ACCU2-L≠ACCU1-L	1	31.25	18.75	12.5	7.5
<I		ACCU2-L<ACCU1-L	1	31.25	18.75	12.5	7.5
<=I		ACCU2-L<=ACCU1-L	1	31.25	18.75	12.5	7.5
>I		ACCU2-L>ACCU1-L	1	31.25	18.75	12.5	7.5
>=I		ACCU2-L>=ACCU1-L	1	31.25	18.75	12.5	7.5

Status word for: ==I, < >I, <I, <=I, >I, >=I,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	0	-	0	Yes	Yes	1

Comparison Instructions (32-bit Integers)

Comparing the 32bit integers in ACCU1 and ACCU2. RLO=1 if the condition is satisfied.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
==D		ACCU2=ACCU1	1	31.25	18.75	12.5	7.5
<>D		ACCU2≠ACCU1	1	31.25	18.75	12.5	7.5
<D		ACCU2<ACCU1	1	31.25	18.75	12.5	7.5
<=D		ACCU2<=ACCU1	1	31.25	18.75	12.5	7.5
>D		ACCU2>ACCU1	1	31.25	18.75	12.5	7.5
>=D		ACCU2>=ACCU1	1	31.25	18.75	12.5	7.5

Status word for: ==I, < >I, <I, <=I, >I, >=I,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	0	-	0	Yes	Yes	1

Comparison Instructions (32-bit Real Numbers)

Comparing the 32-bit real numbers in ACCU1 and ACCU2.
RLO=1 if the condition is satisfied.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
==R		ACCU2=ACCU1	1	31.25	18.75	12.5	7.5
<>R		ACCU2≠ACCU1	1	31.25	18.75	12.5	7.5
<R		ACCU2<ACCU1	1	31.25	18.75	12.5	7.5
<=R		ACCU2<=ACCU1	1	31.25	18.75	12.5	7.5
>R		ACCU2>ACCU1	1	31.25	18.75	12.5	7.5
>=R		ACCU2>=ACCU1	1	31.25	18.75	12.5	7.5

Status word for: ==R, < >R, <R, <=R, >R, >=R,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	0	Yes	Yes	1

3.19 Shift Instructions

Shifting the contents of ACCU1 and ACCU1L to the left or right by the specified number of places. If no address is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC 1.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SLW [1]		Shift the contents of ACCU1-L to the left. Positions that become free are provided with zeros.	1	31.25	18.75	12.5	7.5
SLW	0 ... 15						
SLD		Shift the contents of ACCU1 to the left. Positions that become free are provided with zeros.	1	31.25	18.75	12.5	7.5
SLD	0 ... 32						
SRW [1]		Shift the contents of ACCU1L to the right. Positions that become free are provided with zeros.	1	31.25	18.75	12.5	7.5
SRW	0 ... 15						

Status word for SLW, SLD, SRW	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

[1] Number of places shifted: 0 to 16

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
SRD		Shift the contents of ACCU1 to the right. Positions that become free are provided with zeros.	1	31.25	18.75	12.5	7.5
SRD	0 ... 32						
SSI [1]		Shift the contents of ACCU1L with sign to the right. Positions that become free are provided with the sign (bit 15).	1	31.25	18.75	12.5	7.5
SSI	0 ... 15						
SSD		Shift the contents of ACCU1 with sign to the right. Positions that become free are provided with the sign (bit 31).	1	31.25	18.75	12.5	7.5
SSD	0 ... 32						

Status word for SLW, SLD, SRW	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

[1] Number of places shifted: 0 to 16

3.20 Rotate Instructions

Rotate the contents of ACCU1 to the left or right by the specified number of places. If no address is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC 1.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
RLD		Rotate the contents of ACCU1 to the left	1	31.25	18.75	12.5	7.5
RLD	0 ... 32						
RRD		Rotate the contents of ACCU1 to the right	1	31.25	18.75	12.5	7.5
RRD	0 ... 32						
RLDA		Rotate the contents of ACCU1 one bit position to the left via condition code bit CC1	1	31.25	18.75	12.5	7.5
RRDA		Rotate the contents of ACCU1 one bit position to the right via condition code bit CC1	1	31.25	18.75	12.5	7.5

Status word for: RLD, RRD, RLDA, RRDA,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

3.21 ACCU-transfer instructions, incrementing and decrementing

The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
CAW		Reverse the order of the bytes in ACCU1-L.	1	31.25	18.75	12.5	7.5
CAD		Reverse the order of the bytes in ACCU1.	1	31.25	18.75	12.5	7.5
TAK		Swap the contents of ACCU1 and ACCU2.	1	31.25	18.75	12.5	7.5
ENT		The contents of ACCU2 and ACCU3 are transferred to ACCU3 and ACCU4.	1	31.25	18.75	12.5	7.5
LEAVE		The contents of ACCU3 and ACCU4 are transferred to ACCU2 and ACCU3.	1	31.25	18.75	12.5	7.5
PUSH		The contents of ACCU1, ACCU2, and ACCU3 are transferred to ACCU2, ACCU3, and ACCU4.	1	31.25	18.75	12.5	7.5
POP		The contents of ACCU2, ACCU3, and ACCU4 are transferred to ACCU1, ACCU2, and ACCU3.	1	31.25	18.75	12.5	7.5
INC	k8	Increment ACCU1LL	1	31.25	18.75	12.5	7.5
DEC	k8	Decrement ACCU1LL	1	31.25	18.75	12.5	7.5

3.22 Program Display and Null Operation Instructions

The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
BLD	k8	Program display instruction: Is treated by the CPU as a null operation instruction.	1	15.63	9.38	6.25	3.75
NOP	0 1	Null operation	1	15.63	9.38	6.25	3.75

3.23 Data Type Conversion Instructions

The results of the conversion are in ACCU1.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
BTI		Convert contents of ACCU1-L from BCD (0 to +/- 999) to integer (16 bits) (BCD To Int)	1	31.25	18.75	12.5	7.5
BTD		Convert contents of ACCU1 from BCD (0 to +/- 9 999 999) to double integer (32 bits) (BCD To Doubling)	1	31.25	18.75	12.5	7.5
DTR		Convert contents of ACCU1 from double integer (32 bits) to real number (32 bits) (Doubleint To Real)	1	62.5	37.5	25	15
ITD		Convert contents of ACCU1 from integer (16 bits) to double integer (32 bits) (Int To Doubleint)	1	31.25	18.75	12.5	7.5

Status word for: BTI, BTD, DTR, ITD,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
ITB		Convert contents of ACCU1-L from integer (16 bits) to BCD (0 to +/- 999) (Int To BCD)	1	31.25	18.75	12.5	7.5
DTB		Convert contents of ACCU1 from double integer (32 bits) to BCD 0 to +/- 9 999 999) (Doubleint To BCD)	1	31.25	18.75	12.5	7.5

Status word for: ITB, DTB,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	Yes	Yes	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
RND		Convert a real number into a 32-bit integer.	1	31.25	18.75	12.5	7.5
RND-		Convert a real number into a 32-bit integer. The number is rounded down to the next whole number.	1	31.25	18.75	12.5	7.5
RND+		Convert a real number into a 32-bit integer. The number is rounded up to the next whole number.	1	31.25	18.75	12.5	7.5
TRUNC		Convert a real number into a 32-bit integer. The places after the decimal point are truncated.	1	31.25	18.75	12.5	7.5

Status word for: RND, RND-, RND+, TRUNC,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	Yes	Yes	-	-	-	-

3.24 Forming the Ones and Twos Complements

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
INVI		Form the ones complement of ACCU1L	1	31.25	18.75	12.5	7.5
INVD		Form the ones complement of ACCU1	1	31.25	18.75	12.5	7.5

Status word for: INVI, INVD	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
NEGI		Form the twos complement of ACCU1L (integer)	1	31.25	18.75	12.5	7.5
NEGD		Form the twos complement of ACCU1 (double integer)	1	31.25	18.75	12.5	7.5

Status word for: NEGI, NEGD,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

3.25 Block Call Instructions

The information on the status word only relates to the block call itself and not to the instructions called in this block.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
CALL	FB q, DB q	Unconditional call of an FB, with parameter passing	15/17 1)	1218.75 2)	731.25 2)	487.5 2)	292.5 2)
CALL	SFB q, DB q	Unconditional call of an SFB, with parameter passing	16/17 1)	1218.75 2)	731.25 2)	487.5 2)	292.5 2)
CALL	FC q	Unconditional call of a function, with parameter passing	7/8 1)	1062.5 2)	637.5 2)	425 2)	255 2)
CALL	SFC q	Unconditional call of an SFC, with parameter passing	8	1062.5 2)	637.5 2)	425 2)	255 2)

Status word for: CALL,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	0	0	1	-	0

1) The instruction length depends on the block number (0...255 or more).
2) Plus time required for transferring parameters

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
UC	FB q FC q	Unconditional call of blocks without parameter transfer	1 1)/2	687.5 687.5	412.5 412.5	275 275	165 165
	FB [e]	Memory-indirect FB call	2	687.5+	412.5+	275+	165+
	FC [e]	Memory-indirect FC call	2	687.5+	412.5+	275+	165+
	Parameter	FB/FC call via parameter	2	687.5+	412.5+	275+	165+
CC	FB q FC q	Conditional call of blocks without parameter transfer	1 1)/2	750/156.25 2) 750/156.25 2)	450/93.75 2)450/93.75 2)	300/62.5 2) 300/62.5 2)	180/37.5 2) 180/37.5 2)
	FB [e]	Memory-indirect FB call	2	750 +/156.25 + 2)	450 +/93.75 + 2)	300 +/62.5 + 2)	180 +/37.5 + 2)
	FC [e]	Memory-indirect FC call	2	750 +/156.25 + 2)	450 +/93.75 + 2)	300 +/62.5 + 2)	180 +/37.5 + 2)
	Parameter	FB/FC call via parameter	2	750 +/156.25 + 2)	450 +/93.75 + 2)	300 +/62.5 + 2)	180 +/37.5 + 2)

Status word for: UC, CC,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	- [3]	-
Instruction affects:	-	-	-	-	0	0	1	- [3]	0

[1] With direct addressing, block no. 0 to 255
[+] Plus time for loading the address (see Execution Times with Indirect Addressing (Page 18))
[2] If call is not executed
[3] Command CC: Depending on RLO, sets RLO = 1

Instruction	Address	Description	Length in words	Execution time in ns							
				412		414		416		417	
				1st opening	2nd - nth opening[1]	1st opening	2nd - nth opening[1]	1st opening	2nd - nth opening[1]	1st opening	2nd - nth opening[1]
OPN		Open a data block									
	DB q DI q	Direct data block Direct instance DB	1[2]/2	125	31.25	75	18.75	50	12.5	30	7.5
	DB [e] DI [e]	Data block, memory-indirect Bit memory address area M Local data area L Data block DB/DI	2	125 125 187.5	62.5 62.5 93.75	75 75 112.5	37.5 37.5 56.25	50 50 75	25 25 37.5	30 30 45	15 15 22.5
	Param.	Data block via parameter	2	187.5	93.75	112.5	56.25	75	37.5	45	22.5

Status word for: OPN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

[1] If the same DB or DI is already open
[2] Direct data block, DB no. 1 to 255

See also

System Functions (SFC) (Page 74)

System Function Blocks (SFB) (Page 91)

3.26 Block End Instructions

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
BE		End block	1	593.75	356.25	237.5	142.5
BEU		End block absolute	1	593.75	356.25	237.5	142.5

Status word for: BE, BEU	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	0	0	1	-	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
BEC		End block conditionally if RLO="1"		656.67 125 [1]	394 75 [1]	262.7 50 [1]	157.6 30 [1]

Status word for: BEC,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	Yes	0	1	1	0

[1] If jump is not executed

3.27 Exchange Data Blocks

Exchanging the two current data blocks. The current data block becomes the current instance data block and vice versa. The status word is not affected.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
CDB		Exchange data blocks	1	62.5	37.5	25	15

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JU	LABEL	Jump unconditionally	2	218.75	131.25	87.5	52.5

Status word for: JU,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JC	LABEL	Jump if RLO="1"	2	218.75/31.25 [1]	131.25/18.75 [1]	87.5/12.5 [1]	52.5/7.5 [1]
JCN	LABEL	Jump if RLO="0"	2	218.75/31.25 [1]	131.25/18.75 [1]	87.5/12.5 [1]	52.5/7.5 [1]

Status word for: JC, JCN,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	1	1	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JCB	LABEL	Jump if RLO="1"; Save the RLO in the BR bit	2	218.75/31.25 [1]	131.25/18.75 [1]	87.5/12.5 [1]	52.5/7.5 [1]
JNB	LABEL	Jump if RLO="0"; Save the RLO in the BR bit	2	218.75/31.25 [1]	131.25/18.75 [1]	87.5/12.5 [1]	52.5/7.5 [1]

[1] If jump is not executed

Status word for: JCB, JNB,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	Yes	-	-	-	-	0	1	1	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JBI	LABEL	Jump if BR="1"	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)
JNBI	LABEL	Jump if BR="0"	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)

1) If jump is not executed

Status word for: JBI, JNBI,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	Yes	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	1	-	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JO	LABEL	Jump on stored overflow (OV="1")	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)

Status word for: JBI, JNBI,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	Yes	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JOS	LABEL	Jump on stored overflow (OS="1")	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)

1) If jump is not executed

Status word for: JOS,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	Yes	-	-	-	-
Instruction affects:	-	-	-	-	0	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JUO	LABEL	Jump if "unordered math instruction" (CC1=1 and CC0=1)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)
JZ	LABEL	Jump if result=0 (CC1=0 and CC0=0)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)
JP	LABEL	Jump if result>0 (CC1=1 and CC0=0)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)
JM	LABEL	Jump if result<0 (CC1=0 and CC0=1)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JN	LABEL	Jump if result ≠ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=1)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)
JMZ	LABEL	Jump if result ≤0 (CC1=0 and CC0=1) or (CC1=0 and CC0=0)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)
JPZ	LABEL	Jump if result ≥0 (CC1=1 and CC0=0) or (CC1=0 and CC0=0)	2	218.75/31.25 1)	131.25/18.75 1)	87.5/12.5 1)	52.5/7.5 1)

1) If jump is not executed

Status word for: JUO, JZ, JP, JM, JN, JMZ, JPZ,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
JL	LABEL	Jump distributor The instruction is followed by a list of jump instructions. The address is a jump label to the subsequent instruction in the list. ACCU1-LL contains the number of the jump instruction to be executed (max. 254). The number of the first jump instruction is 0.	2	218.75	131.25	87.5	52.5
LOOP	LABEL	Decrement ACCU1-L and jump if ACCU1-L ≠ 00 (loop programming)	2	187.5/13.25 1)	112.5/18.75 1)	75/12.5	45/7.5 1)

1) If jump is not executed

Status word for: JL, LOOP,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

3.28 Instructions for the Master Control Relay (MCR)

MCR=1 => MCR is deactivated
MCR=0 => MCR is activated.
"T" and "=" instructions write zeros to the corresponding addresses if RLO = "0"; "S" and "R" instructions leave the memory contents unchanged.

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
MCR(		Open an MCR zone. Save the RLO to the MCR stack.	1	31.25	18.75	12.5	7.5

Status word for: MCR(,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	1	-	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
)MCR		Close an MCR zone. Remove an entry from the MCR stack.	1	31.25	18.75	12.5	7.5

Status word for:)MCR,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	1	-	0

Instruction	Address	Description	Length in words	Execution time in ns			
				412	414	416	417
MCRA		Activate the MCR	1	31.25	18.75	12.5	7.5
MCRD		Deactivate the MCR	1	31.25	18.75	12.5	7.5

Status word for: MCRA, MCRD,	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

3.29 Organization Blocks (OB)

A user program for an S7-400 is made up of blocks containing the instructions, parameters, and data for the respective CPU. The individual CPUs of the S7-400 differ in the number of blocks which you can create for the respective CPU or which are supplied by the operating system of the CPU. You can find a detailed description of the OBs and their use in the manual "Programming with STEP 7 V5.5".

Organization blocks	412	414	416	417	Start events (hexadecimal value)
Free cycle:					
OB 1	x	x	x	x	1101, 1102, 1103, 1104, 1105
Time-of-day interrupts:					
OB 10	x	x	x	x	1111
OB 11	x	x	x	x	1112
OB 12		x	x	x	1113
OB 13		x	x	x	1114
OB 14			x	x	1115
OB 15			x	x	1116
OB 16			x	x	1117
OB 17			x	x	1118
Time-delay interrupts:					
OB 20	x	x	x	x	1121
OB 21	x	x	x	x	1122
OB 22		x	x	x	1123
OB 23		x	x	x	1124
Cyclic interrupts: [1]					
OB 30			x	x	1131
OB 31			x	x	1132
OB 32	x	x	x	x	1133
OB 33		x	x	x	1134
OB 34		x	x	x	1135
OB 35	x	x	x	x	1136
OB 36			x	x	1137
OB 37			x	x	1138
OB 38			x	x	1139
Hardware interrupts:					
OB 40	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 41	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 42		x	x	x	1141, 1142, 1143, 1144, 1145
OB 43		x	x	x	1141, 1142, 1143, 1144, 1145
OB 44			x	x	1141, 1142, 1143, 1144, 1145
OB 45			x	x	1141, 1142, 1143, 1144, 1145

Organization blocks	412	414	416	417	Start events (hexadecimal value)
OB 46			x	x	1141, 1142, 1143, 1144, 1145
OB 47			x	x	1141, 1142, 1143, 1144, 1145
Interrupt OBs for DPV1:					
OB 55	x	x	x	x	1155, 1158
OB 56	x	x	x	x	1156, 1159
OB 57	x	x	x	x	1157, 115A, 115B
Multicomputing interrupts:					
OB 60	x	x	x	x	1161, 1162
Synchronous cycle interrupt:					
OB 61	x	x	x	x	1164
OB 62	x	x	x	x	1165
OB 63		x	x	x	1166
OB 64			x	x	1167
Asynchronous error interrupts:					
OB 80	x	x	x	x	3501, 3502, 3505, 3506, 3507, 3508, 3509, 350A
OB 81	x	x	x	x	3821, 3822, 3823, 3825, 3826, 3827, 3831, 3832, 3833, 3921, 3922, 3923, 3925, 3926, 3927, 3931, 3932, 3933
OB 82	x	x	x	x	3842, 3942
OB 83	x	x	x	x	3951, 3954, 3854, 3855, 3856, 3858, 3861, 3961, 3863, 3864, 3865, 3866, 3966, 3267, 3367, 3968
OB 84	x	x	x	x	3582, 3583, 3986, 3587
OB 85	x	x	x	x	35A1, 35A2, 35A3, 34A4, 35A4, 39B1, 39B2, 38B3, 39B3, 38B4, 39B4
OB 86	x	x	x	x	38C1, 39C1, 38C2, 39C3, 38C4, 39C4, 38C5, 39C5, 38C6, 38C7, 38C8, 39CA, 38CB, 39CB, 38CC, 39CD, 39CE
OB 87	x	x	x	x	35D2, 35D3, 35D4, 35D5, 35E1, 35E2, 35E3, 35E4, 35E5, 35E6
OB 88	x	x	x	x	3573, 3575, 3576
Background:					
OB 90	x	x	x	x	1191, 1192, 1193, 1195
Restart (warm restart):					
OB 100	x	x	x	x	1381, 1382, 138A, 138B
Hot restart:					
OB 101	x	x	x	x	1383, 1384
Cold restart:					
OB 102	x	x	x	x	1385, 1386, 1387, 1388

Organization blocks	412	414	416	417	Start events (hexadecimal value)
Synchronous error interrupts:					
OB 121	x	x	x	x	2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 253A, 253C, 253D, 253E, 253F
OB 122	x	x	x	x	2942, 2943, 2944, 2945

[1] Additional start event of the H-CPUs for OB 30 to OB 38: 1130H

3.30 Function Blocks (FBs)

The following table lists the quantity, number and maximum size of the function blocks that you can define in the individual CPUs of the S7-400.

Function blocks	412	414	416	417
Number	1500	3000	5000	8000
Permissible numbers	0 to 7999	0 to 7999	0 to 7999	0 to 7999
Maximum size (runtime-relevant code)	64 KB	64 KB	64 KB	64 KB

3.31 Functions (FC)

The following table lists the quantity, number and maximum size of the functions that you can define in the individual CPUs of the S7-400.

Functions	412	414	416	417
Number	1500	3000	5000	8000
Permissible numbers	0 to 7999	0 to 7999	0 to 7999	0 to 7999
Maximum size (runtime-relevant code)	64 KB	64 KB	64 KB	64 KB

3.32 Data blocks (DB)

The following table lists the quantity, number and maximum size of the data blocks that you can define in the individual CPUs of the S7-400.

Data blocks	412	414	416	417
Number	3000	6000	10000	16000
Permissible numbers	1 to 16000	1 to 16000	1 to 16000	1 to 16000
Maximum size (runtime-relevant code)	64 KB	64 KB	64 KB	64 KB

3.33 System Functions (SFC)

The following tables show the system functions offered by the operating system of the S7-400 CPUs and the execution times on the respective CPU.

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
0	SET_CLK	Set time of day	53	32	20	13
1	READ_CLK	Read time of day	8	3	2	2
2	SET_RTM	Set operating hours counter	8	2	2	2
3	CTRL_RTM	Starts/stops operating hours counter	7	2	2	1
4	READ_RTM	Read operating hours counter	8	2	2	2
5	GADR_LGC	Find logical address of a channel Rack 0	9	7	3	3
		Internal DP	15	8	3	2
6	RD_SINFO	Read start information of current OB	8	3	2	2
7	DP_PRAL	Trigger a hardware interrupt on the DP master First call	115	76	62	44
		Intermediate call	13	9	7	4
		Last call	13	9	7	4
9	EN_MSG	Enable block-related, symbol-related, and group status messages. First call, REQ = 1	39	24	16	10
		Last call	8	7	2	2
10	DIS_MSG	Disable block-related, symbol-related, and group status messages. First call, REQ = 1	39	24	16	10
		Last call	8	7	2	2

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
11	DPSYC_FR	Synchronize groups of DP slaves, first call, integrated DP interface, REQ = 1	38	23	15	9
		Intermediate call, integrated DP interface, BUSY = 1 [1]	8+n*2	3+n*2	2+n*2	2+n*2
		Last call, integrated DP interface, BUSY = 0 [1]	8+n*2	3+n*2	2+n*2	2+n*2
11	DPSYC_FR	First call, external DP interface, REQ = 1	29	23	21	21
		Intermediate call, external DP interface, BUSY = 1 [1]	16+n*2	15+n*2	10+n*2	10+n*2
		Last call, external DP interface, BUSY = 0 [1]	16+n*2	15+n*2	10+n*2	10+n*2
[1] n = Number of active jobs with the same logical address						
12	D_ACT_DP	Disabling and enabling DP slaves via integrated DP interface, MODE = 0	22	14	8	5
12	D_ACT_DP	Disabling and enabling DP slaves via integrated DP interface, MODE = 1, 3 First call	78	52	32	19
		Intermediate call	22	14	8	5
		Last call	30	16	10	7
12	D_ACT_DP	Disabling and enabling DP slaves via integrated DP interface, MODE = 2, 4 First call	160	130	78	48
		Intermediate call	30	14	8	5
		Last call	25	16	10	7
12	D_ACT_DP	Disabling and enabling DP slaves via external DP interface, MODE = 0	22	14	8	5
12	D_ACT_DP	Disabling and enabling DP slaves via external DP interface, MODE = 1, 3 First call	76	61	32	17
		Intermediate call	20	14	8	5
		Last call	28	16	10	7
12	D_ACT_DP	Disabling and enabling DP slaves via external DP interface, MODE = 2, 4 First call	154	125	62	39
		Intermediate call	22	14	8	5
		Last call	30	16	10	7
12	D_ACT_DP	Disabling and enabling IO devices via integrated PNIO interface, MODE = 0 [1]	22	14	8	-

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
12	D_ACT_DP	Disabling and enabling IO devices via integrated PNIO interface, MODE = 1, 3 [1] First call	76	60	30	-
		Intermediate call	22	14	8	-
		Last call	30	16	10	-
12	D_ACT_DP	Disabling and enabling IO devices via integrated PNIO interface, MODE = 2, 4 [1] First call	345	269	185	-
		Intermediate call	21	14	8	-
		Last call	28	16	10	-
[1] Only for CPUs with integrated PNIO interface						
12	D_ACT_DP	Disabling and enabling IO devices via external PNIO interface, MODE = 0	21	14	8	6
12	D_ACT_DP	Disabling and enabling IO devices via external PNIO interface, MODE = 1, 3 First call	62	51	32	16
		Intermediate call	22	15	8	6
		Last call	30	17	10	7
12	D_ACT_DP	Disabling and enabling IO devices via external PNIO interface, MODE = 2, 4 First call	431	325	223	151
		Intermediate call	21	15	8	6
		Last call	29	17	10	7
13	DPNRM_DG	Reading diagnostics data of a DP slave First call	62	39	25	17
		Intermediate call	23	20	9	6
		Last call (28 bytes)	31	22	11	7
14	DPRD_DAT	Read consistent user data via integrated DP interface, 3 bytes	24	16	14	12
		Via integrated DP interface, 32 bytes	24	16	14	12
		Via external DP interface, 3 bytes	27	22	18	16
		Via external DP interface, 32 bytes	105	94	75	34
		Via integrated PROFINET interface, 8 bytes	27	20	16	9
		Via integrated PROFINET interface, 32 bytes	29	21	16	9
		Via external PROFINET interface 8 bytes	46	39	31	24
		Via external PROFINET interface 32 bytes	118	97	75	52

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
15	DPWR_DAT	Write consistent user data via integrated DP interface, 3 bytes	31	21	16	13
		Via integrated DP interface, 32 bytes	31	21	16	11
		Via external DP interface, 3 bytes	48	28	16	11
		Via external DP interface, 32 bytes	104	71	57	36
		Write consistent user data via integrated PROFINET interface, 8 bytes	29	21	16	12
		Via integrated PROFINET interface, 32 bytes	29	22	16	13
		Via external PROFINET interface 8 bytes	43	30	24	13
		Via external PROFINET interface 32 bytes	101	73	57	34
17	ALARM_SQ [1)]	Generate blockrelated messages that can be acknowledged. First call, SIG = 0 -> 1	93+n*2.2	66+n*1.3	45+n*1.1	27+n*0.6
		Empty call	38+n*2.2	23+n*1.3	12+n*1.1	9+n*0.6
18	ALARM_S [1)]	Generate blockrelated messages that cannot be acknowledged. First call, SIG = 0 -> 1	99+n*2.2	68+n*1.3	46+n*1.1	27+n*0.6
		Empty call	38+n*2.2	23+n*1.3	12+n*1.1	9+n*0.6
19	ALARM_SC [1)]	Acknowledgment state of the last ALARM_SC incoming message	23	15	9	6
[1)] n = Number of allocated system resources						
20	BLKMOV	Copy variable within work memory (n = number of bytes to be copied)	16 + n * 0.01	11 + n * 0.008	8 + n * 0.007	4 + n * 0.006
		Source = Load memory	185 +n * 0.23	162 +n * 0.23	140 + n * 0.23	122 +n * 0.23
21	FILL	Prefill field within work memory (n = length of target variable in bytes)	15 + n * 0.18	8 + n * 0.1	3 + n * 0.07	3 + n * 0.04
22	CREAT_DB	Create data block	32	23	14	8
		Save last free DB no. from field of 100 DBs	124	76	49	30
23	DEL_DB	Delete data block	30	16	10	7
24	TEST_DB	Test data block	8	7	3	2
25	COMPRESS	Compress user memory First call (trigger)	39	25	17	11
		Subsequent call	8	6	2	2
26	UPDAT_PI	Update process image input table (runtime entry for 1 DI 32 in central controller)	14	8	8	8

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
		AI 8 * 13 Bit	31	30	28	28
27	UPDAT_PO	Update outputs (runtime entry for 1 DO 32 in central controller)	9	9	9	8
		AO 8 * 13 Bit	30	25	25	25
28	SET_TINT	Set time-of-day interrupt	23	15	9	6
29	CAN_TINT	Cancel time-of-day interrupt	8	3	2	2
30	ACT_TINT	Activate time-of-day Interrupt	15	8	4	4
31	QRY_TINT	Query time-of-day interrupt	2	2	1	1
32	SRT_DINT	Start time-delay interrupt	15	9	4	4
33	CAN_DINT	Cancel time-delay interrupt	8	3	2	2
34	QRY_DINT	Query time-delay interrupt	7	2	1	1
35	MP_ALM	Trigger multicomputing interrupt	116	71	51	35
36	MSK_FLT	Mask synchronous error events	7	3	2	1
37	DMSK_FLT	Unmask synchronous error events	7	3	2	1
38	READ_ERR	Read event status register	7	3	2	1
39	DIS_IRT	Discard new events Block all events (MODE = 0)	61	38	23	13
		Block all events of an alarm class (MODE = 1)	9	7	3	3
		Block one event (MODE = 2)	7	7	2	2
40	EN_IRT	Stop discarding events Enable all events (MODE = 0)	53	31	19	13
		Enable all events of an alarm class (MODE = 1)	9	3	3	2
		Enable one event (MODE = 2)	7	3	2	2
41	DIS_AIRT	Delay interrupt events the first time the delay is activated [2]	47	26	17	11
		If the delay is already activated	6	3	2	1
42	EN_AIRT	If other delays are present	7	3	2	1
		Stop delaying interrupt events when last delay is canceled [3]	100	62	46	27
[2] When the delay is activated for the first time, the runtime of SFC 41 depends on the priority class in which SFC 41 is called. The specified runtime is based on the call in OB 1. It decreases as the priority class number increases. [3] When the delay is activated for the first time, the runtime of SFC 42 depends on the priority class in which SFC 42 is called. The specified runtime is based on the call in OB 1. It decreases as the priority class number increases.						
43	RE_TRIGR	Re-trigger cycle time monitoring	46	25	17	12
44	REPL_VAL	Transfer substitute value to ACCU 1	7	3	2	1
46	STP	Set CPU to STOP, cannot be measured	--	--	--	--
47	WAIT	Delay program execution in addition to waiting time	2	2	2	1

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
48	SNC_RTCB	Synchronize slave clocks	2	2	2	1
49	LGC_GADR	Find slot belonging to a logical address (central and PROFIBUS DP)	9	7	3	3
50	RD_LGADR	Find all logical addresses of a module (runtime entry for 1 DI 32 in central controller)	31	17	10	7
51	RDSYSST	"Module identification" sublist Read one data record (0111)	31	17	11	8
51	RDSYSST	"CPU characteristics" sublist Read all data records (0012)	62	38	24	15
		Read one data record (0112)	38	23	15	9
		Read header information (0F12)	24	15	9	6
51	RDSYSST	"Save" sublist Read one data record (0113)	32	18	12	9
51	RDSYSST	"System areas" sublist Read all data records (0014)	33	23	15	9
		Read header information (0F14)	24	15	9	6
51	RDSYSST	"Block types" sublist Read all data records (0015)	32	23	12	9
51	RDSYSST	"Status of module LEDs" sublist Read the status of all LEDs (0019)	62	39	25	17
		Read header information (0F19)	38	23	15	9
51	RDSYSST	"Component identification" sublist Read all components (001C)	53	32	22	15
		Read one component (011C)	32	23	15	9
		Read header information (0F1C)	30	16	10	7
51	RDSYSST	"Alarm status" sublist Read one data record (0222)	39	24	16	10
51	RDSYSST	"PIP/CPU assignment" sublist Assignment between all process image partitions and OBs (0025)	85	48	33	21
		Assignment between a process image partition and the corresponding OB (0125)	31	17	11	8
		Assignment of an OB to the corresponding process image partitions (0225)	69	39	26	16
		Read header information (0F25)	24	16	10	7
51	RDSYSST	"Communication "status information" sublist Read status information of a communication unit (0132)	39 – 68	23–39	16 – 25	10 – 16
		"Communication "status information" sublist Read status information of a communication unit (0232)	39	23	16	10

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	"Ethernet details of a module" sublist Read the Ethernet details of all Ethernet interfaces of a module (0037)	47	30	18	9
		Read the Ethernet details of an Ethernet interface (0137)	46	26	17	7
		Read header information (0F37)	46	30	17	7
51	RDSYSST	"Module LEDs" sublist Status of an LED (0174)	40	24	17	11
51	RDSYSST	"DP master system information" sublist All DP master systems known to the CPU (0090)	62	38	25	15
		One DP master system (0190)	35	28	13	9
		Read header information (0F90)	24	16	10	7
51	RDSYSST	"Module status information" sublist Read the status information of all plugged modules (n = number of data records) (0091)	213 + n * 16	130 + n * 13	86 + n * 10	56 + n * 7
		Read the status information of all modules/rack with the wrong type identifier (0191)	162 + n * 45	99 + n * 38	64 + n * 30	41 + n * 30
		All disrupted modules (0291)	169 + n * 60	93 + n * 49	62 + n * 38	39 + n * 30
		All modules that are not available (0391)	163 + n * 39	99 + n * 33	64 + n * 27	39 + n * 21
		All submodules of the host module (0591)	46	30	18	11
51	RDSYSST	Module status information of a DP master system (0991)	129 + n * 12	76 + n * 7	47 + n * 5	32 + n * 4
		Read the status information of a module with logical base address Central (0C91)	54	32	23	14
		Distributed on an integrated DP interface (0C91)	63	39	25	16
		Distributed on an integrated PNIO interface (0C91) [1]	60	36	24	-
		Distributed on an external PNIO interface (0C91) First call	86	54	37	21
		Intermediate call	61	39	27	14
		Last call	66	42	29	15
[1] Only for CPUs with integrated PNIO interface						

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	"Module status information" sublist of a distributed module connected to an external DP interface via the logical start address (4C91) First call	71	46	31	25
		Intermediate call	40	24	17	16
		Last call	47	30	18	17
		All modules in the specified rack (n = number of DR) (0D91)	84 + n * 23	51 + n * 16	30 + n * 10	18 + n * 8
		Distributed All modules of the specified DP station / specified IO device (0D91)	62 - 84	38 - 46	24 - 39	21 - 26
		All assigned modules (0E91)	207	130	86	55
		Header information (0F91)	107	63	42	28
51	RDSYSST	"Rack/station status information" sublist Centralized configuration Read the setpoint state of rack 0 (0092)	33	22	15	9
		Distributed configuration Read the setpoint state of DP system 1 (0092)	161	94	63	38
51	RDSYSST	Read the setpoint state of DP system 1 (via external DP interface) (4092) First call	62	39	24	15
		Intermediate call	31	18	11	8
		Last call	39	23	15	9
51	RDSYSST	Read the activation status of DP master system 1 (via integrated DP interface) (0192)	162	100	65	41
51	RDSYSST	Central Read the actual status of rack 0 (0292)	38	22	12	9
		Distributed configuration Read the actual status of DP system 1 (0292)	161	95	65	40
51	RDSYSST	Read the actual status of the stations of a DP master system (via external DP interface) (4292) First call	61	38	24	15
		Intermediate call	32	22	11	8
		Last call	39	24	16	10

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	Read the status of the battery buffer of rack 0 if at least one battery has failed (0392)	33	18	12	9
		Read the status of the entire battery buffer of a CPU (0492)	32	22	12	9
		Read the status of the 24 V supply of all racks of a CPU (0592)	37	22	12	9
51	RDSYSST	Centralized configuration Read the diagnostics status of the expansion devices (0692)	61	38	24	17
		Distributed configuration Read the diagnostics status of the stations of DP system 1 (via integrated DP interface) (0692)	193	115	77	46
		Diagnostics status of the stations of a DP master system that is connected via an external DP interface (4692) First call	61	38	24	15
		Intermediate call	38	18	12	8
		Last call	39	24	16	10
51	RDSYSST	"Rack/station status information" sublist Setpoint state of the central rack Centralized configuration (0094) Setpoint state of the stations of a DP station at an integrated interface (0094) Setpoint state of the stations of an IO controller system at an integrated interface (0094) [1] Setpoint state of the stations of a DP station at an external interface (0094) First call	37 121 320 76	23 76 195 59	19 47 132 40	12 32 - 27
		Intermediate call	54	40	28	19
		Last call	68	50	35	24
[1] Only for CPUs with integrated PNIO interface						
51	RDSYSST	Setpoint state of the stations of an IO controller system at an external interface (0094) First call	74	58	39	27
		Intermediate call	53	41	27	19
		Last call	68	51	34	24

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	Activation status of a station in an IO controller system that is configured and deactivated (0194) at an integrated interface [1]	83	46	32	-
		at an external interface First call	75	58	39	26
		Intermediate call	53	41	27	19
		Last call	69	52	34	24
[1] Only for CPUs with integrated PNIO interface						
51	RDSYSST	Actual status of central rack (0294)	38	23	20	12
		Actual status of the stations of a DP station connected to an integrated interface (0294)	136	84	51	34
		Actual status of the stations of an IO controller system at an integrated interface (0294) [1]	349	204	139	-
		Actual status of the stations of a DP station on an external interface (0294) First call	76	58	39	26
		Intermediate call	52	39	27	19
		Last call	68	51	33	24
51	RDSYSST	Actual status of the stations of an IO controller system at an external interface (0294) First call	75	58	38	27
		Intermediate call	52	42	27	19
		Last call	68	51	34	24
51	RDSYSST	Diagnostics status of the central rack (0694)	68	39	28	19
		Diagnostics status of the stations of a DP station at an integrated interface (0694) [1]	183	114	70	44
		Diagnostics status of the stations of an IO controller system at an integrated interface (0694)	370	222	150	-
		Diagnostics status of the stations of a DP station at an external interface (0694) First call	76	59	39	27
		Intermediate call	52	41	27	19
		Last call	70	54	32	25
[1] Only for CPUs with integrated PNIO interface						

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	Diagnostics status of the stations of an IO controller system at an external interface (0694) First call	74	58	38	26
		Intermediate call	52	42	27	19
		Last call	69	53	33	24
51	RDSYSST	Maintenance status of the central rack (0794)	168	100	67	37
		Maintenance status of the stations of a DP station at an integrated interface (0794)	182	107	70	45
		Maintenance status of the stations of an IO controller system connected to an integrated interface (0794) [1]	361	220	152	-
		Maintenance status of the stations of a DP station at an external interface (0794) First call	77	59	38	26
		Intermediate call	54	41	27	19
		Last call	69	52	31	24
		Maintenance status of the stations of an IO controller system at an external interface (0794) First call	75	58	39	27
		Intermediate call	52	41	26	19
		Last call	68	52	33	24
		Read header information (0F94) (central, DP station, and PROFINET IO)	31	23	14	10
[1] Only for CPUs with integrated PNIO interface						
51	RDSYSST	"Extended DP master system / PROFINET IO system information" sublist Read extended status information about a DP master system connected to an integrated or external interface and about a PROFINET IO system connected to an integrated interface (0195) [1]	38	23	15	9
		Read header information (0F95)	30	16	10	7
51	RDSYSST	"Module status information of all submodules of a specified module" sublist for PROFINET IO connected to an integrated interface (0696) [1]	55	34	24	-
[1] Only for CPUs with integrated PNIO interface						

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	Module status information of a module/sub-module located centrally or at a PROFIBUS DP/PROFINET interface (0C96)	2303	1437	949	550
		PROFIBUS DP via an integrated interface (0C96)	69	45	32	19
		PROFINET IO via an integrated interface (0C96) [1]	66	37	30	-
[1] Only for CPUs with integrated PNIO interface						
51	RDSYSST	PROFINET IO via external interface (0C96) First call	75	57	39	27
		Intermediate call	53	40	26	19
		Last call	69	52	32	24
51	RDSYSST	"Diagnostic buffer" sublist Read all event information that can be supplied in the current operating mode (max. 21) (00A0)	83	46	31	22
		Read the n latest entries (n = 1-23) (01A0)	32 + n * 2.0	22 + n * 1.1	12 + n * 0.9	8 + n * 0.6
		Read header information (0FA0)	30	26	10	7
51	RDSYSST	Information about all the tool changers and their tools on a PROFINET IO system (009C)	38	22	15	-
		Information about all the tool changers on a PROFINET IO system (019C)	37	23	15	-
		Information about a tool changer and its tools (029C)	40	25	16	-
		Information about a tool changer and its IO devices (039C)	40	25	16	-
		Only SSL sublist header information (0F9C)	38	22	14	-
51	RDSYSST	"Diagnostic data DR* 0" Read via logical start address (00B1) Central	108	76	54	44
		PROFIBUS DP (00B1) First call	83	52	35	21
		Intermediate call, REQ = 0	40	25	16	11
		Last call	47	28	21	12
51	RDSYSST	"Diagnostics data DR 1" sublist Read via physical address (00B2) Read a 16-byte long DR 1	102	66	53	41

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
51	RDSYSST	"Diagnostics data DR* 1" sublist Read via logical start address (00B3) Read a 16-byte long DR 1 Centralized configuration	167	119	99	80
		PROFIBUS DP (00B3) First call	84	54	36	21
		Intermediate call	40	26	16	11
		Last call	54	29	21	13
51	RDSYSST	"Diagnostics data DP slave" sublist Read via configured diagnostic address (00B4) First call	86	52	34	21
		Intermediate call, REQ = 0	46	31	17	11
		Last call (6 – 240 bytes)	70	49	30	13
52	WR_USMSG	Write user entry in diagnostics buffer with message	25	17	11	7
		Without message	23	16	10	7
54	RD_DPARM	Read dynamic parameters, centralized configuration, AI 8 * 13 bits	39	24	15	9
		PROFIBUS DP AI 8 * 12 bits (DR1 = 14 bytes)	46	26	17	11
55	WR_PARM	Write dynamic parameters, central AI 8 * 13 bits	129	92	70	60
		PROFIBUS DP First call AI 8 * 12 bits (14 – 240 bytes)	84	47	32	20
		Follow-up/last call, REQ = 0	38	23	15	9
56	WR_DPARM	Write predefined dynamic parameters, AI 8 * 13 bits centralized configuration	176	124	111	98
		PROFIBUS DP First call AI 8 * 12 bits (2 - 240 Bytes)	68	39	25	16
		Follow-up/last call	31	17	11	8
57	PARM_MOD	Assign module parameters, centralized configuration Module/DR count/DR lengths in bytes AI 8 * 13 bits	299	217	194	171
		PROFIBUS DP AO 8 * 12 bits First call (16 - 240 bytes)	68	39	25	16
		Follow-up/last call	31	17	11	8

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
58	WR_REC	Write parameter data record centralized configuration (n = number of bytes)	69 + n * 2.6	48 + n * 2.4	40 + n * 2.3	28 + n * 2.2
		First call, integrated DP interface (n = number of bytes)	76 + n * 0.1	42 + n * 0.1	27 + n * 0.1	18 + n * 0.1
		Intermediate call, REQ = 0, integrated DP interface	30	16	10	7
		Last call, integrated DP interface	31	17	11	8
		First call, external DP interface (n = number of bytes)	76 + n * 0.1	42 + n * 0.1	27 + n * 0.1	18 + n * 0.1
		Intermediate call, REQ = 0, external DP interface	30	16	10	7
		Last call, external DP interface	31	18	11	8
59	RD_REC	Read data record first call, centralized configuration (n = number of bytes)	79 + n * 2.8	52 + n * 2.4	40 + n * 2.3	31 + n * 2.2
		First call, integrated DP interface module	70	48	30	19
		Intermediate call, REQ = 0, integrated DP interface module	31	15	11	7
		Last call, integrated DP interface (n = number of bytes)	61 + n * 0.07	34 + n * 0.07	23 + n * 0.07	19 + n * 0.07
		First call, external DP interface	70	48	30	19
		Intermediate call, REQ = 0, external DP interface	31	15	11	7
		Last call, external DP interface (n = number of bytes)	61 + n * 0.1	34 + n * 0.08	23 + n * 0.07	14 + n * 0.04
60	GD_SEND	Send GD packet 1 byte	43	33	19	12
		32 bytes	110	70	46	27
61	GD_RCV	Accept GD packet (1-32 bytes)	21	15	9	6
62	CONTROL	Query the status of the connection belonging to a local communication SFB instance	31	17	11	8
64	TIME_TCK	Read out millisecond timer	2	2	1	1
65	X_SEND	Send data to external partner First call, establish connection (1-76 bytes) REQ = 1	207	153	123	88
		First call connection available (1-76 bytes)	101	68	41	32
		Intermediate call (1-76 bytes)	39	24	16	10
		Last call, BUSY = 0	46	25	17	10

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
66	X_RCV	Receive data from external partner Verify reception (1-76) bytes	24	21	19	14
		Read data (1-76 bytes)	77	66	58	42
67	X_GET	Read data from external partner First call, establish connection (1-76 bytes) REQ = 1	192	145	116	84
		First call connection available (1-76 bytes)	92	68	54	48
		Intermediate call (1-76 bytes)	39	24	16	10
		Last call, BUSY = 0	69	40	17	10
68	X_PUT	Write data to external partner First call, establish connection (1-76 bytes) REQ = 1	214	148	123	88
		First call connection available (1-76 bytes)	108	72	63	50
		Intermediate call (1-76 bytes)	39	24	16	10
		Last call, BUSY = 0	46	25	17	10
69	X_ABORT	Abort connection to external partner, first call, REQ = 1	62	52	41	29
		Intermediate call	30	22	18	10
		Last call, BUSY = 0	123	99	87	67
70	GEO_LOG	Determine the start address of a module from its slot	15	9	7	4
71	LOG_GEO	Determine the slot that belongs to a logical address	16	9	7	4
72	I_GET	Read data from internal partner, first call, establish connection (1-76 bytes) REQ = 1	207	147	122	88
		First call connection available (1-76 bytes)	92	62	37	24
		Intermediate call (1-76 bytes)	45	24	16	10
		Last call, BUSY = 0	76	41	27	18
73	I_PUT	Write data to internal partner, first call, establish connection (1-76 bytes) REQ = 1	223	162	131	92
		First call connection available (1-76 bytes)	108	70	46	27
		Intermediate call (1-76 bytes)	45	24	16	10
		Last call, BUSY = 0	52	30	18	11

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
74	I_ABORT	Abort connection to internal partner, first call, REQ = 1	62	38	23	15
		Intermediate call	31	21	11	7
		Last call, without / with connection, BUSY = 0	124	100	31	27
78	OB_RT	Determine the OB program runtime	15	8	4	3
79	SET	Set bit array in the I/O area, n = number of bits to be set to 1	14 +n * 0.6	8 + n * 0.4	6 + n * 0.25	4 +n * 0.25
80	RSET	Delete bit array in the I/O area n = number of bits to be set to 0	15 +n * 0.6	8 +n * 0.4	6 + n * 0.25	4 +n * 0.25
81	UBLKMOV	Copy variable without interruption, n = number of bytes to be copied	14 + n* 0.01	8 + n* 0.009	3 + n * 0.008	3 + n* 0.008
87	C_DIAG	Determine current connection status MODE = 0	4	2	2	2
		Mode = 1, 2, 3	93	76	72	55
99	WWW	Enable or synchronize user websites	195	124	99	-
100	SET_CLKS	Set time-of-day and TOD status MODE = 1	46	30	18	12
		MODE = 2	24	15	9	6
		MODE = 3	47	30	18	12
101	RTM	Handle operating hours counter, Mode = 0 Read	15	8	3	3
		Mode = 1, 2 Start/Stop	15	8	3	3
		Mode = 4, 5, 6 Set	15	8	4	3
103	DP_TOPOL	Determine the bus topology in a DP master system, first call, REQ = 1	68	39	25	16
		Intermediate call	12	7	5	2
		Last call, BUSY = 0	12	10	7	3
104	CIR	Control CiR, MODE = 0, Information	7	3	2	1
		MODE = 1, Enable CiR	7	3	2	1
		MODE = 2, Disable CiR completely	7	3	2	1
		MODE = 3, Disable CiR conditionally	7	3	2	1
105	READ_SI	Read dynamically assigned system resources, MODE = 0	31 - 782 [1]	23 - 491 [1]	13 – 383 [1]	8 - 242 [1]
		MODE = 1	38 - 891 [2]	23 - 599 [2]	13 – 599 [2]	9 - 370 [2]
		MODE = 2	38 - 952 [2]	23 - 930 [2]	13 – 1882 [2]	9 - 1131 [2]
		MODE = 3	38 - 875 [3]	23 - 586 [3]	15 – 829 [3]	9 - 366 [3]

SFC no.	SFC name	Description	Execution time in µs			
			412	414	416	417
106	DEL_SI	Enable dynamically assigned system resources, MODE = 1 2)	46 - 752 1)	25 - 717 1)	16 – 1369 1)	10 - 827 1)
		MODE = 2 2)	46 - 722 1)	26 - 684 1)	17 - 1417 1)	11 - 855 1)
		MODE = 3 3)	45 - 745 2)	25 - 712 2)	16 – 1360 2)	10 - 821 2)
1) Depending on the size of the SYS_INST target area and the number of system resources still to be read 2) Depending on the number of active messages (assigned system resources) 3) Depending on the number of active messages (assigned system resources) and the number of assigned instances with the searched CMP_ID.						
107	ALARM_DQ	Generate block-related messages that can be acknowledged, first call, SIG = 0 -> 1	84 + n * 2.2	56 + n * 1.3	38 + n + 1.1	24 + n * 0.6
		Empty call	38 + n * 2.2	18 + n * 1.3	14 + n * 1.1	8 + n * 0.6
108	ALARM_D	Generate block-related messages that cannot be acknowledged, first call, SIG = 0 -> 1	88 + n * 2.2	58 + n * 1.3	40 + n * 1.1	31 + n * 0.6
		Empty call	38 + n * 2.2	18 + n * 1.3	14 + n * 1.1	8 + n * 0.6
109	PROTECT	Activate write protection	2	2	2	1
112	PN_IN 1)	Update inputs of the user program interface of the PROFINET CBA component	< 6979	< 5850	< 4038	-
113	PN_OUT 1)	Update outputs of the user program interface of the PROFINET CBA component	< 5895	< 4893	< 3635	-
114	PN_DP 1)	Update DP interconnections	< 1486	< 1218	< 1015	-
1) Only for the CPUs 412-2 PN, 414-3 PN/DP, 416-3 PN/DP, 416F-3 PN/DP. The execution times of these blocks depend on their respective interconnection configuration and the size of the interface DBs. Please also note the section "CBA response times" in the Product Manual Automation System S7-400CPU Data.						
126	SYNC_PI	Update process image partition of inputs in isochronous mode	27	20	15	12
127	SYNC_PO	Update process image partition of outputs in isochronous mode	26	19	14	12

3.34 System Function Blocks (SFB)

The following table lists the system function blocks supplied by the operating system of the S7-400 CPUs and the execution times on the respective CPU.

SFB no.	SFB name	Description	Execution time in µs			
			412	414	416	417
0	CTU	Count up	1	1	1	1
1	CTD	Count down	1	1	1	1
2	CTUD	Count up and down	1	1	1	1
3	TP	Generate pulse	7	2	2	2
4	TON	Generate ON delay	7	2	2	1
5	TOF	Generate OFF delay	7	5	4	1
8	USEND	Send data uncoordinated (one send parameter supplied) JOB activation (1-440 bytes)	107	68	40	28
		JOB checked	39	23	15	9
		JOB finished, DONE = 1	39	23	15	9
9	URCV	Receive data without coordination (one receive parameter supplied) JOB activation	37	22	14	9
		JOB checked	32	22	12	8
		JOB finished (NDR = 1; 1-440 bytes)	77	46	32	21
12	BSEND	Send data block by block JOB activation (1-3000 bytes)	99	56	39	23
		JOB checked	39	23	16	10
		JOB finished, DONE = 1	39	23	16	10
13	BRCV	Receive data block by block JOB activation (1-3000 bytes)	52	30	18	12
		JOB checked	46	25	16	11
		JOB finished	44	24	16	10
14	GET	Read data from remote CPU (one area specified) JOB activation	91	49	35	20
		JOB checked	39	23	15	9
		JOB finished (NDR = 1 (1-450 bytes)	76	46	36	22
15	PUT	Write data to remote CPU (one area specified) JOB activation (1-404 bytes)	114	68	47	29
		JOB checked	39	23	15	9
		JOB finished, DONE = 1	39	23	15	9
16	PRINT	Send data to a printer Job activation, REQ = 1	124	70	53	32
		JOB checked	39	23	16	9
		JOB finished, DONE = 1	39	23	16	9

SFB no.	SFB name	Description	Execution time in µs			
			412	414	416	417
19	START	Perform warm restart or cold restart in remote device Job activation, REQ = 1	108	69	45	26
		JOB checked	39	23	16	10
		JOB finished, DONE = 1	39	23	16	10
20	STOP	Set remote device to STOP Job activation, REQ = 1	100	64	43	25
		JOB checked	39	24	16	10
		JOB finished, DONE = 1	39	24	16	10
21	RESUME	Perform hot restart in remote device Job activation, REQ = 1	107	69	44	25
		JOB checked	39	24	16	10
		JOB finished, DONE = 1	39	24	16	10
22	STATUS	Query device status of a remote partner, JOB activation, REQ = 1	63	41	26	16
		JOB checked	38	23	15	9
		JOB finished, NDR = 1	101	62	40	25
23	USTATUS	Receive status of remote device without coordination, JOB activation, NDR = 1	32	22	15	8
		JOB checked	32	17	15	8
		JOB finished	106	62	40	25
31	NOTIFY_8P	Generate block-related message without acknowledgment display First call or JOB activation, SIG = 0-> 1 (1-420 bytes)	138	99	57	35
		JOB checked	54	32	19	12
		JOB finished, DONE = 1	54	32	22	13
32	DRUM	Implement sequencer	14	3	2	2
33	ALARM	Generate block-related message with acknowledgment display First call or JOB activation, SIG = 0 → 1 (1-420 bytes)	131	83	52	35
		JOB checked	54	31	19	13
		JOB finished, DONE = 1	55	32	22	13
34	ALARM_8	Generate block-related message without associated value for 8 signals, first call or JOB activated, SIG = 0-> 1 (1-420 bytes)	103	63	41	26
		JOB checked	49	31	20	13
		JOB finished, DONE = 1	54	36	22	13
35	ALARM_8P	Generate block-related message with associated value for 8 signals, first call or JOB activation, SIG = 0-> 1 (1-420 bytes)	131	78	59	35

SFB no.	SFB name	Description	Execution time in µs			
			412	414	416	417
		JOB checked	51	31	19	13
		JOB finished, DONE = 1	54	32	22	13
36	NOTIFY	Generate block-related message without acknowledgment display, first call or JOB activation, SIG = 0-> 1 (1-420 bytes)	139	79	56	35
		JOB checked	52	31	19	12
		JOB finished, DONE = 1	52	32	22	13
37	AR_SEND	Send archive data First call or JOB activation, REQ = 1 (1-3000 bytes)	105	66	44	26
		JOB checked	46	25	17	10
		JOB finished, DONE = 1	46	25	17	10
52	RDREC	Read data record from a central module	107	70	61	42
52	RDREC	Read data record from a DP slave integrated DP interface, first call (2 - 16 bytes)	84	45	30	21
		Intermediate call	31	17	11	8
		Last call	38	22	15	8
52	RDREC	Read data record from a DP slave external DP interface, first call (4 - 16 bytes)	84	41	30	18
		Intermediate call	31	17	11	8
		Last call	37	22	14	8
52	RDREC	Read data record from an IO device, integrated PROFINET interface,[1] First call (2-16 bytes)	81	45	31	-
		Intermediate call	37	22	15	-
		Last call	37	22	15	-
[1] Only for CPUs with integrated PNIO interface						
52	RDREC	Read data record from an IO device, external PROFINET interface, first call (2-16 bytes)	80	43	32	20
		Intermediate call	33	18	12	9
		Last call	39	24	15	9
53	WRREC	Centralized configuration	107	70	55	38
53	WRREC	Write data record to a DP slave, integrated DP interface First call (1-10 bytes)	84	47	31	20
		Intermediate call	32	17	14	8
		Last call	37	22	15	8

SFB no.	SFB name	Description	Execution time in µs			
			412	414	416	417
53	WRREC	Write data record to a DP slave, external DP interface First call (2-14 bytes)	82	47	31	19
		Intermediate call	32	17	11	8
		Last call	38	22	15	8
53	WRREC	Write data record to an IO device, integrated PROFINET interface[1)] First call (1-10 bytes)	86	55	34	-
		Intermediate call	36	22	15	-
		Last call	36	22	15	-
[1)] Only for CPUs with integrated PNIO interface						
53	WRREC	Write data record to IO device, external PROFINET interface, first call (2-24 bytes)	83	48	32	19
		Intermediate call	38	22	15	8
		Last call	38	22	15	8
54	RALRM	Receive interrupt from a DP slave or IO device, runtime measurement for OBs not connected to I/O, MODE = 1, OB 1	30	18	13	8
54	RALRM	Receive interrupt from a DP slave or IO device, runtime measurement on central I/O, MODE = 1, OB 40, OB 83, OB 86	71	50	31	19
		OB 55 to OB 57, OB 82	74	54	33	21
54	RALRM	Receive interrupt from a DP slave or IO device, runtime measurement on integrated DP or PROFINET interface, MODE = 1, OB 40, OB 83, OB 86	90	51	34	21
		OB 55 to OB 57, OB 82	96	55	37	23
54	RALRM	Receive interrupt from a DP slave or IO device, runtime measurement on external DP or PROFINET interface, MODE = 1, OB 40, OB 83, OB 86	168	119	90	68
		OB 55 to OB 57, OB 82	213	174	135	106
81	RD_DPAR	Read predefined parameters, central	75	46	31	19
81	RD_DPAR	Read predefined parameters, internal DP	-	46	31	19

SFB no.	SFB name	Description	Execution time in µs			
			412	414	416	417
81	RD_DPAR	Read predefined parameters, external DP, First call	83	60	35	24
		Last call	83	60	35	24
81	RD_DPAR	Read predefined parameters PNIO [1] First call	104	62	40	-
		Intermediate call	104	72	47	-
		Last call	39	24	26	-
[1] This is only possible via an external PNIO interface at all CPUs except CPU 412-2 PN, CPU 414-3 PN/DP, 416-3 PN/DP and 416F-3 PN/DP.						
104	IP_CONF	Create an IP configuration First call	40	28	17	-
		Last call	44	30	19	-

3.35 Function Blocks for Open Communication via Industrial Ethernet

The following tables list the function blocks for open communication via Industrial Ethernet provided by the operating system of the S7-400 CPUs and the execution times on the respective CPU.

FB no.	FB name	Description	Execution time in µs			
			412	414	416	417
63	TSEND [1]	Send data via TCP and ISO on TCP (n bytes) First call	84 + n*0.014	52 + n*0.01	34 + n*0.008	21 + n*0.006
		Intermediate call	32	23	15	9
		Last call	32	23	15	9
64	TRCV [1]	Receive data via TCP and ISO on TCP (n bytes) First call	75	45	31	19
		Intermediate call	38	23	15	9
		Last call	61	33	24	15
[1] The "TCP" protocol is only supported by the CPUs with PN/IO interface.						
65	TCON	Establish connection First call	82	52	33	21
		Intermediate call	30	20	9	6
		Last call	30	20	10	7
66	TDISCON	Terminate connection First call	58	33	23	13
		Intermediate call	24	20	9	6
		Last call	30	21	10	7
67	TUSEND	Send data via UDP (n bytes) First call	98 + n*0.014	60 + n*0.01	40 + n*0.008	26 + n*0.008
		Intermediate call	38	23	15	9
		Last call	39	23	15	9
68	TURCV	Receive data via UDP First call	76	46	37	19
		Intermediate call	38	23	15	9
		Last call	81	46	24	23

3.36 IEC Functions

You can use the following IEC functions in STEP 7.

These blocks are saved in the standard library, IEC Function Blocks of STEP 7.

FC no.	FC name	Description
DATE_AND_TIME		
3	D_TOD_DT	Combines the data formats DATE and TIME_OF_DAY (TOD) and converts to data format DATE_AND_TIME.
6	DT_DATE	Extracts the DATE data format from the DATE_AND_TIME data format.
7	DT_DAY	Extracts the day of the week from the DATE_AND_TIME data format.
8	DT_TOD	Extracts the TIME_OF_DAY data format from the DATE_AND_TIME data format.
Time formats		
33	S5TI_TIM	Converts S5 TIME data format to TIME data format.
40	TIM_S5TI	Converts TIME data format to S5 TIME data format.
Duration		
1	AD_DT_TM	Add a duration in TIME format to a point in time in DT format; the result is a new point in time in DT format.
35	SB_DT_TM	Subtract a duration in TIME format from a point in time in DT format; the result is a new point in time in DT format.
34	SB_DT_DT	Subtract two points in time in DT format; the result is a duration in TIME format.
Compare DATE_AND_TIME		
9	EQ_DT	Compares the contents of two variables in the DATE_AND_TIME format for equal to.
12	GE_DT	Compares the contents of two variables in the DATE_AND_TIME format for greater than or equal to.
14	GT_DT	Compares the contents of two variables in the DATE_AND_TIME format for greater than.
18	LE_DT	Compares the contents of two variables in the DATE_AND_TIME format for less than or equal to.
23	LT_DT	Compares the contents of two variables in the DATE_AND_TIME format for less than.
28	NE_DT	Compares the contents of two variables in the DATE_AND_TIME format for unequal to.
Compare STRING		
10	EQ_STRNG	Compares the contents of two variables in the STRING format for equal to.
13	GE_STRNG	Compares the contents of two variables in the STRING format for greater than or equal to.
15	GT_STRNG	Compares the contents of two variables in the STRING format for greater than.
19	LE_STRNG	Compares the contents of two variables in the STRING format for less than or equal to.
24	LT_STRNG	Compares the contents of two variables in the STRING format for less than.
29	NE_STRNG	Compares the contents of two variables in the STRING format for unequal to.
Processing STRING variables		
21	LEN	Reads out the actual length of a STRING variable.
20	LEFT	Reads the first L character of a STRING variable.
32	RIGHT	Reads the last L character of a STRING variable.
26	MID	Reads the center L character of a STRING variable. (starting from the defined character).
2	CONCAT	Combines two STRING variables in one STRING variable.
17	INSERT	Inserts a STRING variable into another STRING variable at a defined point.
4	DELETE	Deletes L characters of a STRING variable.

FC no.	FC name	Description
31	REPLACE	Replaces L characters of a STRING variable with a second STRING variable.
11	FIND	Finds the position of the second STRING variable in the first STRING variable.
Format conversions with STRING		
16	I_STRNG	Converts a variable from INTEGER format to STRING format.
5	DI_STRNG	Converts a variable from INTEGER (32bit) format to STRING format.
30	R_STRNG	Converts a variable from REAL format to STRING format.
38	STRNG_I	Converts a variable from STRING format to INTEGER format.
37	STRNG_DI	Converts a variable from STRING format to INTEGER (32bit) format.
39	STRNG_R	Converts a variable from STRING format to REAL format.
Processing of numbers		
22	LIMIT	Limits a number to a defined limit value.
25	MAX	Selects the largest of three numerical variables.
27	MIN	Selects the smallest of three numerical variables.
36	SEL	Selects one of two variables.

SSL partial list

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SSL ID	Index	Message function
		Module identification
0111_H		Identification data record corresponding to the specified index
	0001_H	CPU type and version number
	0006_H	Identification of basic hardware
	0007_H	Identification of basic firmware
		CPU characteristics
0012_H	–	All characteristics
0112_H		Characteristics of a group
	0000_H	STEP 7 processing
	0100_H	Time system in the CPU
	0200_H	System behavior of the CPU
	0300_H	STEP 7 instruction supply
$0F12_H$	–	Header information only
		User memory areas
0013_H	–	All data records of available user memory areas
0113_H		One data record for the specified memory area
	0001_H	Work memory
		System areas
0014_H	–	Data records of all system areas
$0F14_H$	–	Header information only
		Block types
0015_H	–	Data records of all block types
		Status of the module LEDs
0019_H	–	Read the status of all LEDs
$0F19_H$	–	Header information only
		Component identification
$001C_H$	–	Read all data records
$011C_H$		Data record for specified index
	0001_H	Station name
	0002_H	Name of the module
	0003_H	Plant ID of the module
	0004_H	Copyright entry
	0005_H	Serial number of the module
	0007_H	Module type name
	0008_H	Serial number of the micro memory card
	0009_H	Manufacturer and profile of a CPU module
	$000A_H$	OEM identifier

SSL ID	Index	Message function
	$000B_H$	Location ID
$0F1C_H$	–	Header information only
		Interrupt status
0222_H		Data record for specified interrupt
	OB no.	Number of the OB (OB1 only)
		Assignment between process image partitions and CPUs (only for CPUs that support synchronous cycle)
0025_H	–	Assignment of all partial process images and OBs
0125_H	PIP no. (number of the process image partition)	Assignment of a partial process image to the corresponding OB
0225_H	OB no.	Assignment of an OB to the corresponding partial process images
$0F25_H$	–	Only SSL sublist header information
		Communication status data
0132_H		Communication status information on the specified communication unit (only one data record)
	0004_H	OMS/contactor
	0005_H	Diagnostics
	0008_H	Time system (TIME)
	$000B_H$	Runtime meter (32 bit) 0 to 7
	$000C_H$	Runtime meter (32 bit) 8 to 15
0232_H		Communication status information on specified communication unit
	0004_H	OMS/contactor
		Status of the module LEDs
0074_H	–	Read the status of all LEDs
0174_H		Read the status of individual LEDs
	0001_H	GE, group error
	0004_H	RUN, RUN LED
	0005_H	STOP, STOP LED
	0006_H	FRCE, Force LED
	$000B_H$	BF1 LED
	$000C_H$	BF2 LED
	0014_H	BF3 LED
	0015_H	MAINT LED
		DP master system information
0090_H	0000_H	Information DP master systems known to the CPU
0190_H	DP master system ID	Information about a DP Master system
$0F90_H$	0000_H	Only SSL sublist header information
		Module status information (27 data records are supplied as a maximum)
0037_H		Details of all Ethernet interfaces of a module
0137_H		Details of an Ethernet interface
$0F37_H$		Header information
0091_H		Status information of all modules/sub-modules inserted

SSL ID	Index	Message function
0191_H		Status information of all modules/racks with the wrong type identifier
0291_H		Module status information of all disrupted modules
0391_H		Module status information of all unavailable modules
0591_H	–	Module status information for all submodules that a host recognizes
0991_H		Module status information of a DP master system
$0A91_H$	–	Module status information of all DP master systems known to the CPU (only CPUs with DP interface)
$0C91_H$		Module status information of a module in a central configuration or on an integrated DP interface or on an internal PROFINET interface
$4C91_H$		Module status information of a module on an external DP interface or on an external PROFINET interface
	Any logical address of a module/submodule	Module status information of a module via logical address
$0D91_H$		Module status information of a rack or station
	Centralized configuration: 0000_H: Rack 0 0001_H: Rack 1 0002_H: Rack 2 0003_H: Rack 3 **PROFIBUS DP:** $xxyy_H$: DP subnet ID/station no. **PROFINET IO:** Slot address of PROFINET IO device: Bit 15: is always = 1 Bit 11-14: PN IO subsystem ID (value range 100-115; in which only 0 to 15 must be specified) Bit 0-10: Station number of the PROFINET IO device	Module status information of all modules in the specified rack/station
$0E91_H$		Module status information of all assigned modules
		Rack/station status information
0092_H		Setpoint state of the rack in the central configuration or stations of a subnet
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID	Information about the state of the stations in the subnet
4092H		Setpoint state of the stations of an DP master system connected via an external DP interface
0192_H		Activation status of the stations in a DP master system that is connected via an integrated DP interface
0292_H		Actual state of the rack in the central configuration or stations of a subnet
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID	Information about the state of the stations in the subnet
0292_H		Status of the backup batteries in a rack of a CPU after at least one battery has failed

SSL ID	Index	Message function
0292_H		Status of the overall battery backup status of all racks/module racks of a CPU
0292_H		Status of the 24-V power supply to all racks/module racks of a CPU
4292_H		Actual status of the stations of a DP master system that is connected via an external DP interface module
0392_H		Status of the backup batteries in a rack/module rack of a CPU after at least one battery has failed
0492_H		Status of the overall battery backup status of all racks/module racks of a CPU
0592_H		Status of the 24-V power supply to all racks of a CPU
0692_H		Diagnostic state of the rack in the central configuration or stations of a subnet
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID	Information about the state of the stations in the subnet
4692_H		Diagnostics status of the stations of a DP master system connected via an external DP interface.
		Rack/station status information
0094_H		Setpoint state of the rack in the central configuration or stations of a subnet
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID or PN IO subsystem no.	Information about the state of the stations in the subnet
0194_H		Activation status of station in an IO controller system that is configured and deactivated
0294_H		Actual state of the rack in the central configuration or stations of a subnet
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID or PN IO subsystem no.	Information about the state of the stations in the subnet
0694_H		Diagnostic state of the rack in the central configuration or stations of a subnet
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID or PN IO subsystem no.	Information about the state of the stations in the subnet
0794_H		Faulty- and/or maintenance status of station
	0000_H	Information about the state of the rack in the central configuration
	DP master system ID or PN IO subsystem no.	Information about the state of the stations in the subnet
$0F94_H$	–	Header information only
		Extended DP master system information
0195_H	$xxyy_H$: DP master system ID/00_H	Extended DP master system information of a DP master system (only CPUs with DP interface)
$0F95_H$	–	Header information only (only CPUs with DP interface)

SSL ID	Index	Message function
		Submodule status information
0696$_H$	Any logical address of a module/submodule	Status data of all submodules of a module
0C96$_H$	Any logical address of a module/submodule	Status data of a submodule
		ToolChanger information (only for CPUs with PN interface)
009C$_H$		Information about all tool changers and their tools in a PN IO subsystem
019C$_H$		Information about all tool changers
029C$_H$		Information about a tool changer and its tools
039C$_H$		Information about a tool and its IO device
0F9C$_H$		only header information
		Diagnostics buffer
00A0$_H$		All input event information (in the RUN of CPU default mode outputs only 10 entries; the number of event information output in RUN can be parameterized from 10 - 499)
01A0$_H$	x	The "x" most recent input event information
0FA0$_H$	–	Header info SSL only
		Diagnostic data on modules
00B1$_H$	Any logical address of a module/submodule	The first four diagnostic bytes of a module (diagnostics data record DS0)
00B2$_H$	Rack and slot number	All diagnostics data of a module (diagnostics data record DS1-only for centrally mounted modules)
00B3$_H$	Any logical address of a module/submodule	All diagnostics data of a module (diagnostics data record DS1)
00B4$_H$	Logical basic address (diagnosis address of the slave)	Standard diagnostics data of a DP slave (only CPUs with DP interface)