SIEMENS

Counter Module 6ES5-424

Technical Reference Manual Version 18. 10. 1986

Preface

This document provides detailed hardware and software information on the 6ES5-242 Counter Module. The types of information and their locations within this manual are listed below.

Chapter 1 Hardware Description

This chapter presents a general description of the module and the two LSI chips that perform all counting and interrupt functions. Also, a general description of each of the registers contained in the counter chip, the interrupt chip and the remaining registers of the module is given.

Chapter 2 Module Setup

Information concering initial setup, switch setting and jumper configurations is provided. Specifications on the module's I/O, as well as pin configurations for the five front connectors, are also included. The final portion in this chapter contains the module's memory map.

Chapter 3 Register Description and Use

Coverage examines manipulation of the module's internal registers. A description of each of the available counting modes is also presented.

Chapter 4 Standard Software Function Blocks

The two standard function blocks available for the 6ES5 242 module, FB158 and FB159, are examined. Function block parameters are listed and explained in detail. The chapter closes with a few helpful programming hints so you can manipulate the module's firmware.

Contents

		Page
Chapter 1 Hardware Description		
1.1	**General Description**	**42**
1.1.1	Gate Control	42
1.1.2	Inputs	42
1.1.3	Outputs	42
1.1.4	Interrupt	42
1.1.5	Scaler 1	42
1.1.6	Scaler 2	42
1.2	**6ES5 - 242 Block Diagram**	**42**
1.3	**The AM 9513 Counter Chip**	**43**
1.3.1	Master Mode Register (AM 9513)	43
1.3.2	Counter Mode Register (AM 9513)	43
1.3.3	Load Register (AM 9513)	43
1.3.4	Hold Register (AM 9513)	43
1.3.5	Alarm Register (AM 9513)	43
1.4	**6ES5 - 242 Module Registers**	**43**
1.4.1	Control Register	43
1.4.2	Function Number Register	43
1.4.3	Interrupt Mask Register	44
1.4.4	Interrupt Information Register	44
1.4.5	Error Signal Register	44
1.4.6	Result of Counter Register	44
Chapter 2 Module Setup Procedures		
2.1	**Switch S1 - Addressing**	**45**
2.2	**Switch S2 Group Interrupts**	**45**
2.3	**Switch S3 - System Interrupts**	**46**
2.4	**Switch S4 - Gate Signal Conditioning**	**47**
2.5	**Switch S5 - Counter Input Routing**	**47**
2.6	**Switch S6 - Gate Input Routing**	**47**
2.7	**Jumper Assignmets**	**47**
2.8	**Inputs and outputs**	**48**
2.8.1	Plug Connectors	48
2.8.2	Counter and Gate Inputs	48
2.8.3	Counter Outputs	49
2.8.4	Signal Conditioning	49
2.9	**Module Pin Out**	**50**
2.10	**6ES5 - 242 Module Memory Map**	**50**
Chapter 3 Register Details and Use		
3.1	**INTM - Interrupt Mask Register (AM 9519)**	**51**
3.2	**INTI -Interrupt Information Register**	**51**
3.3	**MM - Master Mode Register (AM 9513)**	**52**
3.3.1	Real - Time Clock: MM1 - MM0	52
3.3.2	Comparators 1 and 2: MM3 - MM2	52
3.3.3	Scaler 2 (FOUT) Pulse Source: MM7 - MM4	52
3.3.4	Scaler 2 (FOUT) Scaling Factor: MM11 - MM8	52
3.3.5	Scaler 2 (FOUT) Enable: MM12	53
3.3.6	Scaler 1 Counting Mode: MM15	53
3.3.7	Bits MM14 and MM13	53
3.4	**CM-Counter Mode Register (AM 9513)**	**53**
3.4.1	Output Selection: CM2 - CM0	53
3.4.2	Counting Direction: CM3	54
3.4.3	Counting Mode: CM4	54
3.4.4	Counting Type: CM5	54
3.4.5	Reloading Selection: CM6	54
3.4.6	Special Function Enable: CM7	54
3.4.7	Pulse Source Selection: CM11 - CM8	54
3.4.8	Cascading Counters	54
3.4.9	Pulse Edge Selection: CM12	54
3.4.10	Gate Control Selecion: CM15 - CM13	54
3.5	**Counter Modes**	**55**
3.5.1	Mode A	55
3.5.2	Mode B	55
3.5.3	Mode C	55
3.5.4	Mode D	55
3.5.5	Mode E	55
3.5.6	Mode F	55
3.5.7	Mode G	56
3.5.8	Mode H	56
3.5.9	Mode I	56
3.5.10	Mode J	56
3.5.11	Mode K	56
3.5.12	Mode L	56
3.5.13	Mode N	57
3.5.14	Mode O	57
3.5.15	Mode Q	57
3.5.16	Mode R	57
3.5.17	Mode S	57
3.5.18	Mode V	58
3.5.19	Mode X	58
3.6	**CTRL - Control Register**	**58**
3.6.1	Control Words: CTRL7 - CTRL5	58
3.6.2	Additional Functions	59
3.6.3	Counter Selection: CTRL4 - CTRL0	59
3.7	**FNR - Function Number Register**	**59**
3.8	**FEM - Error Signal Register**	**59**
3.8.1	Error Descriptions	60
3.9	**Ex - Results of Counter Registers**	**60**
Chapter 4 Standard Software		
4.1	**Function Block 158**	**61**
4.1.1	Organization Blocks for 158	61
4.1.2	Explanation of FB 158	61
4.1.3	Parameter BGDB	61
4.1.4	Parameter P/Q	61
4.1.5	Parameter PAFE	61
4.1.6	Parameter BFEH	61
4.1.7	Parameter SFEH	61
4.2	**Function Block 159**	**61**
4.2.1	Explanation of FB 159	62
4.2.2	Parameter BG	62
4.2.3	Parameter PQ	62
4.2.4	Parameters Z4-1 and Z--5	62
4.2.5	Parameter BEF	62
4.2.6	Parameter DBDW	63
4.2.7	Parameter INTL	63
4.2.8	Parameter FEML	63
4.2.9	Parameter PAFE	63
4.3	**Standard Software Data Blocks**	**64**
4.4	**FB 159 Usage**	**64**
4.4.1	Access Time	64
4.4.2	MM and INTM Registers	64
4.4.3	Alarms Registers	65
	Appendix A	66
	Appendix B	67
Figures		
1-1	6ES5-242 Counter Module Block Diagram	42
2-1	242 Module Plug Connector Block Diagram	48
2-2	242 Module Plug Connector Pinout	48
2-3	Counter & Gate Input Circuitry	48
2-4	Counter & Gate Input TTL Level Circuitry	49
2-5	Counter & Gate Input 24 V Level Circuitry	49
2-6	Counter Output Circuitry	49
4-1	Function Block 158	61
4-2	Function Block 159	62
Tables		
4-1	Organization Block Calls	61
4-2	Data Block Assignments	64

1.1 General Description

The 6ES5-242 module consists of five high speed counters which can be independent of each other, or cascaded. The following is a general discussion of capabilities available with the 6ES5-242 Counter Module. Details of these capabilities and how to configure the module is presented in Chapter 2 of this manual.

1.1.1 Gate Control

Each counter can be enabled with either an external field signal or an internally generated signal. A variety of signal configurations is available for the gate inputs.

1.1.2 Inputs

Internally generated signals from the output of one of the other counters, or output from one of the two internal scalers are provided. External inputs are provided from each of the counters, which can be connected to a user application.

1.1.3 Outputs

The outputs may be used internally to feed another counter or to trigger an interrupt; or externally connected to a user function.

1.1.4 Interrupts

Counters 1 & 2 allow you to program the counter to generate an interrupt when a specific count is reached. All of the counters can generate an interrupt (if enabled) when the counter's output becomes active. The counter's active state can be defined by the user.

Gate inputs 1, 2, & 3 are connected directly to the interrupt controller, and can be enabled to generate an interrupt when they are active. The gate inputs signals can be selected for active high or active low states. These three interrupts operate separately and are not influenced by counters 1, 2, or 3.

1.1.5 Scaler 1

An internal scaler is available whose five fixed frequency outputs can be routed to the input of any of the counters or the input of Scaler 2. The 2 MHz system clock is used as the input frequency to the scaler. The outputs are scaled in factors of 10 or 16 from the input frequency.

1.1.6 Scaler 2

Scaler 2 is used to scale its input by a selectable factor between 1 and 16. The input can be selected from any of the counter inputs, gate inputs, or Scaler 1 outputs. The output of Scaler 2 can be connected by a jumper, selectable on switches S5 or S6 to the counter inputs, or gate inputs of any of the five counters.

1.2 6ES5-242 Block Diagram

The 6ES5-242 counter module is an intelligent peripheral controlled by a 8085 microprocessor system. The module uses the AM 9513 Counter Chip, which contains five independent, high-speed 16-bit counters to perform the counting operations. The AM 9519, an interrupt controller, is used to control the user-programmable interrupt structure.

The firmware for the module is stored on a 4K byte EPROM. A 1K byte CMOS RAM chip is used for data storage.

The counter and gate inputs and the counter outputs are optically to the front connectors of the module. Figure 1-1 is a block diagram of the logic on the 6ES5-242 counter module. The control logic handles the interface between the 6ES5-242 and the PC.

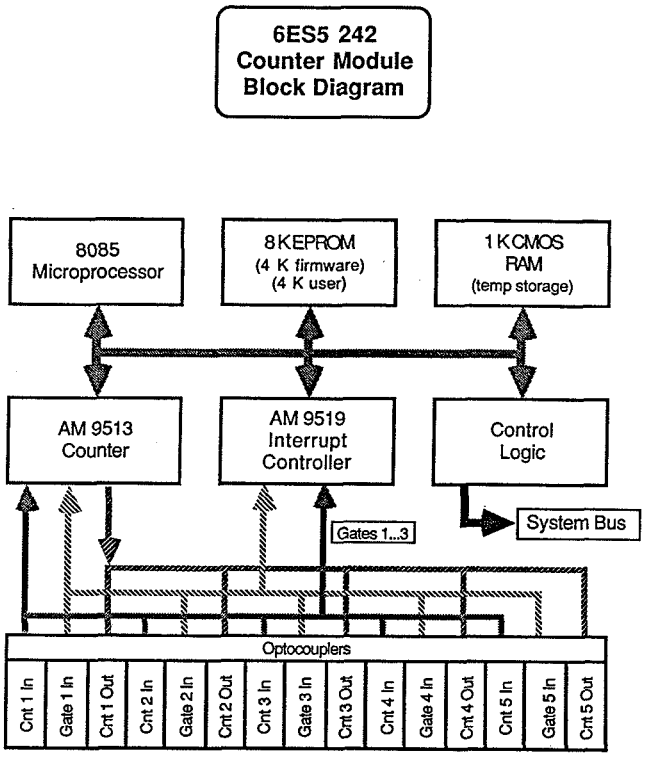


Figure 1-1 6ES5-242 Counter Module Block Diagram

1.3 The AM 9513 Counter Chip

The AM 9513 counter chip contains five high-speed counters which can be programmed to perform various counting and scaling functions. A general description for each of the 16-bit registers that control these counters is given below.

1.3.1 Master Mode Register (AM 9513)

The Master Mode register (MM) is used to enable and perform special functions which are common to each individual counter. There is one master mode register for all five counters. These functions include:

- Defining and enabling the inputs, outputs, and scaling factor for Scaler 2. This is the main function of the MM register
- Providing an enable bit for the output of Scaler 2. The output of Scaler 2 will be referred to as FOUT
- Providing enable bits for the two comparators that are available for Counters 1 and 2
- Providing a bit to select the operating mode of Scaler 2. Either binary scaling or BCD scaling is allowed
- Providing two bits which are used to control and enable the real-time clock function

1.3.2 Counter Mode Register (AM 9513)

There is one Counter Mode register (CM) for each of the five counters. The counter mode registers are used to provide control, setup, and operation of each individual counter. These functions include:

- Providing four bits to select one of 16 available pulse sources to the counter
- Providing a bit to enable or disable the gate control functions
- Providing three bits to select the operating mode of the gate control function
- Providing a bit to select the counting pulse edge, either rising or falling edge
- Providing a bit to select one of two registers from which the counter value can be loaded
- Providing a bit to select one of two counting modes, either continuous or onecycle mode
- Providing a bit to select the counter's operating mode, either binary or BCD counting
- Providing a bit to select the counting direction, either up counting or down counting.
- Providing three bits to select the output configuration of the counter

1.3.3 Load Register (AM 9513)

There is one Load register (L) for each of the five counters. The Load register is used to provide the counter with a preset count value which is set by the user.

1.3.4 Hold Register (AM 9513)

There is one Hold register (H) for each of the five counters. The Hold register is used as a storage buffer for the counter value. The contents of the counter will be transferred to the Hold register via a software command. This feature allows the user to check the current value of the counter without interrupting the counting operation.

The Hold register cannot be read directly; its data is first transferred to the result of counter register. You must then read the result of counter register to retrieve the value stored in the Hold register. The result of Counter register is described in Section 1.5.1.

1.3.5 Alarm Register (AM 9513)

There are two Alarm registers (A); one for Counter 1, and one for Counter 2. The Alarm register is used in conjunction with the comparators available to Counters 1 and 2. The Alarm register is used to store the value which will be compared with the counter value. If the comparator is enabled in the Master Mode register, the output of the counter will become active only when the Alarm register value equals the counter value. The Alarm register may also be referred to as the Interrupt register.

1.4 6ES5-242 Module Registers

The 6ES5-242 module has several registers which are not found in the AM 9513 or the AM 9519 chips. These registers are used for various functions which are not available on the AM 9513 or the AM 9519, but are necessary for the operation of the AM 9519, but are necessary for the operation of the module. A brief description of these registers is presented.

1.4.1 Control Register

The Control register (CTRL) is used to control various functions and counter selections of the AM 9513. This register is not normally addressed directly by the user; the function blocks used to communicate with the 6ES5-242 module will handle any data transfers to this register. These functions include:

- Providing three bits to select from one of eight possible chip operations which include: parameter assignment, counter manipulation, and selection of additional functions.
- Providing five bits, one for each counter, which are used to specify which counter or counters are to be involved in the operation selected by the other three bits of the register.

1.4.2 Function Number Register

The Function Number Register (FNR) is used to identify the user-stored functions. These functions can be stored on a 4K byte EPROM.

1.4.3 Interrupt Mask Register

The 6ES5-242 module has one 16-bit Interrupt Mask register (INTM); the eight low order bits of the interrupt mask register are used to enable and disable the eight interrupts generated by the AM 9519. Only two of the eight high order bits of the interrupt mask register are used. These two bits are used for enabling a group interrupt for a Ready signal and an Error signal, which will be described in detail later in this manual.

1.4.4 Interrupt Information Register

The Interrupt Information register (INTI) is a 16-bit register which is a mirror image of the Interrupt Mask register. It is used to store any interrupts that have occurred. You may read the contents of the Interrupt Information register to determine which interrupt has occurred.

1.4.5 Error Signal Register

The Error Signal register (FEM) is a 16-bit register which may be read to determine if one of several errors has occurred. A group interrupt will be sent to the PC if the error bit in the Interrupt Mask register is set.

1.4.6 Result of Counter Register

There is one Result of Counter register (E1 - E5) for each of the five counters. The Result of Counter register is used to store the current count of the counter when the register is read. Reading the register does not affect the operation of the counter

The Hold register cannot be read directly; its data is first transferred to the Result of Counter register. You then read the Result of Counter register to retrieve the value stored in the Hold register.

This section will describe in detail the setup of the six switches located on the 6ES5-242 module.

2.1 Switch S1 - Addressing

The S1 switch is used to select the module's address within a PC. It is connected to the address lines A4 - A11. The addressing range is selected from 128 to 240 decimal. The following figures show the details of the S5-150, S5-135U, and S5-115U.

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
x	x	x	x	1	s	s	s	0	0	0	0
module address								sub address			

x = irrelevant if jumper E-F is removed. If jumper E-F is installed, A11 - A8 should be open. Note that jumper E-F should only be installed for the S5-210 system.

I = selected or jumper closed. A7 must be closed to have an address of at least 128.

s = selectable jumpers. With jumpers A6 - A4 there are eight different addresses selectable for the module.

o = represents the sub address, A3 - A0. Each module has 16 internal addresses which are relative to the module's address.

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Decimal	Hex
x	x	x	x	1	0	0	0	0	0	0	0	128-143	xx80-xx8F
x	x	x	x	1	0	0	1	0	0	0	0	144-159	xx90-xx9F
x	x	x	x	1	0	1	0	0	0	0	0	160-175	xxA0-xxAF
x	x	x	x	1	0	1	1	0	0	0	0	176-191	xxB0-xxBF
x	x	x	x	1	1	0	0	0	0	0	0	192-207	xxC0-xxCF
x	x	x	x	1	1	0	1	0	0	0	0	208-223	xxD0-xxDF
x	x	x	x	1	1	1	0	0	0	0	0	224-239	xxE0-xxEF
x	x	x	x	1	1	1	1	0	0	0	0	240-255	xxF0-xxFF

x = irrelevant it jumper E-F is open. If jumper E-F is closed, jumpers must be open.
1 = jumper closed.
0 = jumper open.

For the S5-210 system bus the addressing range is between F01xH and FFFxH. A maximum of 255 modules may be addressed.

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
s	s	s	s	s	s	s	s	0	0	0	0
		module address						sub		address	

Jumper E-F should be installed for the S5-210 system.

s = selectable jumpers. With jumpers A11 - A4 there are 255 different addresses selectable for the module.

o = represents the sub address, A3 - A0. Each module has 16 internal addresses, which are relative to the module's address.

SWITCH S1 Jumper Assignments

Jumper	Address
8-9	A4
7-10	A5
6-11	A6
5-12	A7
4-13	A8
3-14	A9
2-15	A10
1-16	A11

2.2 Switch S2 Group Interrupts

NOTE:
If your PC is not the S5-150S, all jumpers on Switch S2 should be open and the setting of switch S2 is not necessary.

Switch S2 is used in conjunction with the 150S PC. The 150S does not have a hardware interrupt line on the backplane of the PC as do the 135U, 115U, and the 210 PCs. Instead the 150 uses IBO (input byte 0) to provide interrupt capabilities. To allow the use of IBO the 242 module provides special circuitry which allows it to simulate IBO.

The 150S system may contain up to eight 242 modules. If the interrupt capabilities are to be used, each of the modules used within the PC must be assigned a group interrupt code. This is accomplished with switch S2.

The first module used within the PC must be assigned as the Master module. If only one module is used, it must be assigned as the Master. When an interrupt occurs it will appear on IB0, bit 0 for the module that is coded as the Master.

The remaining modules used in the PC will be assigned a slave number, slaves 1 - 7. These slave numbers correspond to the remaining bits in IB0; i.e., slave 2 will be IB0.2.

The 150S interrupt system has a priority organization, IB0.0 has the highest priority and IB0.7 has the lowest priority. This in turn will be true for the 242 modules installed within the PC. The Master will have interrupt priority over the slaves, slave 1 will have priority over slave 2 and so on.

Also used in conjunction with switch S2 will be jumper G-H. The jumper G-H is used to determine if the module is the Master or a slave. The following table reflects the correct settings for each of thr eight possible modules.

IBO.x	S2 Jumper	Description	OBx	Jumper G-H
0	8-9	Master	OB2	open
1	7-10	Slave 1	OB3	closed
2	6-11	Slave 2	OB4	closed
3	5-12	Slave 3	OB5	closed
4	4-13	Slave 4	OB6	closed
5	3-14	Slave 5	OB7	closed
6	2-15	Slave 6	OB8	closed
7	1-16	Slave 7	OB9	closed

Coding Rules For The Master Module:

1. Jumper G-H must be open.
2. Jumper 8-9 on S2 must be closed. This will identify the module as the Master.
3. The remaining jumpers on S2 will be closed, unless there is a slave module assigned to that jumper; then it should be open.

Coding Rules For Slave Modules:

1. Jumper G-H must be closed.
2. Jumper 8-9 on S2 must be open.
3. Only the jumper on S2 for the appropiate slave number should be closed. The remaining jumpers on S2 must be open.

NOTE:
Because an interrupt will occur on any transition at IBO the user must program the OBs not to respond when the interrupts are reset, a transition from 1 to 0. The OBs should only respond when the transition is from 0 to 1. The following statements could be installed at the beginning of the OB to provide interrupt reaction only on a 0 to 1 transition.

OBx
A I 0.x
BEC

Note:
If the 6ES5 242 module is installed and the group interrupts are used, an input module cannot be assigned to byte address 0 (IB0). If there is an input module installed with byte address 0 (IB0) assigned, the group interrupt will not operate; instead, the input module will operate.

2.3 Switch S3 - System Interrupts

Switch S3 provides the module a choice of which system interrupt it will be connected to within the PC. The 6ES5 242 can be connected to one of seven different interrupt lines by closing the proper jumper on switch S3. Which interrupt is used is dependent on which type of PC the module is installed in. A brief description of how to handle the interrupts for a particular system is given below.

NOTE:
All jumpers on switch S3 which do not pertain to the system being used should be left open.

S5-150
The S5-150 does not use switch S3; instead Group Interrupt switch S2 is used to assign interrupts. When using a S5-150, all of the jumpers should be open. Refer to the previous section for interrupt handling with the S5-150.

S5-210
The S5-210 system has four system interrupts available and a 210 bus interrupt (PL4) available. The program response to each of the available interrupts must be written in assembly language. The interrupt handling system for the S5-210 system is beyond the scope of this manual and the reader should refer to the instruction manual for the S5-210 system.

Jumper	Description
8-9	System Interrupt IRA'
7-10	System Interrupt IRB'
6-11	System Interrupt IRC'
5-12	System Interrupt IRD'
1-16	210 Bus Interrupt PL4' (EANK')

S5-135U
The S5-135U has only one system interrupt for each of the four available CPUs. This is a hardware interrupt, and is handled by OB2. Because there is just one interrupt for each CPU, you should identify which module issued the interrupt by checking each of the interrupt information registers of the counter modules connected to that CPU. This is done in OB2 of each CPU. Each counter module may be connected to more than one interrupt; i.e., one counter module may be connected to the interrupts of CPU 1 and CPU 2, while another counter module is just connected to the interrupts of CPU 2.

OB2	Jumper	Description
OB2	8-9	System interrupt IRA' for CPU 1
OB2	7-10	System interrupt IRB' for CPU 2
OB2	6-11	System interrupt IRC' for CPU 3
OB2	5-12	System interrupt IRD' for CPU 4

S5-115U
The S5-115U has two system interrupts. These are hardware interrupts, and are handled by two organization blocks. You have to specify which modules will be connected to which interrupt, and handle the interrupts via the availavle OBs. For example, if more than one module is connected to IRA', then each of the modules connected must have their Information Registers read to determine which module issued the interrupt.

OBx	Jumper	Description
OB2	8-9	System interrupt IRA'
OB3	7-10	System interrupt IRB'

2.4 Switch S4 - Gate Signal Conditioning

Switch S4 is used to change the transition direction of the gate input signals that feed the interrupt system of the 6ES5 242 module. The first three external gate signals, G1 - G3, are fed to three of the interrupt lines of the AM 9519 interrupt controller chip.

This allows use of any of the three external gate inputs to trigger an interrupt for the module. The Interrupt Mask Register must be set accordingly to enable the gate interrupts. Note also that the external gate signals are first routed through switch S6.

The AM 9519 interrupt controller chip is firmware programmed to allow a 0 to 1 transition. You must determine which type of external gate transition will be used (1 to 0 or 0 to 1), and set switch S4 accordingly.

Jumper	Description
1-8	G1 external gate input to AM 9519.
2-7	G2 external gate input to AM 9519.
3-6	G3 external gate input to AM 9519.
4-5	G4 external gate input, not used.

Jumper closed = 0 to 1 transition, rising edge.
Jumper open = 1 to 0 transition, falling edge.

2.5 Switch S5 - Counter Input Routing

Switch S5 is used to physically connect the input to each of the five counter inputs of the AM 9513 to either the external counter input or the FOUT signal. The external counter input is routed through optocoupling from the connectors located on the front of the module (see section 2.8.1, Plug Connector). The FOUT signal is an output of the AM 9513 counter chip which can be programmed by the user (see section 3.3, Master Mode Register).

For example, if you connect the counter input of counter 1 to the FOUT signal and you would like to use the FOUT signal for an input to counter 2, you would specify counter 1 as the pulse source in the counter mode register of counter 2.

Counter	External Input	F2 Scaler (FOUT)
1	1 - 20	2 - 20
2	3 - 18	4 - 18
3	5 - 16	6 - 16
4	7 - 14	8 - 14
5	9 - 12	10 - 12

2.6 Switch S6 - Gate Input Routing

Switch S6 is used to physically connect the input to each of the five gate inputs of the AM 9513 to either the external gate input or the FOUT signal. The external gate input is routed through optocoupling from the connectors located on the front of the module (see section 2.8.1, Plug Connector). The FOUT signal is an output of the AM 9513 counter chip which can be programmed by the user (see section 3.3, Master Mode Register).

For example, if you connect the gate control input of counter 1 to the FOUT signal, and you would like to use the FOUT signal for an input to counter 2, you would specify counter 1 as the pulse source in the counter mode register of counter 2.

Gate	External Input	F2 Scaler (FOUT)
1	1 - 20	2 - 20
2	3 - 18	4 - 18
3	5 - 16	6 - 16
4	7 - 14	8 - 14
5	9 - 12	10 - 12

2.7 Jumper Assignments

There are several solder type jumpers which are installed on the 6ES5 242 module. Their meanings are listed below.

Jumper	Delivery State	Description
A - B	closed	Used for testing
C - D	open	Used to enable de coding of byte ø
E - F	closed	Used for module addressing in conjunction with swith S1.
G - H	open	Used to determine if the module is a master (open) or slave (closed).
I - K	closed	Used to determine if the module is reset with the system CPKL' signal
L- M	open	Is used to enable (closed) the TRAP interrupt routine stored in firmware for 8085.

2.8 Inputs And Outputs

2.8.1 Plug Connectors

The connection of the 6ES5 242 counter module to the user inputs and outputs is accomplished via a 9-pin plug connector. There are five such connectors mounted on the front plate of the module, one for each of the five counters. (See Figures 2-1 and 2-2)

Pin	Signal	Description
1	Shield	Cable shield connection
2	INxM	Counter Input x, M terminal (minus)
3	INx	Counter Input x, signal
4	Tx	Gate Input x, signal
5	TxM	Gate Input x, M terminal (minus
6	AxP	Counter Output x, external voltage
7		not connected
8	Ax	Counter Output x, signal
9	AxM	Counter Output x, external voltage (minus)

NOTE: x = 1 - 5

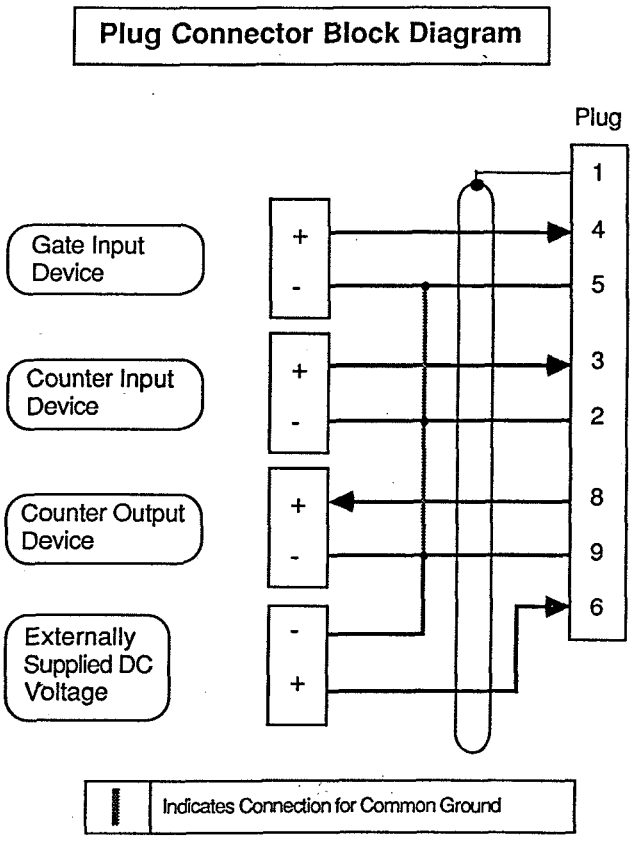


figure 2-1 242 Module Plug Connector Block Diagram

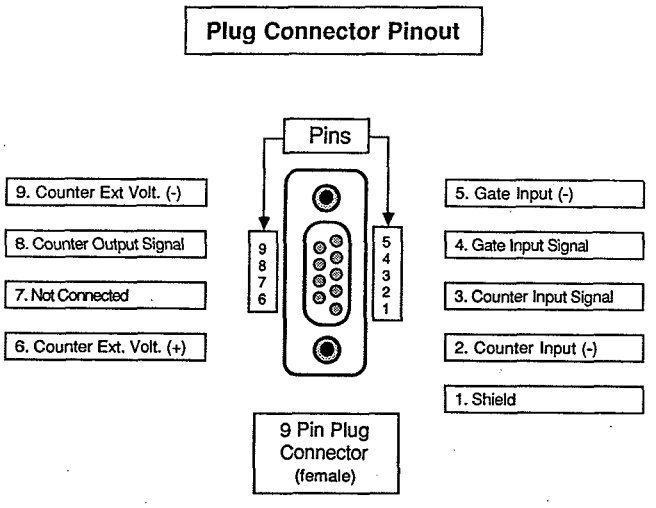


Figure 2-2 242 Module Plug Connector Pinot

2.8.2 Counter and Gate Inputs

The counter and gate inputs which are connected through the front connectors of the module are galvanically isolated by means of optocouplers. The input circuitry is identical for both types of inputs and can be configured for TTL levels or 24 vdc levels.

The counter inputs are pulse edge sensitive. The gate inputs can be programmed in the counter mode (CM) register to be either pulse edge sensitive or level sensitive.

Figure 2-3 illustrates the circuitry of the counter input gates. The circuit is supplied with an input resistor (Rx) to allow different input voltage levels to be selected. A capacitor (Cx) can be added to the output to suppress noise spikes. Note that the counting frequency is affected when capacitors are added.

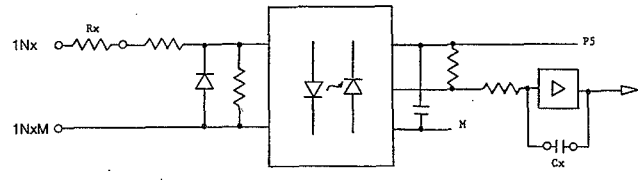


Figure 2-3 Counter & Gate Input Circuitry

TTL Level Specifications

The input circuit for TTL levels should be designed to provide a +5 vdc at INx continously, and provide an open collector configured circuit at the INxM input, which does the switching. This circuit configuration is show in Figure 2-4.

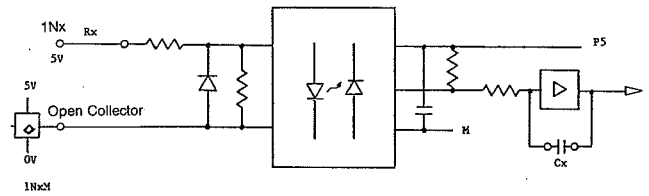


Figure 2-4 Counter & Gate Input TTL Level Circuitry

Description	Value	Notes
INx	4.75 - 5.25 Vdc	
INxM	0.5 - 0.8 Vdc	Low Level
INxM	1 ma leakage current	High Level
Input current	approx. -6.5 ma	INxM = 0.4 V, INx = 5 V
Input Resistance	approx. 500 ohm	
Rx	Jumper	

24 Vdc Level Specifications

Figure 2-5 illustrates the necessary configuration for 24 V input to the gate input circuitry

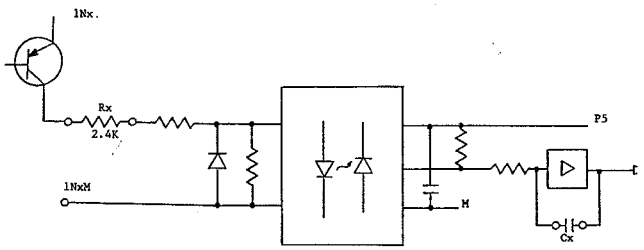


Figure 2-5 Counter & Gate Input 24 V Level Circuitry

Description	Value	Notes
INxM	0.0 v	
INx	13 - 33 Vdc	High Level
INx	-35 - +4.5 Vdc	Low Level
Input Current	approx. 12 ma	INxM = 0V, INx = 24 Vdc
Input Resistance	approx. 2 k ohm	
Rx	1,5 k ohm	

2.8.3 Counter Outputs

The output of each of the five counters is routed to the plug connectors on the front of the module. These outputs are galvanically isolated by means of optocouplers. The outputs are the equivalent of P switches and are current limited. Driving distance is a function of the external voltage source and, of course, the type of wire used. Distances of 200 meters and beyond are attainable. Figure 2-6 illustrates the counter output circuitry configuration.

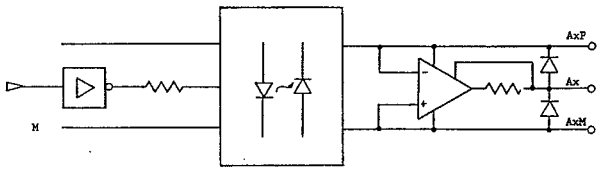


Figure 2-6 Counter Output Circuitry

Description	Value	Notes
Ax High Level	22V	Residual voltage approx. 2V Output Current = -100 ma
Ax Low Level		Resident current = -100 ua
Short Circuit	200 ma	AxP=24V, AxM=0V, Rext=0
AxP	20 - 30V	External supply voltage
Switching Freq	10kHz	Rext = 330 ohm
Delay Times		
Low to High	20 usec	Rext = 330 ohm
High to Low	20 usec	Rext = 330 ohm
Rise Time	1 usec	Rext = 330 ohm
Fall Time	5 usec	Rext = 330 ohm

NOTE: Rext = external load resistance

2.8.4 Signal Conditioning

The Cx and Rx numbers for each of the counters and gates are listed below.

Counter/Gate	Counter Cx Rx	Gate Cx Rx
1	C15 R21	C22 R26
2	C16 R22	C23 R27
3	C17 R23	C24 R28
4	C18 R24	C25 R29
5	C19 R25	C26 R30

The values for Cx and the maximum counting frequency are listed below.

Maximum	Counting Freq.	Cx value
approx	2000 kHz	no capacitor installed
approx	200 kHz	100 pf
approx	20 kHz	1 nf
approx	2 kHz	10 nf

2.9 Module Pin Out

The 6ES5 242 module is supplied with a 48-pin connector which conforms to DIN 41612. The pin out of the module is listed below.

Pin	d	b	z
2		0 V	+5 V
4		PESP	
6		ADB 0	CPKL
8		ADB 1	MEMR'
10		ADB 2	MEMW'
12		ADB 3	RDY'
14	IRA'	ADB 4	DB 0
16	IRB'	ADB 5	DB 1
18	IRC'	ADB 6	DB 2
20	IRD'	ADB 7	DB 3
22	IRE'	ADB 8	DB 4
24	IRF'	ADB 9	DB 5
26	IRG'	ADB 10	DB 6
28		ADB 11	DB 7
30			PL 4, EANK'
32		O V	

2.10 6ES5 242 Module Memory Map

Setting of the physical address of the 6ES5-242 module was discussed in an earlier section. In that section the subaddress was shown to have 16 possible addresses. This section will map out these 16 subaddresses.

Direct reading and writing operations to the module are accomplished through peripheral words (PWxx). This is particulary useful when you need to develop a "custom" software function. See Chapter 4 for detailed information on Standard Software Blocks. Exercise extreme caution when using this feature with standard software, as these two operations may interfere with each other.

Sub Address	Register name Write Operation	Register name Read Operation
xxx0	Control	Interrupt Information - High
xxx1	not assigned	Interrupt Information - Low
xxx2	Function Number	Error Signal - High
xxx3	not assigned	Error Signal - Low
xxx4	Interrupt Mask - High*	not assigned
xxx5	Interrupt Mask - Low*	not assigned
xxx6	Master Mode - High*	Result Counter 1 - High
xxx7	Master Mode - Low*	Result Counter 1 - Low
xxx8	Counter Mode - High*	Result Counter 2 - High
xxx9	Counter Mode - Low*	Result Counter 2 - Low
xxxA	Load - High*	Result Counter 3 - High
xxxB	Load - Low*	Result Counter 3 - Low
xxxC	Hold - High*	Result Counter 4 - High
xxxD	Hold - Low*	Result Counter 4 - Low
xxxE	Alarm - High*	Result Counter 5 - High
xxxF	Alarm - Low*	Result Counter 5 - Low

*: The value in this register will be sent to any of the counters specified during the parameter assignment.

NOTE:
The Standard software offering does not read the alarm register when parameters are assigned to counters 3, 4, and 5.

The counter module's operation is totally software driven. Complete manipulation of the five counters is accomplished by writing software which set various registers with values predefined in the module's firmware. In this section, detailed information is presented on the registers and the selections available. The registers and their abbreviations are:

Interrupt Mask Register - INTM
Interrupt Information Register - INTI
Master Mode Register - MM
Counter Mode Register - CM
Control Register - CTRL
Function Number Register - FNR
Error Signal Register - FEM
Result of Counter 1 - E1
Result of Counter 2 - E2
Result of Counter 3 - E3
Result of Counter 4 - E4
Result of Counter 5 - E5
Load Register - L
Hold Register - H
Alarm Register - A

3.1 INTM - Interrupt Mask Register

The interrupt mask register allows you to enable or disable the group interrupt (set via switch S2) and the system interrupts (set via switch S3) for each of the interrupts available.

To enable an interrupt, write a logic 1 in the corresponding bit of the INTM register. The AM 9519 interrupt controller chip is an edge sensitive device and will generate a group and a system interrupt when a transition of the enabled interrupt input is detected.

Interrupt processing requires a properly defined organizational block for the type of PC used to handle these interrupts. This includes the use of a reset call using the standard function block which will be described in detail in Chapter 4 of this manual. The setting of switches S2 and S3 was described in Section 2.2 and 2.3.

INTM - Low Order Byte Subaddress xxx5, Write

Bit	7	6	5	4	3	2	1	0
	Z1	Z2	Z3	Z4	Z5	T1	T2	T3
			Counter OUT signals			Gate signals		

Z1 - Z5 = The counter OUT signal from the AM 9513. These signals must have the CM register set to active high or active low.

T1 - T3 = The gate input signals for gates 1 - 3. The inputs may be manipulated by the setting of the S4 switch. See Section 2.4.

INTM - High Order Byte Subaddress xxx4, Write

Bit	15	14	13	12	11	10	9	8
	R	E	0	0	0	0	0	0
	Ready Signal	Error Signal	not used					

1 = interrupt enabled
2 = interrupt disabled

When the error signal enable bit of the INTM is set to a logic 1, a group interrupt will occur when an error occurs in the FEM register. You must check the INTI register to identify the interrupt within the INTM register, and then check the FEM register to identify the initial cause of the interrupt.

When the ready signal enable bit of the INTM is set to a logic 1, a group interrupt will occur when the 6ES5 242's internal 8085 microprocessor has completed its internal program processing and is available to be accessed.

NOTE:
The INTM register is used only to enable the group and system interrupts for the module. If an interrupt occurs it will appear in the INTI register, regardless of the setting in the INTM register.

Refer to Chapter 4 for setting the INTM register with standard software blocks. The INTM register can be set using the PA mode of FB 159. Care must be taken when using the PA mode because the INTM register is set each time the PA mode is used for a particular counter.

3.2 INTI - Interrupt Information Register

The interrupt information register is used to store any interrupts that may occur on the module. The bit assignments of the INTI register are the same as the INTM register. An interrupt is identified by a logic 1.

When an interrupt occurs, you must read the value of the INTI register to identify which interrupt has occurred. The INTI register may be read directly using a "L PWxx" instruction or by checking the value of the data word assigned to represent the INTI register within the data block (defined when using the standard software). This programming is described in more detail in Chapter 4 of this manual.

INTM - Low Order Byte Subaddres xxx1, Read

Bit	7	6	5	4	3	2	1	0
	Z1	Z2	Z3	Z4	Z5	T1	T2	T3
			Counter OUT signals			Gate signals		

Z1 - Z5 = The counter OUT signal from the AM 9513.
T1 - T3 = The gate input signals for gates 1 - 3.

INTM - Hig Order Byte Subaddress xxx0, Read

Bit	15	14	13	12	11	10	9	8
	R	E	0	0	0	0	0	0
	Ready Signal	Error Signal	not used					

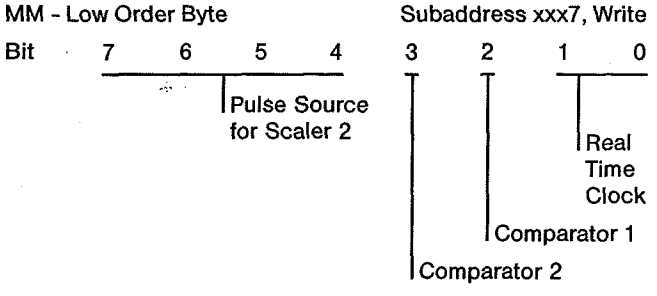
NOTE:
The INTI register will provide an indication of an interrupt whenever an interrupt occurs, regardless of the INTM register's settings.

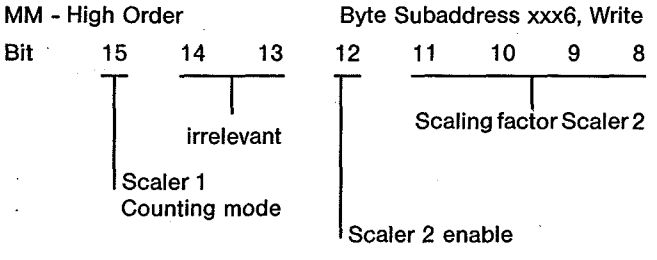
3.3 MM - Master Mode Register (AM 9513)

The MM register is used to enable and perform special functions common to each of the five counters on the AM 9513 counter chip. This section will describe the meaning of each of these functions, and how to set the MM register to accomplish the special function.

The MM register, a 16-bit register divided into seven sections, is used to enable and assign parameters for the various functions performed by the MM register. The bit assignments of the MM register and their meanings are listed below.

Refer to Chapter 4 for setting the MM register with standard software blocks. The MM register can be set using the PA mode of FB159. Care must be taken when using the PA mode because the MM register is set each time the PA mode is used for a particular counter.





3.3.1 Real-Time Clock: MM1 - MM0

The AM 9513 can perform a real-time clock function but this function is not supported by the 8085 firmware. A custom-made function block is required to support this feature. Unless you have created this function block, the value of MM1 and MM0 should be 00 to leave this function disabled.

MM1	MM0	Description
0	0	Real time clock disabled
0	1	Input frequency scaled for 50Hz
1	0	Input frequency scaled for 60Hz
1	1	Input frequency scaled for 100 Hz

3.3.2 Comparators 1 and 2: MM3 - MM2

The comparator function of the AN 9513 will allow Counters 1 and 2 to perform a 16-bit compare function. The actual value of the counter is compared to the value stored in the alarm register for the counter.

Enabling the compare function for the counter will enable special circuitry in the AM 9513, which will configure the counter output to go to the active state when the comparison is true. The comparison is considered true only when the values are equal to each other.

When the count value changes from the true state, the output will again appear in the false state. The active state of the counter may be set to active high or active low in the CM register (CM2 - CM0).

MM3	MM2	Description
x	0	Comparator 1 disabled
x	1	Comparator 1 enabled
0	x	Comparator 2 disabled
1	x	Comparator 2 enabled

x = irrelevant

3.3.3 Scaler 2 (FOUT) Pulse Source: MM7 - MM4

MM7	MM6	MM5	MM4	Description of pulse source
0	0	0	0	Output Scaler 1 F1
0	0	0	1	Counter input 1
0	0	1	0	Counter input 2
0	0	1	1	Counter input 3
0	1	0	0	Counter input 4
0	1	0	1	Counter input 5
0	1	1	0	Gate input 1
0	1	1	1	Gate input 2
1	0	0	0	Gate input 3
1	0	0	1	Gate input 4
1	0	1	0	Gate input 5
1	0	1	1	Output Scaler 1 F1
1	1	0	0	Output Scaler 1 F2
1	1	0	1	Output Scaler 1 F3
1	1	1	0	Output Scaler 1 F4
1	1	1	1	Output Scaler 1 F5

NOTE:
The reset or default value for MM7 - MM4 is 0000.

3.3.4 Scaler 2 (FOUT) Scaling Factor: MM11 - MM8

The scaling factor of the pulse source signal, which was selected in bits MM7 - mm4, can now be selected using bits MM11 - MM8. A scaling factor from 1-16 may be selected. Scaler 2 now scales the selected pulse source by the selected scaling factor. The results is routed to the output of scaler 2 (FOUT).

MM11	MM10	MM9	MM8	Scaling Factor
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

3.3.5 Scaler 2 (FOUT) Enable: MM12

This bit of the MM register is used to enable and disable the output of scaler 2 (FOUT). The default value of 0 will enable the FOUT signal.

MM12	Description
0	FOUT enabled
1	FOUT disabled

3.3.6 Scaler 1 Counting Mode: MM15

This bit is used to set the counting mode of Scaler 1. The default value of 0 will place the output of Scaler 1 in the binary counting mode.

MM15	Description
0	Scaler 1 in binary counting mode
1	Scaler 1 in BCD counting mode

Scaler 1 Outputs - Input Frequency: 2MHz

Output	BCD Mode		Binary Mode	
F1	:1	2000kHz	:1	2000kHz
F2	:10	200kHz	:16	125kHz
F3	:100	20kHz	:256	7.812kHz
F4	:1000	2kHz	:4096	488.3Hz
F5	:10000	200Hz	:65536	30.5Hz

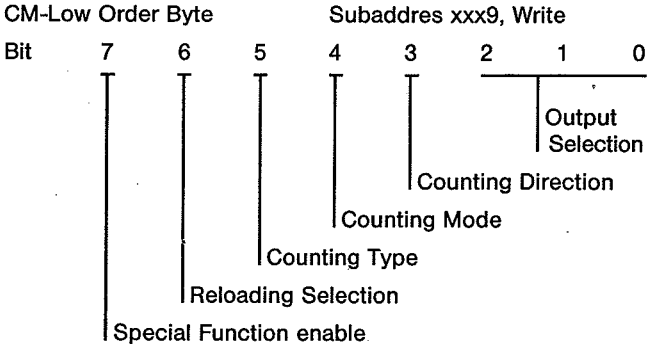
3.3.7 Bits MM14 and MM 13

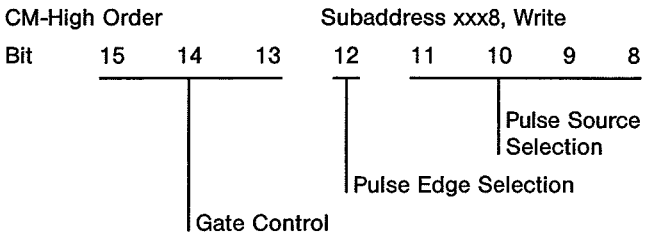
Bits MM 14 and MM13 of the MM register are not available to the user on the 6ES5 242 module. These bits are used by the 8085 firmware. The condition of these bits is irrelevant.

3.4 CM - Counter Mode Register (AM 9513)

There are five CM registers on the AM 9513, one for each counter. The CM register is used to assign the operation parameters for the counters.

The CM register is a 16-bit register that is divided into nine sections. These nine sections are used to select the operating mode of the counter. The bit assignments of the CM register and their meanings are listed below.





3.4.1 Output Selection: CM2 - CM0

Bits CM2 - CM0 of the CM registers allow selection of several different counter output modes. The output of each counter is connected to the AM 9519 interrupt controller and also to the respective front connector of the module.

CM2	CM1	CM0	Description
0	0	0	Illegal
0	0	1	Active high, TC Pulse mode
0	1	0	TC Toggled mode, start low
0	1	1	TC Toggled mode, start high
1	0	0	Illegal
1	0	1	Active low, TC Pulse mode
1	1	0	Illegal
1	1	1	Illegal

TC = Terminal Count

DEFINITIONS:
Terminal Count: The point in time where the counter value reaches a value of zero. This is the point where the counter output will change state. The following is a listing of the conditions that will cause TC to occur on the next count.

Counter Value	Direction	Counting Mode
0001	down	BCD or binary
9999	up	BCD
FFFF	up	binary

When using the counter outputs of the AM 9513 you must remember that all outputs switch on TC, which means that all counting operations depending on a switched output must either count down to TC, or count up to TC, to achieve the expected output.

TC Pulse mode: This mode will produce an output when the count value equals zero. The output will become active on the leading edge of TC. The width of the output pulse depends on the time the counter is at a zero value. Active high and active low simply mean the state of the pulse during the time the counter is at zero value.

TC Toggle mode: This mode will produce an output level instead of a pulse. This level will toggle between the high and the low states on the trailing edge of TC.

3.4.2 Counting Direction: CM3

This bit is used to determine the counting direction of the counter.

CM3	Direction
0	Down counting
1	Up counting

3.4.3 Counting Mode: CM4

This bit is used to determine the counting mode of the counter.

CM4	Mode
0	Binary counting
1	BCD counting

NOTE:
Bits CM7 - CM5 and CM15 - CM13 are used together to determine a particular counter mode. These modes will be described in detail later in this section. First, each of the bits mentioned above will be described separately.

3.4.4 Countig Type: CM5

This bit is used to determine which type of counting is to be used.

CM5	Type
0	Count once (one-shot)
1	Count repetitively (periodic)

Count once: This type of counting will allow the counter to count until TC occurs. At TC the counter will be disarmed automatically.

Count repetitively: This type of counting will allow the counter to count in the mode specified until disarmed.

3.4.5 Reloading Selection: CM6

This bit provides a selection of which register the counter will be loaded by when TC occurs. The selection of the Hold register or the Load register is dependent on the counter's operating mode. These modes are described in detail later in this section.

CM6	Reloading register
0	Reloading from the Load register
1	Reloading from the Load or Hold registers

3.4.6 Special Function Enable: CM7

This bit is used to enable or disable special functions which are associated with gate control, bits CM15 - CM13. The setting of this bit is again dependent on the counter's operating mode.

CM7	Gate Control
0	Special Function disabled
1	Special Function enabled

3.4.7 Pulse Source Selection: CM11 - CM8

CM11	CM10	CM9	CM8	Description of pulse source
0	0	0	0	Counter output n-1
0	0	0	1	Counter input 1
0	0	1	0	Counter input 2
0	0	1	1	Counter input 3
0	1	0	0	Counter input 4
0	1	0	1	Counter input 5
0	1	1	0	Gate input 1
0	1	1	1	Gate input 2
1	0	0	0	Gate input 3
1	0	0	1	Gate input 4
1	0	1	0	Gate input 5
1	0	1	1	Output scaler 1 F1
1	1	0	0	Output scaler 1 F2
1	1	0	1	Output scaler 1 F3
1	1	1	0	Output scaler 1 F4
1	1	1	1	Output scaler 1 F5

3.4.8 Cascading Counters

Counter output n-1 "0000" can "feed" the output of a previous counter into the input of the next counter, according to the following flow:

Counter Input	Previous Counter Output
1	5
2	1
3	2
4	3
5	4

3.4.9 Pulse Egde Selection: CM12

This bit will set edge triggering selection on the input pulse that begins the counting process. The choices are:

CM12	Counting Egde
0	The leading edge of the input triggers counting
1	The trailing edge of the input triggers counting

3.4.10 Gate Control Selection: CM15 - CM13

Bits CM15 - CM13 are used to configure the gate control options.

CM15	CM14	CM13	Gate Control
0	0	0	No gate control
0	0	1	Counter output (TC) n-1, active high
0	1	0	Gate n+1, active high level
0	1	1	Gate n—1, active high level
1	0	0	Gate n, active high level
1	0	1	Gate n, active low level
1	1	0	Gate n, active high edge
1	1	0	Gate n, active low edge

3.5 Counter Modes

The AM 9513 can implement numerous counting modes through software commands. These modes can be selected by using the proper codes in CM15 - CM13 and CM7 - CM5. For more details on each of the modes including waveform diagrams, the reader should refer to the AM 9513 data sheet. Some of the modes do not exist or are not supported by the 6ES5 242 module. Modes that may not be used are: M, P, T, U, W. The name of each of the modes available is listed below.

Mode	Title
A	Software triggered with no hardware gating
B	Software triggered with level gating
C	Hardware triggered strobe
D	Rate generator with no hardware gating
E	Rate generating with level gating
F	Non-retriggerable one-shot
G	Software triggered delayed pulse One-shot
H	Software triggered delayed pulse one-shot with hardware gating
I	Hardware triggered delayed pulse strobe
J	Variable duty cycle rate generator without hardware gating
K	Variable duty cycle rate generator with hardware gating
L	Hardware triggered delayed pulse one-shot
N	Software triggered strobe with level gating and hardware retriggering
O	Software triggered strobe with edge gating and hardware retriggering
Q	Rate generating with Synchronization
R	Retriggerable one-shot
S	Selectable reloading source
V	Frequency shift keying
X	Hardware Save

3.5.1 Mode A

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count once
0	0	0	0	0	0	Reloading: Load Register

This mode will allow the counter to start counting when an ARM command is received. The counter will reload from the Load register and count until TC occurs. Counting will resume when the ARM command is received again.

3.5.2 Mode B

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count once
LEVEL			0	0	0	Reloading: Load Register

This mode is the same as mode A with the exception that the counter will only be allowed to count when the gate input is in its active state. This allows the user to shut the counting process off by placing the gate input to an inactive state.

3.5.3 Mode C

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count once
EDGE			0	0	0	Reloading: Load Register

This mode is again the same as mode A. The difference is that this mode will only allow the counter to start counting upon receiving the first active edge from the gate input after the counter is armed. Once the counting process begins, other gate input edges are ignored. The counter will stop at TC.

3.5.4 Mode D

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count repetitivey
0	0	0	0	0	1	Reloading: Load Register

This mode once started will continuous count to TC then reload from the Load register and count to TC again. It is not affected by gate control. It can be used to generate waveforms whose period, between TCs, is determined by the value in the Load register.

3.5.5 Mode E

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count once
LEVEL			0	0	1	Reloading: Load Register

This mode is the same as mode D with the exception that the output will only be enabled while the gate input is in an active state. This allows you to stop and start the output waveform by disabling/enabling the gate input.

3.5.6 Mode F

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count once
EDGE			0	0	1	Reolading: Load Register

The counter in this mode, after it is armed, will start counting when the first gate edge is received. If another gate edge occurs it will be ignored once the counter is started. The counter will stop when TC occurs and reload from the Load register. The counter will remain stopped until the next gate edge occurs after the counter has stopped.

3.5.7 Mode G

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Countig Type:
						Count once
0	0	0	0	1	0	Reloading:
						Load or Hold Register

In this mode the counter will count to TC twice, once armed. The counter will initially be loaded from the Load register. Once counting has started and the counter reaches TC the first time, the counter will reload from the Hold register and proceed to count until TC is again reached. After the second occurrence of TC, the counter will automatically disarm and reload from the Load register.

3.5.8 Mode H

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count once
L	E	V	E	L		Reloading:
			0	1	0	Load Registe

This mode is the same as mode G with the exception that the counter will only count while the gate input is active. The counter will count to TC twice. Reloading occurs the first time from the Hold register and the second time from the Load register. The counting process will stop after the second TC is reached.

3.5.9 Mode I

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count once
E	D	G	E			Reloading:
			0	1	0	Load Register

This mode also performs the same as mode G with the exception that the counter, once armed, will start counting with the first active edge received at the gate input. Once the counting has started any other signals applied to the gate input are disregarded. Once the counter has counted to TC twice, it will have to be armed and another signal applied to the gate input in order for it to start the counting process over.

3.5.10 Mode J

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count repetitively
0	0	0	0	1	1	Reloading:
						Load Register

This mode allows you to create an output waveform which has two different cycle times. The counter, once started by an ARM command, will count continuously until it is stopped by a DISARM command. The counter will first be loaded with the value in the Hold register and will then count until TC is reached. Upon occurrence of TC, the counter will be loaded from the Load register. Each time TC is reached the counter will alternate between loading from the Hold and the Load registers.

3.5.11 Mode K

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count once
L	E	V	E	L		Reloading:
			0	1	1	Load Register

This mode is the same as mode J with the exception that the gate control is used to enable counting. With the gate input active the counter will count all input pulses to it. With the gate input inactive the counter will ignore any input pulses to it. Once armed, the counter will be loaded from the Hold register and on the next occurrence of TC will load from the Load register. This alternating loading will continue until the counter receives a DISARM command.

3.5.12 Mode L

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count once
E	D	G	E			Reloading:
			0	1	1	Load Register

This mode operates the same as mode K with the exception that the counter, once armed, will start counting when an active edge is applied to the gate input. After the first TC, the counter will load from the Hold register and count to until the second TC. At the second TC, the counter will load from the Load register and stop. The counter will start counting again when the next active edge is applied to the gate input, thus starting the count cycle again.

3.5.13 Mode N

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						enabled
						Counting Type:
						Count once
L E V E L			1	0	0	Reloading:
						Load Register

This counting mode allows you to trigger the counter via software to start the counting cycle and use a hardware retrigger thereafter. Once counting has started, all pulses fed to the counter will be counted if the gate input is active (level). When the counter reaches TC the counter will disarm and reload from the Load register.

Counting will resume with the issuing of an ARM command. The gate input will now function differently than it did before. When an active edge is received at the gate input the counter will store the counter contents in to the Hold register.

The first active edge received at the counter input while the gate input is active will cause the counter to reload from the Load register. The second active edge received at the counter input while the gate is active will cause the counter to resume counting. The counter will operate is this fashion until disarmed.

3.5.15 Mode O

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count once
E D G E			1	0	0	Reloading:
						Load Register

This operating mode is similiar to mode N with the exception that the counter will be started by an active edge applied to the gate input, to an armed counter. The counter once started will count to the first occurrence of TC, at this time it will disarm and reload from the Load register.

A new ARM command and an active edge input at the gate input must used to start the counter again. The counter will now be restarted upon each occurrence of an active edge input to the gate input (hardware retrigger).

When an active is received the contents of the counter will be placed in the Hold register. Upon receiving the first active edge at the counter input after retriggering, the counter will be reloaded from the Load register. The next active edge will start the counting process again.

3.5.15 Mode Q

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count repetitively
L E V E L			1	0	1	Reloading:
						Load Register

In this mode the counter must be armed before counting can occur. Once armed the counter will count all active edges at the counter input while the gate input is active. The counter will count to TC repetitively.

The counter will be reloaded from the Load register on each TC. The counter may be hardware retriggered by placing an active edge at the gate input. When retriggered, the contents of the counter will be stored into the Hold register. With the gate level active, the first active edge input to the counter will reloaded the counter with the contents of the Load register. The second edge will cause counting to resume.

3.5.16 Mode R

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count repetitively
E D G E			1	0	1	Reloading:
						Load Register

This mode is similiar to mode Q. The difference is that the input to the gate is edge-sensitive instead of level-sensitive. Once armed, the counter will count until TC, at which time it will stop and be reloaded from the Load register.

Counting will be resumed when the first active edge is received at the gate input. The counter will be retriggered on each occurrence of an active edge while the counter is counting. This retriggering sequence includes saving the contents of the counter to the Hold register. The counter will be reloaded from the load register when the first active edge input is received at the counter input. The counting will resume when the second active edge is received.

3.5.17 Mode S

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function:
						not enabled
						Counting Type:
						Count once
0	0	0	1	1	0	Reloading:
						Load Register

In this mode the gate input is used only to determine which register will load the counter. The gate input in this mode does not control counting operations. When the gate input is high the Hold (High-Hold) register is used, and when the gate is low the Load (Low-Load) register is used. Once armed, the counter will count to TC twice, each time reloading from the register selected. Once the second TC has occurred, the counter will disarm itself. A new ARM command will be required to start the counter cycle again.

3.5.18 Mode V

Counter Register Setup

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: not enabled Counting Type: Count repetitively
0	0	0	1	1	1	Reloading: Load Register

In this mode the gate input is used, as in mode S, to determine which register will load the counter. The counter will be loaded from the Load register when the gate input is low, and from the Hold register when the gate input is high. The counter will be loaded when a LOAD command is issued, or when a TC occurs. The counter will count repetitively once it is started. A DISARM command is required to stop the counter.

3.5.19 Mode X

Hardware Save (available in AM 9513 A only)

CM15	CM14	CM13	CM7	CM6	CM5	Special Function: enabled Counting Type: Count repetitively
E	D	G	E	1	1	1	Reloading: Load Register

Mode X, provides a hardware sampling of the counter contents without interrupting the count. A Load and Arm command or a Load command followed by an Arm command is required to initialize the counter. Once armed, a Gate edge starts the counting operation; gate edges applied to a disarmed counter are disregarded. After application of the Triggering Gate edge the counter will count all qualified source edges until the first TC, irrespective of the gate level. All gate edges applied during the counting sequence will store the current count in the Hold register, but they will not interrupt the counting sequence. On each TC, the counter will be reloaded from the Load register and stopped. Subsequent counting requires a new triggering Gate edge; counting resumes on the first source edge following the triggering Gate edge.

3.6 CTRL - Control Register

There is only one control register for the module. It is used to assign parameters and manipulate each of the counters. The CTRL register must be addressed by peripheral byte (PBxx) and is only available as a write operation. If the user is going to use the standard software (FB159), the CTRL register will not be addressed directly. A description of each of the functions is given in the preceding sections, along with the equivalent "BEF" parameter assignments for FB159. FB159 is described in Chapter 4.

NOTE:
Because of the processing time required by the 6ES5 242 module when a control word is received, you must allow a period of 500 microseconds for the module to process the control word.

If the module receives another control word in less than 500 microseconds, the first process will be interrupted. You can test the Ready bit of the INTI register to be sure that the module has processed its last control word and is available for communication.

CTRL - Byte — Subaddres xxx0, Write

Bit	7	6	5	4	3	2	1	0
	Control Words			Counter Selection				

3.6.1 Control Words: CTRL7 - CTRL5

These three bits are used to determine which function will be performed.

CTRL 7 6 5	FB159 "BEF"	Title and Description
0 0 0	PA	Parameter assignment; the parameters for the selected counters will be transferred from transfer memory area on the module to the counters.
0 0 1	ST	Start counter; the selected counters will be started. This is a software start.
0 1 0	LO	Load counter; the selected counters will be loaded from either the Load or the Hold register depending on which counting mode is used.
0 1 1	LS	Load & Start counter; the selected counters will be loaded and started in the same operation. This can also be considered an ARM command for a counting mode with a hardware trigger.
1 0 0	CO	Copy H to E; for the selected counters, the contents of the Hold register will be transferred to the counter.
1 0 1	SA	Save counter; for the selected counters, the contents of the counter will be transferred to the Hold register. This operation does not affect the operation of the counter.
1 1 0	SP	Stop counter; theselected counters will be stopped or disarmed. DISARM command.
1 1 1		Addition functions of the CTRL register are called. These functions are described in the next section. Bits 4 thru 0 of the CTRL register perform differently than they do in the abovementioned funtions.

3.6.2 Additional Functions

The additional functions of the CTRL register are listed below. It is necessary for bits 7 - 5 to set to "1" to call the additional functions. The equivalent "BEF" titles for FB159 are also listed for each of the functions.

CTRL 4 3 2 1 0	FB159 "BEF"	Title and Description
0 0 0 0 1	RB	Reset module; this function will perform an overall reset of the module. All parameters assigned will be deleted.
0 0 0 1 0	FL	Load predefined function; this function will load the predefined function whose number has been previously placed in the FNR register. See Section 3.7 for a detailed description of the FNR register.
0 0 0 1 1	RI	Reset interrupts; this function is used to reset the interrupts in the INTI register to "0". See Section 3.2 for a detailed description on the INTI register.
0 1 0 0 1	S1	Step counter; this function will step the selected counter by a count of one. The counter will be incremented or decremented depending on the value of bit CM3 for the selected counter.
0 1 0 1 0	S2	
0 1 0 1 1	S3	
0 1 1 0 0	S4	
0 1 1 0 1	S5	

NOTE:
All codes not described above are illegal.

3.6.3 Counter Selection: CTRL4 - CTRL0

The counter selection bits CTRL4 - CTRL0, are used for those functions described in Section 3.6.1. These bits are not used for counter selection when the additional functions of the CTRL register are used (see the previous section).

CTRL Bits 4 3 2 1 0
Counter 5 4 3 2 1

0 = not selected 1 = selected

When using the functions described in Section 3.6.1, any or all of the counters may be selected by setting the appropriate bits. To ensure the proper operation of a particular function, it is important to ensure that all of the registers involved have been loaded or preset before executing the function.

For example, if you would like to perform a start operation on counters 1 and 3, it is important to have the appropriate values in the CM, MM, Load, and Hold registers for each of the counters prior to the execution of the start function.

3.7 FNR - Function Number Register

The FNR register is used to point the module to the predefined function that is to be performed. These predefined functions can be stored in a 4K byte user EPROM installed on the module. Up to 254 function numbers can be assigned (00H thru FEH). There are also several predefined functions located in the modules firmware. These functions are described below.

When executing a predefined function, it is first necessary to store in the FNR register the function number that will be performed. Then by using the Control Register, the predefined function may be loaded in to the counter. This was described in the previous section. If you are using the standard software, then the "BEF" parameter of FB159 will be set to "FL" to perform a load of a predefined function.

The firmware for the module contain five predefined functions (firmware version V04). These function numbers and their meanings are described below.

FNR	Description
00H	Test for AM 9513, counter chip
01H	Test module RAM
02H	Test module EPROM
03H	Test for AM 9519, interrupt controller
04H	LOZI

The LOZI function will cause Counters 1-3 to be loaded from Load register after an interrupt has occurred from the gate interrupts 1 - 3. These gate interrupts are caused directly from the gate inputs 1 - 3 and are masked by the INTM register. See Section 3.1 for more information about the INTM register.

The operation of the first four function of the V04 firmware can be checked by reading the FEM register. The FEM register is described in the next section.

3.8 FEM - Error Signal Register

The FEM register allows you to determine which error has occurred when the Error bit of the INTI register is set (INTI, bit 14).

FEM - Low Order Byte — Subaddress xxx3, Read

Bit	7	6	5	4	3	2	1	0
	not assigned	IN	NR	CO	PA	TI	RO	RA

FEM - High Order Byte — Subaddress xx2, Read

Bit	15	14	13	12	11	10	9	8
				not assigned				

0 = no error 1 = error

3.8.1 Error Descriptions

FEM Bit	Name	Title & Description
0	RA	RAM test; will be set if an error has occurred while performing FNR 01H
1	RO	EPROM test; will be set if an error has occurred while performing FNR 02H
2	TI	AM 9513 test; will be set an error has occurred while performing FNR 00H
3	PA	Parameter assignment; will be set if a parameter has been assigned incorrectly
4	CO	Command; will be set if an incorrect control word has been used in the CTRL register
5	NR	Function number; will be set if a predefined function that does not exist is stored in the FNR register
6	IN	AM 9519 test; will be set if an error has occurred while FNR 03H
7-15		not assigned.

3.9 Result Of Counter Registers

The Result of Counter registers are 16-bit registers that allow you to read the current counter value. The counter contents are transferred to the transfer memory area of the module and are then available to the user. Reading a result of counter register does not affect the counter operation.

While using the standard software, the "BEF" parameter of FB159 will be "LE" in order to read the result of counter registers. This parameter is described in detail in Chapter 4 of this manual.

Counter	Add	Byte	Description
1	xxx6 xxx7	High Low	E1; Result of Counter Register 1
2	xxx8 xxx9	High Low	E2; Result of Counter Register 2
3	xxxA xxxB	High Low	E3; Result of Counter Register 3
4	xxxC xxxD	High Low	E4; Result of Counter Register 4
5	xxxE xxxF	High Low	E5; Result of Counter Register 5

At this time, there are two standard software function blocks that can be used with the 6ES5 242 counter module. They are FB158 which is used to initialize the module; and FB159 which is used by an application program to communicate the module.

These two function blocks will support the needs of most countig applications. Special applications will require the creation of custom function blocks. To that end, additional information in this section will provide the framework to follow as an example.

4.1 Function Block 158

Function block 158 is used to initialize the module when the PC is first powered up or after a cold or warm restart. Each module within a PC must have a call from FB158. These calls should be placed in the proper organizational blocks for your PC type.

4.1.1 Organization Blocks for FB158

Calls to FB158 should be placed in the listed organization blocks according to Table 4-1.

Table 4-1 Organization Block Calls

135U SYSTEM:

OB20 Manual Cold restart without memory
OB21 Manual Cold restart with memory
OB22 Automatic Warm restart with memory

115U SYSTEM:

OB21 Initial start from stop
OB22 Initial power on sequence

150 SYSTEM:

OB20 Manual Cold restart
OB21 Manual Warm restart
OB22 Automatic Warm restart

4.1.2 Explanation of FB158

The listing in Figure 4-1 illustrates FB158 as it will appear whwn it is called on the programming unit. Also listed is an explanation for each of the parameters used within the function block.

```
FB158 PER:ZTP
0000   NAME : PER: ZTP
0001   BGDB :      KY128,235
0002   P/Q  :      KSP  only 150S/135U (see Software
0003   PAFE :      F 191.4                 description)
0004   BFEH :      F 191.5
0005   SFEH :      F 191.6
0006        : ***
```

Figure 4-1 Function Block 158

4.1.3 Parameter BGDB

BGDB:

The first byte specifies the module's peripheral address; i.e., 128. The address range is from 128 to 240. Switch S1 on the module is used to select this address.

The second byte points to the data block that is assigned to this address. The data block must be opened to at least 70 data words. This data block will explained in detail in a later section.

4.1.4 Parameter P/Q (only 150S/135U)

P/Q:

This parameter specifies which peripheral area the module is located. P = Normal peripheral area. Q = Extended peripheral area. The KS format is used.

4.1.5 Parameter PAFE

PAFE:

Parameter assignment error flag. If the assigned bit is set, the user must check Flag Byte 255 to determine the error.

255.0 = address range incorrect
255.1 = not used
255.2 = data block not defined
255.3 = data block is too short or non-existent
255.4 = not used
255.5 = not used
255.6 = not used
255.7 = not used

4.1.6 Parameter BFEH

BFEH:

Specifies the hardware error flag. (Module Self Test)

4.1.7 Parameter SFEH

SFEH:

Specifies the general error flag. This flag will set if either PAFE or BFEH is set.

4.2 Function Block 159

Function Block 159 is available to the user for control of the 17 functions provided by the 6ES5 242 module. These functions are determined using the BEF parameter. All of the parameters associated with FB159 are described in this section.

4.2.1 Explanation of FB159

The listing in Figure 4-2 illustrates FB159 as it will appear when it is called on the programmer. Also listed is an explanation of each within the function block.

```
FB159 PER:ZST

0000   NAME : PER: ZST
0001   BG   :       KF+128
0002   P/Q  :       KSP  only 150S/135U (see Software
                    description)
0003   Z4-1  :      KH0001
0004   Z--5  :      KH0000
0005   BEF   :      KSIN
0006   DBDW :       KY235,0
0007   ABIT  :      KY0,0
0008   INTL  :      FB117
0009   FEML  :      FB201
000A   PAFE  :      F 191.3
000B          : ***
```

Figure 4-2 Function Block 159

4.2.2 Parameter BG

BG:

This parameter specifies the module's peripheral address, i.e. 128. The address range is from 128 to 240. Switch S1 on the module is used to select this address.

4.2.3 Parameter P/Q

P/Q: (only 150S/135U)

This parameter specifies which peripheral area the module is located. P = Normal peripheral area. Q = Extended peripheral area. The KS format is used.

4.2.4 Parameters Z4-1 and Z--5

Z4-1:

Counter selection. The user must identify which counter this FB call will enable. The bit definitions are as follows: KH4321.

KH1000 = Counter 4 selected
KH0100 = Counter 3 selected
KH0010 = Counter 2 selected
KH0001 = Counter 1 selected
KH0000 = Counter 1 thru 4 not selected

It is possible to select more than one counter, e.g.
KH00111 = Counter 1, 2, 3 is selected.

Z--5:

This parameter is used in conjunction with Z4-1. By setting bit zero counter 5 is selected. Bits 1 thru 3 have no meaning and should be set to zero; i.e., KH0005.

KH0001 = Counter 5 selected
KH000 = Counter 5 not selected

4.2.5 Parameter BEF

BEF:

Function selection parameter. This parameter allows you to select the function assignments that the function block call will be performing. Remember that you must call FB159 each time a different function is to be performed. Below is a list and explanation of the 17 different functions available for the 6ES5 242 module.

1. PA - Parameter assignment. When this function is used the function block will transfer the values of five data words, which are defined in DBDW, to the counter module. The counter you have selected will determine which data word will be pointed to in DBDW. Below is a list of the DBDW values for each counter. For an explanation of meanings of each of the five data words, refer to the next section.

   Counter 1, DBDW = data block = xx, data word = 11
   Counter 2, DBDW = data block = xx, data word = 18
   Counter 3, DBDW = data block = xx, data word = 25
   Counter 4, DBDW = data block = xx, data word = 32
   Counter 5, DBDW = data block = xx, data word = 38

2. ST - Start counter. This function will start the counter or counters which have been selected. The value in the DBDW parameter is irrelevant.
3. LO - Load counter. This function will load the counter or counters selected, with the values found in the DB selected in FB158 and the DWs for the particular counter. Below is a list of data word locations that must contain the values to be loaded for each counter. Again, the value in the DBDW parameter is irrelevant.

   Counter 1, data block = xx, data word = 14
   Counter 2, data block = xx, data word = 21
   Counter 3, data block = xx, data word = 28
   Counter 4, data block = xx, data word = 35
   Counter 5, data block = xx, data word = 42

4. LS - Load and start. This function combines the LO and the ST functions. The same rules apply for the load portion of this function as they do for the LO-function.
5. CO - Copy H register into the E register. This function will copy the contents of the hold register (H) to the result of counter register (E) for the counter or counters selected. The counter should be stopped when this command is used to prevent the transferred value from being changed.
6. SA - Save counter value in the H register. This function will read the value of the counter or counters selected without modifing the value in the counter, and place the value in the H register. To read the value stored in the Hold register, you must first use a CO command to transfer the contents of the Hold register to the E register. Then you must use an LE command to read the value of the counter into the data block. Note that the counter should be stopped when the last commands are executed.
7. SP - Stop counter. This function will stop the counter or counters selected. The DBDW parameter value is irrelevant.
8. RB - Reset module. This function will reset the 242 counter module. Resetting will delete any parameters that have been assigned.

9. FL - Load predefined function. This function is used to call a pre-defined function that has been stored in EPROM 2. A 4k byte memory area is available on the module for this purpose.

   Each user program must be identified with a function numbers (FN). Up to 254 function numbers can be assigned, the range being from 00H to EFH. This function, FL, is used to tell the module which function number (FN) is to executed.

   The function number must be stored in a function number register (FNR). The FNR is actually the left byte of a data word pointed to by the DBDW parameter; i.e., DBDW: KY200,3 will tell FB159 that the FNR is the value in DB200, DW3. If DB200, DW3 = KH0A00, the function number to be executed would be FN10. The FNR must be loaded before the call to FB159.

10. RI - Reset interrupts. This function will reset the ABIT parameter bit, the INTL flag byte will also be reset. Note that the ABIT parameter is not used with the S5-135U and 115U.

11. - 15. S1 thru S5 - Step counter. This function allows you to single step counters 1 thru 5 (S1 thru S5). The counter will be incremented or decremented by one count depending on the counter's selected counting direction. To step a counter five times for example, the FB would have to be called five times.

16. LE - Read counter. This function will read the values of the counter or counters selected and place the value in a result of counter register. These values will then be placed in an eight data word block within the DB selected.

    The parameter DBDW is used to point to the data word which will be the first word of the eight word block. Note, the DB in parameter DBDW must be the same DB as in FB158. The first data word must be greater than 51. For an explanation of the meaning of each data word in the eight word block refer to the next section. The eight word block will start at DW60; i.e., DBDW: KY235,60.

17. IN - Reset interrupt bit. This function is used to reset the interrupt flags in the ABIT and INTL parameters.

4.2.6 Parameter DBDW

DBDW:

This parameter is used to point to the data block and data word for some of the BEF parameter modes. A list of which functions of the BEF parameter require a value to be placed in the DBDW parameter.

BEF parameters requiring a DBDW value:

PA	Parameter assignment
LE	Read Counter

BEF parameters not requiring a DBDW value:

ST	Start counter
LO	Load counter
LS	Load and start counter
CO	Copy H to E
SA	Save counter to H
SP	Stop counter
RB	Reset module
FL	Load predefined function
RI	Reset interrupts
S1	Step counter 1
S2	Step counter 2
S3	Step counter 3
S4	Step counter 4
S5	Step counter 5
IN	Reset interrupt bit

4.2.7 Parameter INTL

INTL:

Interrupt flag byte. If the module recognizes a group interrupt the source of the error can be found by reading the INTL Byte.

4.2.8 Parameter FEML

FEML:

Error flag byte. This byte represents the low order byte of the FEM register.

4.2.9 Parameter PAFE

PAFE:

Parameter assignment error flag. If the assigned bit is set then the user must check Flag Byte 255 to determine the error.

255.0 = address range incorrect
255.1 = Parameter P/Q is not defined
255.2 = data block not defined
255.3 = data block is too short or non-existant
255.4 = BEF parameter error
255.5 = not used
255.6 = no counter defined
255.7 = not used

4.3 Standard Software Data Blocks

For each module that is installed within a PC there must be a data block. This data block is as an area where the values needed to manipulate the counter module are to be stored. The data block must be openned to a minimum of 70 data words. The following list shows the assignment of the data words for the data block.

Table 4-2 Data Block Assignments

DW 0 -
DW 9 - Working area - Not to be assigned by user
DW10 - Counter 1 KHFFFF; must value
DW11 - Interrupt Mask Register (INTM)
DW12 - Master Mode Register (MM)
DW13 - Counter Mode Register (CM)
DW14 - Load Register (L)
DW15 - Hold Register (H)
DW16 - Alarm Register (A)

DW17 - Counter 2 KHFFFF; must value
DW18 - Interrupt Mask Register (INTM)
DW19 - Master Mode Register (MM)
DW20 - Counter Mode Register (CM)
DW21 - Load Register (L)
DW22 - Hold Register (H)
DW23 - Alarm Register (A)

DW24 - Counter 3 KHFFFF; must value
DW25 - Interrupt Mask Register (INTM)
DW26 - Master Mode Register (MM)
DW27 - Counter Mode Register (CM)
DW28 - Load Register (L)
DW29 - Hold Register (H)
DW30 - unused

DW31 - Counter 4 KHFFFF; must value
DW32 - Interrupt Mask Register (INTM)
DW33 - Master Mode Register (MM)
DW34 - Counter Mode Register (CM)
DW35 - Load Register (L)
DW36 - Hold Register (H)
DW37 - unused

DW38 - Counter 5 KHFFFF; must value
DW39 - Interrupt Mask Register (INTM)
DW40 - Master Mode Register (MM)
DW41 - Counter Mode Register (CM)
DW42 - Load Register (L)
DW43 - Hold Register (H)
DW44 - unused

DW45 - Error Register Counter 1
DW46 - Error Register Counter 2
DW47 - Error Register Counter 3
DW48 - Error Register Counter 4
DW49 - Error Register Counter 5
DW50 - Test/Load Register
DW51 - unused

Greater than DW 51 - Assigned by the LE function of the BEF parameter. In the example, DW 60 is used as the first data word.

DW60 - Interrupt Information Register (INTI)
DW61 - Error Signal Register (FEM)
DW62 - unused
DW63 - Result of Counter 1 Register (E1)
DW64 - Result of Counter 2 Register (E2)
DW65 - Result of Counter 3 Register (E3)
DW66 - Result of Counter 4 Register (E4)
DW67 - Result of Counter 5 Register (E5)
Open to DW70

4.4 FB159 Usage

This section is meant to provide the user with some hints on how to use FB159 properly.

4.4.1 Access Time

Because of the access time required by FB159, a cycle time exceeded error may occur if repeated calls to the function block are performed. If this happens it may be required for the user to reset the watchdog timer in the PC before making a call to FB159. This can be accomplished by making a jump to the appropriate organizational block for the PC being used.

4.4.2 MM and INTM Registers

Because there is only one master mode (MM) register and only one interrupt information register (INTM) on the module it is only necessary to set them once.

The structure of FB159 is such that each time a counter is parameterized (BEF, PA function) the MM and INTM values contained in the data block are sent to the module. Because the MM and INTM registers on the module reflect the value of the last parameterized counter, it is necessary for the user to pay close attention to the values stored in the data block for each counters MM and INTM values. An example of this is given below.

If the user would like to set the MM register to a value of 3EH, the values in the data block are as show below.

DW12	3EH	MM counter 1
DW19	00H	MM counter 2
DW26	00H	MM counter 3
DW33	00H	MM counter 4
DW40	00H	MM counter 5

In order for the MM register to be set to the correct value, it would be necessary to use the PA function for counter 1 after the using the PA for any of the other counters. For example:

1. - PA counter 1; the MM register will be set to 3EH
2. - PA counter 3; the MM register will be set to 00H
3. - PA counter 1; the MM register will again be set to 3EH

This is a simple example and it could easily be changed to operate properly, but this is not the point. The idea of the example is to show that while using the PA function it is necessary to make sure that once the MM or the INTM is set, that it is not changed without the user being aware of the change.

A solution to this problem would be to write the values for the MM and INTM registers in each of the data words for the five counters. This way the user will not have to be concerned that the MM register or the INTM register values will be changed on each PA function call.

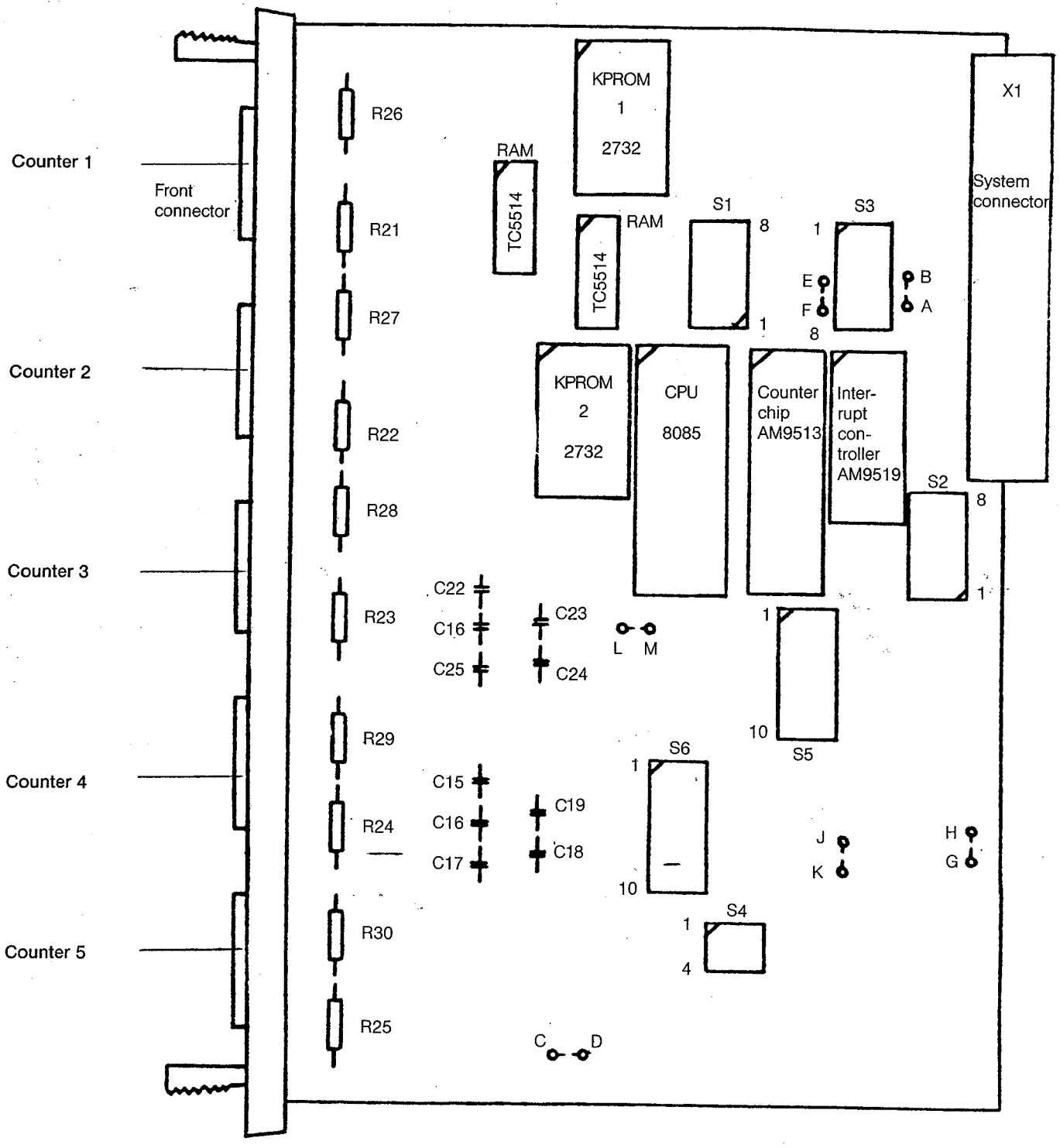
4.4.3 Alarms Registers

The AM 9513 counter chip and therefore the 6ES5 242 module are organized in such a manner that only counters 1 and 2 have alarm registers available to them for use. These registers are used to provide a comparison value, when the compare function is enabled in the MM register.

FB159 in turn provides an alarm register value for each of the five counters within the data block. Only the values for counters 1 and 2 are of any use. The values for counters 3, 4, and 5 are irrelevant. The associated data words within the data block are listed below.

DW16 Alarm register for Counter 1, active
DW23 Alarm register for Counter 2, active
DW30 Alarm register for Counter 3, irrelevant
DW37 Alarm register for Counter 4, irrelevant
DW44 Alarm register for Counter 5, irrelevant

APPENDIX A
Module Layout



Module Address = _____

MM = | _ _ _ _ | _ _ _ _ | _ _ _ _ | _ _ _ _ |

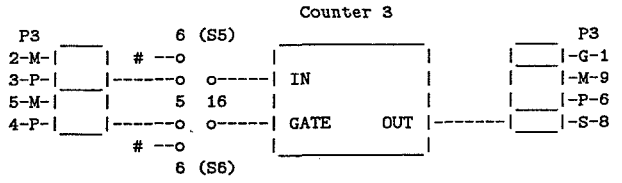
Pulse Source = Counter __ | Gate __ | Scaler 1 F__ | n-1 __ |

Scaling Factor = ____ FOUT = "#"

Scaler 1 outputs

F1 = 2 MHZ F2 = 200 KHZ F3 = 20 KHZ F4 = 2 KHZ F5 = 200 HZ

Counter 3

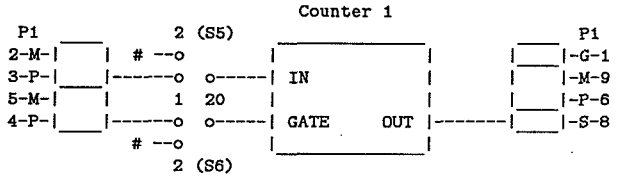


Pulse Source = Counter __ | Gate __ | Scaler 1 F__ | n-1 __ |

CM = | _ _ _ _ | _ _ _ _ | _ _ _ _ | _ _ _ _ |

Alarm = _____ Load = _____ Hold = _____

Counter 1

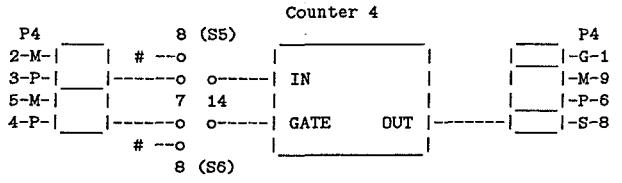


Pulse Source = Counter __ | Gate __ | Scaler 1 F__ | n-1 __ |

CM = | _ _ _ _ | _ _ _ _ | _ _ _ _ | _ _ _ _ |

Alarm = _____ Load = _____ Hold = _____

Counter 4

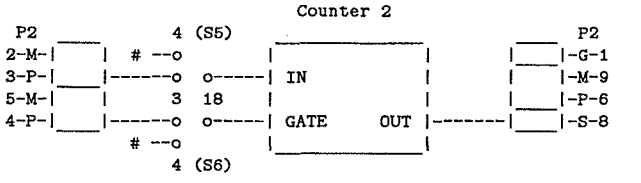


Pulse Source = Counter __ | Gate __ | Scaler 1 F__ | n-1 __ |

CM = | _ _ _ _ | _ _ _ _ | _ _ _ _ | _ _ _ _ |

Alarm = _____ Load = _____ Hold = _____

Counter 2

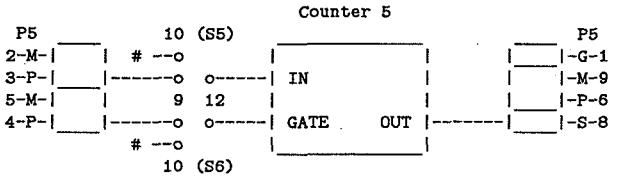


Pulse Source = Counter __ | Gate __ | Scaler 1 F__ | n-1 __ |

CM = | _ _ _ _ | _ _ _ _ | _ _ _ _ | _ _ _ _ |

Alarm = _____ Load = _____ Hold = _____

Counter 5



Pulse Source = Counter __ | Gate __ | Scaler 1 F__ | n-1 __ |

CM = | _ _ _ _ | _ _ _ _ | _ _ _ _ | _ _ _ _ |

Alarm = _____ Load = _____ Hold = _____