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Automation System S7-400 CPU Specifications

Reference Manual

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Safety Guidelines

This manual contains notices intended to ensure personal safety, as well as to protect the products and connected equipment against damage. These notices are highlighted by the symbols shown below and graded according to severity by the following texts:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

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indicates that minor personal injury can result if proper precautions are not taken.

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Notice

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Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

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Note the following:

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This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

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Preface

Purpose of the Manual

The manual contains reference information on operator actions, descriptions of functions and technical specifications of the central processing units, power supply modules and interface modules of the S7-400.

How to configure, assemble and wire these modules (and other) in an S7-400 system is described in the installation manuals for each system.

Required Basic Knowledge

You will need general knowledge of automation to understand this manual.

Target Group

General knowledge in the field of automation technology is presumed.

Prerequisite is also sufficient knowledge in the use of computers or PC–type equipment (programming devices, for example) with Windows 2000 or XP operating system. The S7-400 system is configured in STEP 7 standard software. You should therefore have sufficient knowledge of this standard software. This knowledge is provided in the “Programming with STEP 7” manual.

Please note the information on the safety of electronic control systems in the appendix of this manual, in particular when operating an S7-400 in safety–relevant areas.

Scope of this Manual

The manual applies to the S7-400 automation system, including the following CPUs:

- CPU 412-1; (6ES7412-1XF04-0AB0)
- CPU 412-2; (6ES7412-2XG04-0AB0)
- CPU 414-2; (6ES7414-2XG04-0AB0)
- CPU 414-3; (6ES7414-3XJ04-0AB0)
- CPU 416-2; (6ES7416-2XK04-0AB0)
- CPU 416-2F; (6ES7416-2FK04-0AB0)
- CPU 416-3; (6ES7416-3XL04-0AB0)
- CPU 417-4; (6ES7417-4XL04-0AB0)

Approvals

You can find details on approvals and standards in the “Module Data” reference manual.

Place of this Documentation in the Information Environment

This manual is part of the documentation package for S7-400.

System	Documentation Package
S7-400	• *S7-400 Programmable Controller*; *Hardware and Installation* • *S7-400 Programmable Controllers; Module Data* • *Automation System S7-400; CPU Data* • *S7-400 Instruction List*

Navigating

The manual offers the following access help to make it easy for you to find specific information:

- At the start of the manual you will find a complete table of contents and a list of the diagrams and tables that appear in the manual.
- An overview of the contents of each section is provided in the left column on each page of each chapter.
- You will find a glossary in the appendix at the end of the manual. The glossary contains definitions of the main technical terms used in the manual.
- At the end of the manual you will find a comprehensive index which gives you rapid access to the information you need.

Standard Software for S7 STEP 7 Basics	• Installing and commissioning STEP 7 on a programming device / PC • Working with STEP 7 in the following context: Project and file management S7-400 configuration and parameter assignment Assigning symbolic names to user programs Creating and testing a user program in STL/LAD Creating data blocks Configuring the communication between CPUs Downloading, uploading, saving and deleting user programs on the CPU / programming device Monitoring and controlling user programs Monitoring and controlling the CPU • Guide to the efficient implementiation of programming tasks using the programming device / PC and STEP 7 • Operating principle of the CPUs (for example, memory concept, I/O access, addressing, blocks, data management) • Description of STEP 7 data management • Using data types of STEP 7 • Using linear and structured programming • Using block call instructions • Utilizing debug and diagnostic functions of the CPUs in the user program (for example, error OBs, status word)
STEP 7 Reference Information *Statement List (STL) for S7-300 and S7-400* *Ladder Logic (LAD) for S7-300 and S7-400* *Function Block Diagram (FBD) for S7-300 and S7-400* *System and Standard Functions*	• Basics on working with STL, LAD, or FBD (for example, structure of STL, LAD, or FBD, number formats, syntax) • Description of all STEP 7 instructions (with program examples) • Description of the various addressing options of STEP 7 (with examples) • Description of the internal registers in the CPU • Description of all integrated system / standard functions of the CPUs • Description of all integrated organization blocks of the CPUs

Recycling and Disposal

The S7-400 is low in contaminants and can therefore be recycled. To recycle and dispose of your old device in an environment-friendly manner, please contact a disposal company certified for disposal of electronic waste.

Further Support

If you have any further questions related to the use of your product for which you have not found an answer in this documentation, please contact your Siemens partner at your local Siemens office.

You can find your contact partner under:

`http://www.siemens.com/automation/partner`

A guide to out technical documentation for the various SIMATIC products and systems is found under:

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The online catalog and order system is found under:

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Training Centers

We offer various courses to newcomers to the SIMATIC S7 programmable logic controller. For details, please contact your regional training center or our central training center in D 90327 Nuremberg, Germany:

Phone: +49 (911) 895-3200.

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- A forum, where users and experts from all over the world exchange their experiences.
- Your local representative for Automation & Drives.
- Information on field service, repairs, spare parts and more under “Services”.

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Structure of a CPU 41x

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1.1 Control and display elements of the CPUs

Controls and display elements of the 412-1 CPU

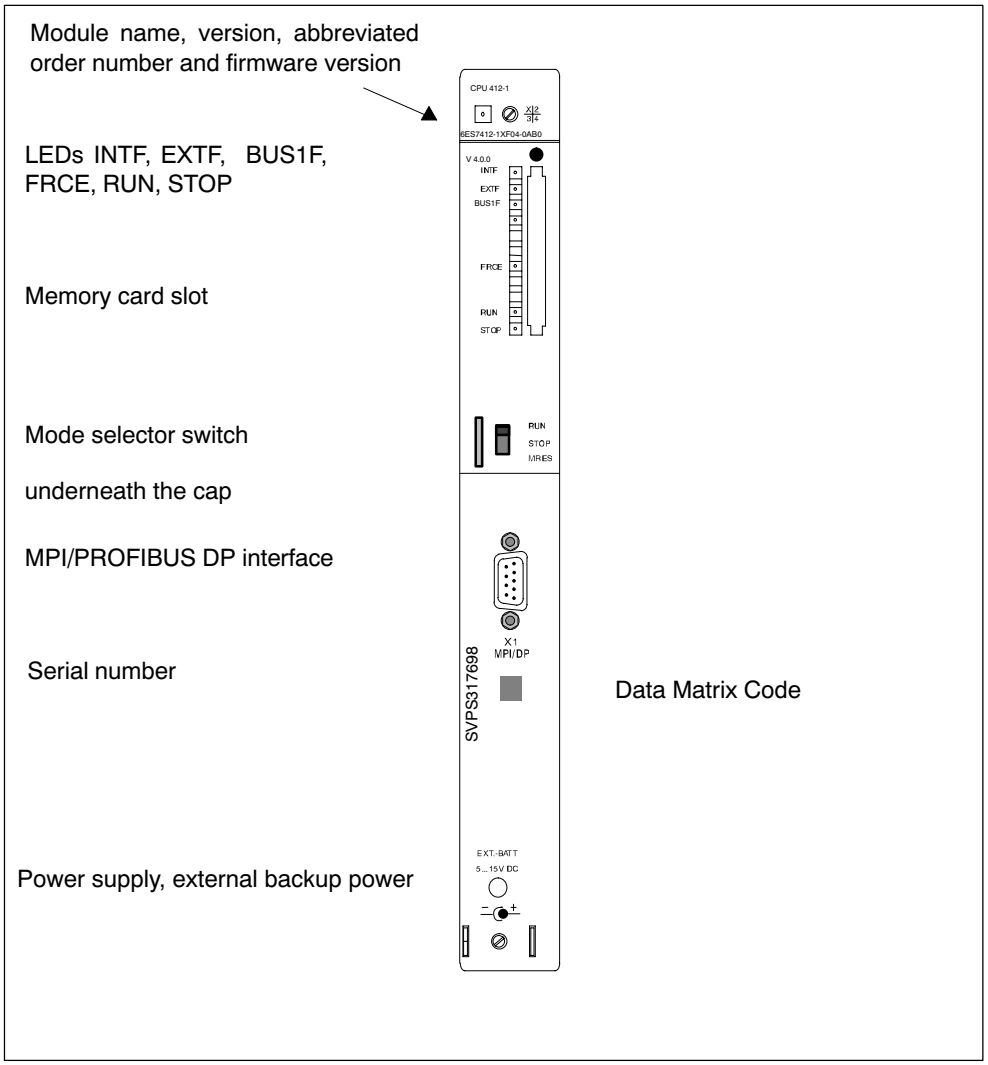


Figure 1-1 Layout of the control and display elements of a 412-1 CPU

Controls and display elements of the 41x-2 CPU

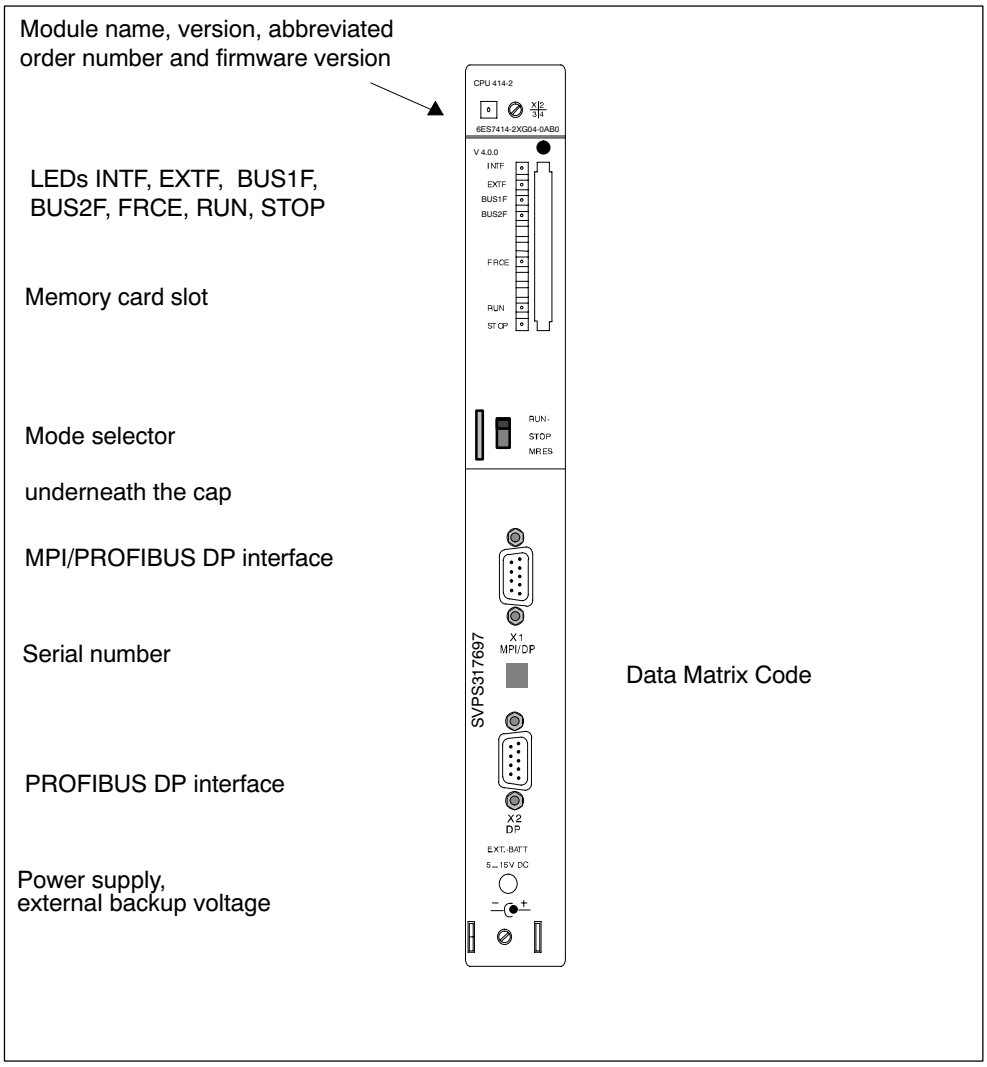


Figure 1-2 Layout of the control and display elements of the 41x-2 CPU

Controls and display elements of the 41x-3 CPU

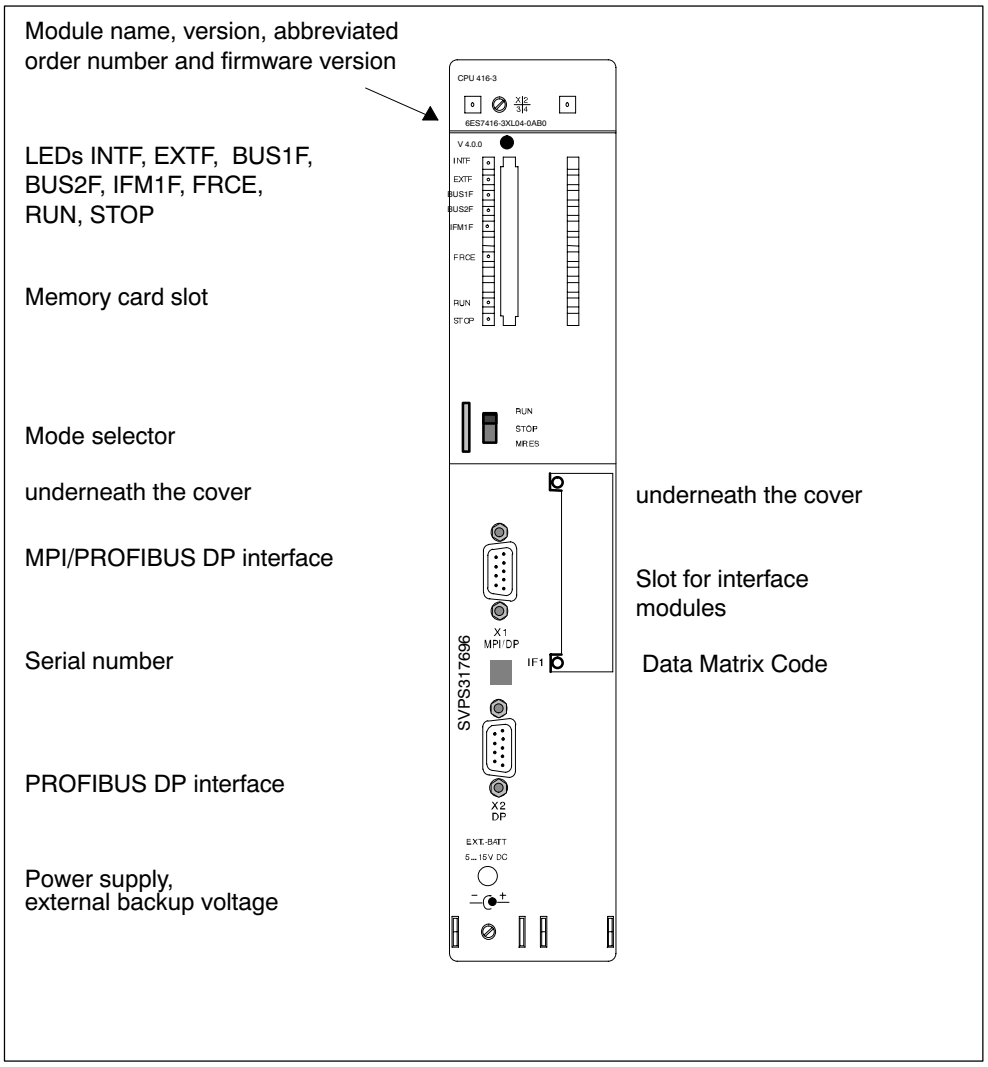


Figure 1-3 Layout of the control and display elements of the 41x-3 CPU

Controls and display elements of the 417-4 CPU

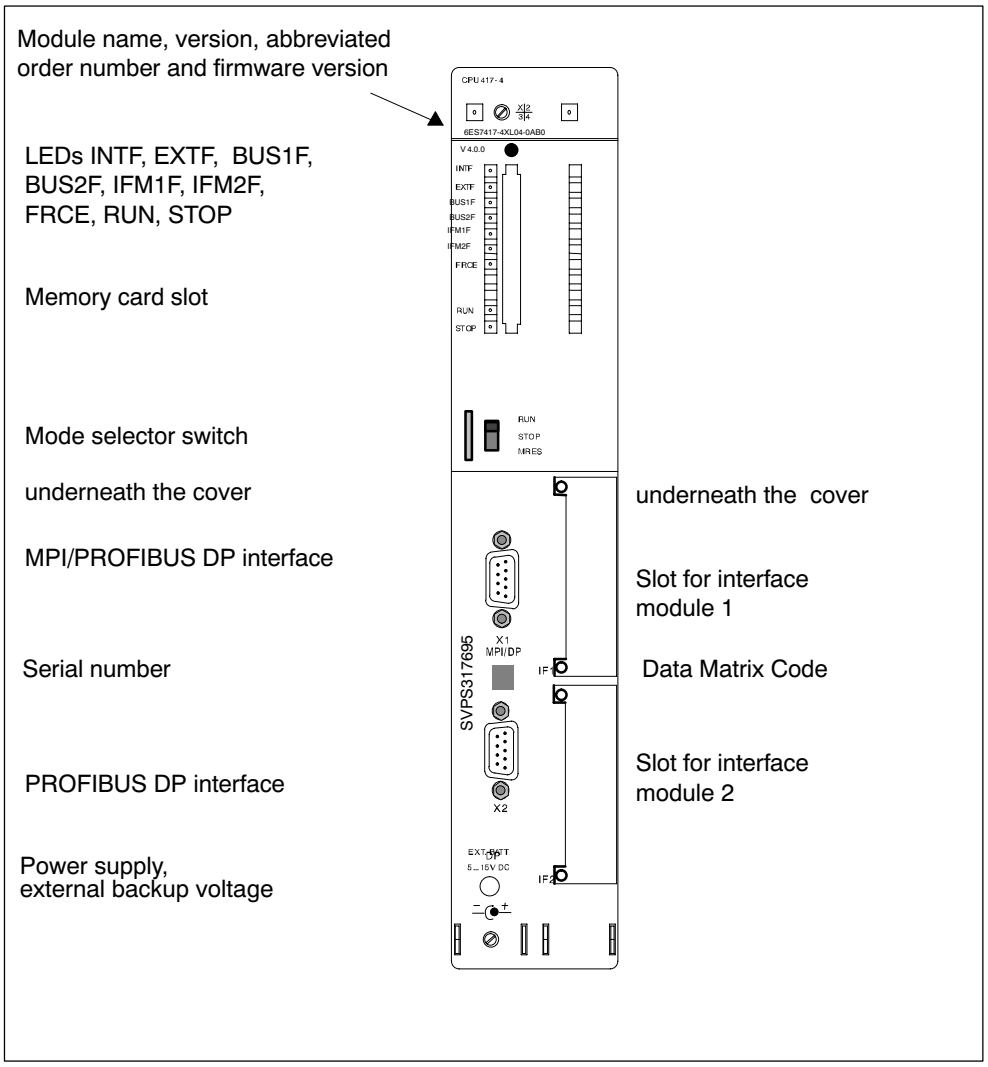


Figure 1-4 Layout of the control and display elements of the 417-4 CPU

LED displays

Table 1-1 gives you an overview of the LEDs on the individual CPUs.

Section 1.2 describes the states and errors indicated by these LEDs.

Table 1-1 LEDs of the CPUs

LED	Color	Meaning	CPU			
			412-1	412-2 414-2 416-2	414-3 416-3	417-4
INTF	red	Internal error	x	x	x	x
EXTF	red	External error	x	x	x	x
FRCE	yellow	Active force request	x	x	x	x
RUN	green	RUN mode	x	x	x	x
STOP	yellow	STOP mode	x	x	x	x
BUS1F	red	Bus error at MPI/PROFIBUS DP interface 1	x	x	x	x
BUS2F	red	Bus error at PROFIBUS DP interface 2	–	x	x	x
IFM1F	red	Error at interface submodule 1	–	–	x	x
IFM2F	red	Error at interface submodule 2	–	–	–	x

Mode selector switch

You can use the mode selector to select the current operating mode of the CPU. The mode selector is a three-position toggle switch.

Section 1.4 describes the functions of the mode selector switch.

Memory Card slot

You can insert a memory card into this slot.

There are two types of Memory Card:

- RAM cards

  For the expansion of CPU load memory.

- FLASH cards

  Non-volatile memory for storing the user program and data (retentive without backup battery). You can either program the FLASH card on the programming device or in the CPU. The FLASH card also expands the load memory of the CPU.

  For a detailed description of the Memory Cards, refer to Chapter 1.5.

Slot for Interface Modules

This slot holds one interface module (IF module) for 1x-3 and 41x-4 CPUs .

MPI/DP interface

Devices you can connect to the MPI interface of the CPU, for example:

- Programming devices
- Control and monitoring devices
- Further S7-400 or S7-300 PLCs (see chapter 1.6).

Use the bus connector with angular cable outlet (see the manual *Hardware and Installation*, Chapter 7)

You can also configure the MPI interface as DP master in order to use it as PROFIBUS DP interface with up to 32 DP slaves.

PROFIBUS DP interface

Lets you connect the distributed I/O, programming devices/OPs and further DP master stations.

POwer supply, external backup voltage at the “EXT.-BATT.” connector

You can install either one or two backup batteries in the S7-400 power supply modules, depending on the module type. By doing so, you:

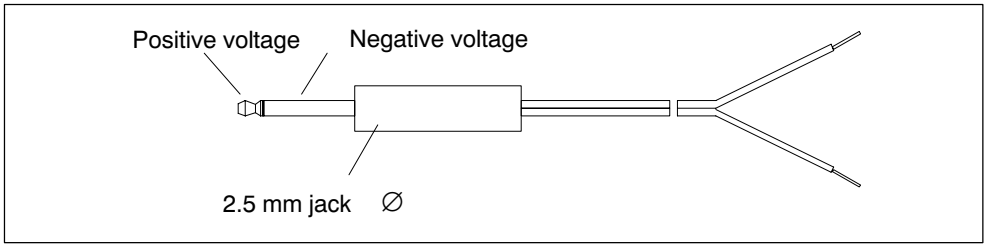
- Backup the user program in RAM memory.
- Retain the values of flags, timers, counters, system data and data of dynamic DBs.
- Backup the internal clock.

You can achieve the same effects by supplying a voltage between 5 V DC and 15 V DC to the “EXT.-BATT.” connector of the CPU.

Properties of the “EXT.-BATT.” input:

- Polarity reversal protection
- Short-circuit current limited to 20 mA

You need a cable with a 2.5 mm ∅ jack to connect the power suplpy to the “EXT.-BATT” socket, as shown in the following illustration. Note the polarity of the jack.



Note

You require the external power supply to the “EXT.-BATT.” socket when you replace a power supply module and want to backup the user program in RAM and the data mentioned earlier while you are replacing the module.

1.2 Monitoring functions of the CPU

Monitoring and error messages

The CPU hardware and the operating system monitoring functions ensure proper functioning of the system and a defined reaction to errors. Certain error events will also trigger a reaction in the user program. When recursive errors occur, the LED is switched off with the next incoming error.

The table below provides an overview of possible errors, their causes and the reactions of the CPU.

Type of Fault/Error	Cause of Fault	Response of the Operating System	Error LED
Access error , incoming	Module failure (SM, FM, CP) I/O write access error I/O read access error	The ”EXTF” LED stays lit until the error is acknowledged. In SMs: • Call of OB122 • Entry in the diagnostic buffer • At input modules: “NULL” entry of for the date in the accumulator or the process image On other modules: • Call of OB122	EXTF
Time-out error, incoming	• The user program execution time (OB1 and all interrupt and error OBs) exceeds the specified maximum cycle time. • OB request error • Overflow of the startup buffer • Watchdog interrupt • Resume RUN after CiR	The ”INTF” LED is lit until the error is acknowledged. Call of OB80 If this OB is not loaded: The CPU goes into STOP.	INTF
Faulty power supply module(s) (not mains failure), incoming and outgoing error	In the central or distributed I/O rack: • At least one backup battery of the power supply module is low. • Backup voltage is missing. • The 24 V DC supply of the power supply module has failed.	Call of OB81 If this OB is not loaded: The CPU continues RUN.	EXTF
Diagnostic Interrupt (incoming and outgoing)	An I/O module with interrupt capability reports a diagnostic interrupt.	Call of OB82 If this OB is not loaded: The CPU goes into STOP.	EXTF
Removal /insertion interrupt (incoming and outgoing)	Removal or insertion of an SM and insertion of the wrong module type. The LED EXTF will not light up if only one SM is installed and then removed while the CPU is in STOP (default configuration). The LED lights up briefly when the SM is inserted again.	Call of OB83 If the OB is not loaded: The CPU goes into STOP mode.	EXTF
CPU Hardware error (incoming)	• A memory error was detected and eliminated	Call of OB84 If this OB is not loaded: The CPU continues RUN.	INTF
Priority class error (Only incoming, depending on the OB85 mode	• A priority class is called, but the corresponding OB is not available. • In the case of an SFB call: The instance DB is missing or faulty.	Call of OB85 If this OB is not loaded: The CPU goes into STOP.	INTF

Type of Fault/Error	Cause of Fault	Response of the Operating System	Error LED
or incoming and outgoing)	• Error while updating the process image		EXTF
Rack / station failure (incoming and outgoing)	• Power failure on an expansion module • DP segment error • Failure of a coupling segment: missing or defective IM, cable break)	Call of OB86 If this OB is not loaded: The CPU goes into STOP.	EXTF
Communication error (incoming)	• Unable to enter status information in the DB • Invalid message frame ID • Frame length error • Error in the structure of the shared datagram • DB access error	Call of OB87	INTF
Execution cancelled (incoming)	• Synchronous error nesting depth exceeded • Too many nested block calls (B stack) • Error when allocating local data	Call of OB88 If the OB is not loaded: The CPU goes into STOP mode.	INTF
Programming error (incoming)	Error in the machine code or user program: • BCD conversion error • Range length error • Range error • Alignment error • Write error • Timer number error • Counter number error • Block number error • Block not loaded	Call of OB121 If the OB is not loaded: The CPU goes into STOP mode.	INTF
Code error (incoming)	Error in the compiled user program (e.g. ilegal OP code or a jump has violated block boundaries)	CPU goes into STOP mode. Restart or CPU memory reset required.	INTF
Loss of the clock signal (incoming)	When using clock sync mode: The clock signal was lost either because OB61 ... 64 was not started due to higher priorities, or because additional asynchronous bus loads suppressed the bus clock.	Call of OB80 If the OB is not loaded: The CPU goes into STOP Call of OB 61..64 at the next pulse.	INTF EXTF

Further test and information functions are available in each CPU and can be called in STEP 7.

1.3 Status and error displays

Status displays

The two RUN and STOP LEDs on the front panel of the CPU indicate the current CPU operating state.

LED		Meaning
RUN	STOP	
H	D	CPU is in RUN.
D	H	CPU is in STOP. The user program is not processed. Restart and warm restart/reboot is possible. If the STOP status was triggered by an error, the error indication (INTF or EXTF) is also set.
B 2 Hz	B 2 Hz	CPU status is FAULTY. The INTF, EXTF and FRCE LEDs also flash.
B 0.5 Hz	H	CPU HOLD was triggered by a test function.
B 2 Hz	H	A warm restart / cold restart / hot restart was triggered. It can take a minute or longer to execute these functions, based on the length of the OB called. If the CPU still does not go into RUN, there might be an error in the system configuration.
x	B 0.5 Hz	The CPU requests memory reset.
x	B 2 Hz	CPU memory reset is active.

D = LED is dark; H = LED is lit; B = LED flashes at the specified frequency; x = LED status is irrelevant

Error displays and special features, all CPUs

The three LEDs INTF, EXTF and FRCE on the front panel of the CPU indicate errors and special features in user program execution.

LED			Meaning
INTF	EXTF	FRCE	
H	x	x	An internal error was detected (program or configuration error) or the CPU is performing a CiR.
x	H	x	An external error was detected (that is, the cause of error cannot be traced back to the CPU module).
x	x	H	A force job is active.

H = LED is lit; x = LED status is irrelevant

The LEDs BUSF1 and BUSF2 indicate errors at the MPI/DP and PROFIBUS DP interfaces.

LED		Meaning
BUS1F	BUS2F	
H	x	An error was detected at the MPI/DP interface.
x	H	An error was detected at the PROFIBUS DP interface.
B	x	DP master: One or more slaves at PROFIBUS DP interface 1 are not responding. DP slave: not addressed by the DP master
x	B	DP master: One or more slaves at PROFIBUS DP interface 2 are not responding. DP slave: not addressed by the DP master

H = LED is lit; B = LED flashes; x = LED status is irrelevant

Error displays and special features, 41x-3 and 41x-4 CPUs

41x-3 and 41x-4 CPUs are still equipped with the IFM1F or IFM1F and IFM2F LEDs. These indicate errors at the first and second IFM.

LED		Meaning
IFM1F	**IFM2F**	
H	x	An error was detected at module interface 1.
x	H	An error was detected at module interface 2.
B	x	DP master: No response from one or several slaves connected to the PROFIBUS DP interface module in slot 1 DP slave: not addressed by the DP master
x	B	DP master: No response from one or several slaves conected to the PROFIBUS DP interface in slot 2 DP slave: not addressed by the DP master

H = LED is lit; B = LED flashes; x = LED status is irrelevant

Diagnostic buffer

In STEP 7, you can select “PLC –> Module status” to read the cause of an error from the diagnostic buffer.

1.4 Mode selector switch

Function of the mode selector switch

The mode selector switch can be used to set the CPU to RUN or STOP mode, or to reset the CPU memory. STEP 7 offers further mode selection options.

Positions

The mode selector switch is a toggle switch. Figure 1-5 shows the positions of the mode selector switch.

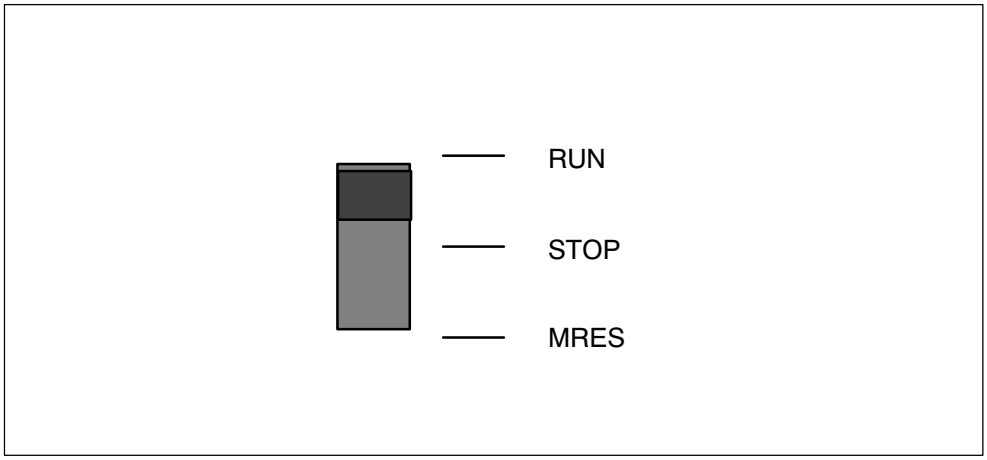


Figure 1-5 Positions of the mode selector switch

Table 1-2 descibes the positions of the mode selector switch. In the event of a fault or if there are problems preventing a startup, the CPU goes into STOP or retain this mode, regardless of the position of the mode selector switch.

Table 1-2 Positions of the mode selector switch

Position	Explanation
RUN	If there is no startup problem or error and the CPU was able to go into RUN, the CPU either executes the user program or remains idle. • You can upload programs from the CPU to the programming (CPU –> PG) • You can upload programs from the PG to the CPU (PG –> CPU).
STOP	The CPU does not execute the user program. The digital signal modules are locked. Programs can: • You can upload programs from the CPU to the programming (CPU –> PG) • You can upload programs from the PG to the CPU (PG –> CPU).
MRES (CPU memory reset; Master Reset)	Momentary-contact position of the toggle switch for CPU memory reset (see below).

Security classes

A security class can be agreed for S7-400 CPUs in order to prevent unauthorized access to CPU programs. You can define a security class which allows users access to PG functions without particular authorization (password). On password level you can access all PG functions.

Setting the security classes

You can set the security classes (1 to 3) for a CPU by calling STEP 7 –> HW Config.

You can delete the the security class set STEP 7 –> HW Config by means of a manual reset using the mode selector switch.

Table 1-3 lists the security classes of an S7-400 CPU.

Table 1-3 Security classes of an S7-400 CPU

Security class	Function
1	• Access to all programming device functions is allowed (default).
2	• Objects may be uploaded from the CPU to the PG. That is, only the read–only functions can be accessed on the PG. • Access to process control, process monitoring and process communication functions is allowed. • Access to the information functions is allowed.
3	• Access to process control, process monitoring and process communication functions is allowed. • Access to the information functions is allowed.

Sequence for CPU memory reset

Case A: You want to download all data of a new user program to the CPU.

1. Set the switch to STOP.

   Result: The STOP LED is lit.

2. Set the switch to MRES setting and hold it at this position.

   Result: The STOP LED performs this cycle: 1 sec OFF –> 1 sec ON –> 1 sec OFF –> continuous signal.

3. Reset the switch to STOP, then set MRES again within the next 3 seconds, then reset it to STOP.

   Result: The STOP LED flashes at least 3 seconds at 2 Hz (memory reset is being executed), then its signal is set continuously.

Case B: The CPU requests memory reset, indicated by the flashing STOP LED (5 Hz). The system requests a CPU memory reset after a memory card was removed or inserted, for example.

Set the switch to MRES and then return it to STOP.

Result: The STOP LED flashes at least 3 seconds at 2 Hz (memory reset is being executed), then its signal is set continuously.

For detailed information on CPU memory reset refer to chapter 6 of the manual *S7-400 Programmable Controllers Hardware and Installation*.

CPU sequence for memory reset

The CPU performs the following processes for memory reset:

- It deletes the user program from work memory and in load memory (integrated RAM or RAM Card).
- It deletes all counters, flags and timers (except the time).
- It performs a hardware selftest.
- It initializes the hardware and system program parameters, that is, its internal default settings. Some of the configured defaults are taken into account.
- When a FLASH Card is inserted and after the CPU memory reset is completed, the CPU loads the user program and the system parameters from the FLASH Card to work memory.

What is retained after a CPU memory reset...

The following data are retained:

- The contents of the diagnostics buffer can be read by uploading it to the PG in STEP 7.
- The parameters of the MPI interface (MPI address and highest MPI address). Note the special features shown in the table below.
- The time
- The status and value of the operating hours counter

Special feature: MPI parameters

A special situation is given for the MPI parameters when a CPU memory reset is preformed. The table below shows which MPI parameter remain valid after a CPU memory reset.

CPU memory reset ...	MPI parameters...
with FLASH Card	..., stored on the FLASH Card are valid
without FLASH Card	...are retained in the CPU and valid

Cold start

- During a cold start, all data (process image, flags, timers, counters and DBs) are reset to the start values stored in the program in load memory, regardless whether these are configured as retentive or non-retentive data.
- Program execution is restarted at the start position (OB100, OB101, OB102 or OB1).

Restart (warm start)

- A restart resets the process image and the non-retentive flags, timers, times and counters.

  Retentive flags, times and counters retain their last valid value.

  All DBs assigned the “Non Retain” attribute are reset to load values. The remaining DBs retain their last valid value.
- Program execution is restarted at the start position (startup OB or OB 1).
- After a power supply interruption, the warm restart function is only available in backup mode.

Hot restart

- When a hot restart is performed, all data and the process image retain their last valid value.
- Program execution is resumed at the breakpoint.
- The outputs do not change their status until the current cycle is completed.
- After a power supply interruption, the hot restart function is only available in backup mode.

Control sequence for restart (warm restart)

1. Set the switch to STOP.

   Result: The STOP LED is lit.
2. Set the switch to RUN.

Control sequence for hot restart

1. Select “hot restart” via PG.

   The correspondend button can be used only if a hot restart is possible whith your CPU.

Control sequence for cold restart

A cold start can only be initiated on the PG.

1.5 Structure and function of the Memory Card

Order numbers

The order numbers for memory cards are listed in chapter 6 of the technical specification.

Configuration

The memory card is slightly larger than a credit card and protected by a strong metal casing. It is inserted into a front slot of the CPU. The memory card casing is encoded to allow only one position of insertion.

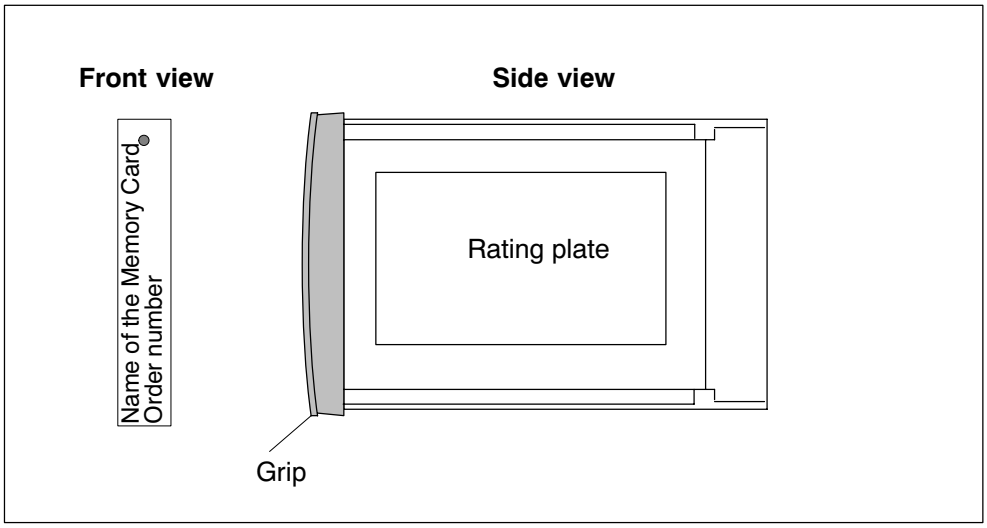


Figure 1-6 Structure of the Memory Card

Function

The memory card and an integrated memory area on the CPU together form the load memory of the CPU. In operation, the load memory contains the entire user program, including comments, symbols, special additional information that permits decompilation of the user program, and all the module parameters (see chapter 4.1).

What is stored on the Memory Card?

The following data can be stored on the memory card:

- User program, that is, blocks (OBs, FBs, FCs, DBs) and system data
- Parameters which determine the behavior of the CPU
- Parameters which determine the behavior of the I/O modules.
- In STEP 7 V5.1 or higher, all project data on suitable Memory Cards.

Types of Memory Cards for S7-400

Two types of memory card are used in the S7-400:

- RAM cards
- Flash cards (FEPROM cards)

Note

Non-Siemens memory cards cannot be used in the S7-400.

What type of Memory Card should I use?

Whether you use a RAM card or a Flash card depends on your application.

Table 1-4 Types of Memory Cards

If you ...	...Then
want to store the data in RAM and edit your program in RUN,	use a **RAM card**
want to backup your user program permanently on the memory card (without backup battery or outside the CPU),	use a **Flash card**

RAM Card

To use a RAM card and load the user program, you must insert it into the CPU slot. The user program is loaded with the help of the programming device (PG).

You can load the entire user program or individual elements such as FBs, FCs, OBs, DBs, or SDBs to the load memory in when the CPU is in STOP mode or RUN.

All data on the RAM Card are lost when you remove it from the CPU. The RAM card does not have a built-in backup battery.

If the power supply has a functioning backup battery or an external backup voltage is supplied to the CPU via the “EXT. BATT.” socket, the contents of the RAM card are retained after power is switched off, provided the RAM card stays in the CPU and the CPU stays in the rack.

Flash Card

With a Flash card, you have two options of loading the user program:

- Set the CPU to STOP using the mode selector, plug the Flash card into the CPU, then load the user program with
  STEP 7 “PLC –> Load User Program to Memory Card”.
- Load the user program into the Flash card in offline mode at the programming device or adapter and then insert the Flash card into the CPU.

You can only reload the full user program using the Flash card. You can load smaller program sections into the integrated load memory on the CPU using the programming device. In the case of extensive program changes, you must always reload the Flash card with the full user program.

The Flash card does not require a backup voltage, that is, the information stored on it is retained even when you remove the Flash card from the CPU or if you operate your S7-400 system without a buffering function (without backup battery in the power supply module or “EXT. BATT.” socket of the CPU).

Which Memory Card Capacity to Use

The capacity of the memory card is determined by the size of the user program and the additional memory requirements when using function modules or communications modules. For information on memory requirements, refer to the relevant module manuals.

To optimze utilization of work memory (code and data) on your CPU, you should expand the load memory of the CPU with a memory card which has at least the same capacity as the work memory.

Changing the Memory Card

To change the memory card:

1. Set the CPU to STOP.
2. Remove the memory card.

Note

If you remove the memory card, the CPU requests a memory reset in a 3-sec sequence, which is indicated by the flashing STOP LED. This sequence cannot be influenced by error OBs.

---

3. Insert the “new” memory card.
4. Reset CPU memory.

1.6 Multipoint Interface (MPI)

Connectable devices

You can connect the following stations to the MPI, for example:

- Programming devices (PG/PC)
- Control and monitoring devices (OPs and TDs)
- Additional SIMATIC S7 PLCs

Some devices use the 24 V DC power supply of the interface. This voltage connected to a reference potential.

PG/OP->CPU communication

A CPU is capable of maintaining several simultaneous online connections. Only one of these connections is reserved as default connection for a PG, and a second for the OP/ control and monitoring device.

For CPU-specific information on the number of connection resources of connectable OPs, refer to chapter 6 of the Technical Specifications.

Communication and interrupt response times

Notice
The interrupt reaction times may be extended by read / write operations involving the maximum data length (approx. 460 byte).

CPU -> CPU communication

There are three types of CPU-CPU communication:

- Data transfer by means of S7 basic communication
- Data transfer by means of S7 communication
- Data transfer by means of global data communication

For further information, refer to the “Programming with STEP 7” manual.

Connectors

Always use bus connectors with angular cable outlet PROFIBUS DP or PG cables used to connect devices to the MPI (see chapter 7 of the manual *Hardware and Installation*).

Multipoint interface as DP interface

You can also configure the MPI interface for operation as DP interface. To do so, you can reconfigure the MPI interface in SIMATIC Manager of STEP 7 . You can use this to set up a DP segment consisting of up to 32 slaves.

1.7 PROFIBUS DP Interface

Connectable devices

You can connect any compliant DP slave to the PROFIBUS DP interface.

Here, the CPU is operated either as a DP master or a DP slave which is connected via PROFIBUS DP field bus to the passive slave stations or other DP masters.

Some devices use the 24 V DC power supply of the interface. This voltage connected to a reference potential.

Connectors

Always use the bus connector for PROFIBUS DP or PROFIBUS cables used to connecting devices to the PROFIBUS DP interface (see chapter 7 of the manual *Hardware and Installation*).

1.8 Overview of the Parameters for the S7-400 CPUs

Default values

All parameters are assigned factory settings. These defaults are suitable for a whole range of standard applications, that is, an S7-400 can be used immediately as turnkey system which does not require any further settings.

You can define CPU-specific default values using the “HW Config” tool in STEP 7.

Parameter Blocks

The behavior and properties of the CPU are declared in the parameters which are stored in system data blocks. The CPUs are assigned default values. You can edit these default values by changing the parameters in HW Config.

The list below provides an overview of the configurable system properties of the CPUs.

- General properties (for example, the CPU name)
- Startup (for example, enabling a hot restart)
- Constant bus cycle time interrupts
- Cycles / memory flags (e.g. scan cycle cycle monitoring time)
- Retentivity (number of retentive tags, timers and counters)
- Memory (e.g. local data)

  Note: If you change the work memory allocation by modifying parameters, this work memory is reorganized when you load system data to the CPU. The result is, that the DBs which were generated by an SFC will be deleted, and the remaining DBs are assigned default initial values from load memory.

  Work memory space available for storing code or DBs can be reorganized when system data are loaded by changing the following parameters:

  – Size of the process image (byte–oriented; on the “Cycle / clock flag” tab)
  – Communication resources (on the “Memory” tab)
  – Size of the diagnostics buffers (on the “Diagnostics / clock” tab)
  – The amount of local data for all priority classes (“Memory” tab)
- Assignment of interrupts (process interrupts, delay interrupts, asynchronous error interrupts) to the priority classes
- Time-of-day interrupts (e.g. start, interval duration, priority)
- Watchdog interrupts (e.g. priority, interval duration)
- Diagnostics/clock (e.g. time synchronization)
- Protection levels

Note

16 memory bytes and 8 counter numbers are set to retentive in the default settings, in other words, they are not deleted when the CPU is restarted.

Parameter Assignment Tool

You can set the individual CPU parameters using “Configuring Hardware” in STEP 7.

Note

If you make changes to the existing settings of the following parameters, the operating system carries out initializations like those during cold restart.

- Size of the process image of the outputs
- Size of the process image of the inputs
- Size of the local data
- Number of diagnostic buffer inputs
- Communication resources

These initializations are:

- Data blocks are initialized with the load values
- Memory bits, times, counts, inputs and outputs are deleted regardless of the retentive settings (0)
- DBs generated via SFC are deleted
- Permanently configured, base communication connections are established
- All the priority classes start from the beginning again

Special functions of a 41x CPU

2

Chapter Overview

In Section	You Will Find	On Page
2.1	Read Service Data	2-2
2.2	Multicomputing	2-3
2.3	Modifications to the System During Operation	2-7

2.1 Reading Service Data

Requirements

This function requires STEP 7 V5.3 or higher.

When is this function used?

If you require service support, please contact your Siemens Customer Support Center. The Customer Support Center may request specific information about the status of the CPU in your system for analysis. This information is stored in the diagnostics buffer and in the actual service data.

Select the “PLC –> Save service data” menu command to read this information, then save the data to two files and send these to your Customer Support Center.

Please note:

- You should save all service data immediately after the CPU has changed to STOP, or when a redundant system has lost its synchronization.
- Always save the service data of both CPUs in the redundant system, that is, including the data of the CPU which is still in RUN after synchronization is lost.

The service data are written to the file <filename.ext> in the <pathname> path.

Procedure

1. Select the “PLC –> Save service data” menu command

   A dialog box opens where you can define a storage location and name for both files.

2. Save the files.
3. Send these files to your Customer Support Center upon request.

2.2 Multicomputing

Chapter overview

Section	Description	Page
2.2.1	Peculiarities	2-5
2.2.2	Multicomputing Interrupt	2-6
2.2.3	Configuring and programming multicomputing operation	2-6

What is multicomputing?

Multicomputing refers to the concurrent operation of several (max. 4) CPUs which are capable of multicomputing in a central S7-400 system.

The participating CPUs automatically change their status in synchronism. That is, all CPUs are in synchronism during startup and transitions to STOP. Every CPU executes its own user program, irrespective of the user programs in the other CPUs. This feature facilitates the execution of control tasks in parallel.

Which racks are suitable for multicomputing?

The racks listed below are suitable for multicomputing:

- UR1 and UR 2
- UR2-H, multicomputing with several CPUs is only possible if all CPUs are inserted in the same in the same unit.
- CR3, the CR3 is equipped only with four slots, that is, you can only operate two CPUs in multicomputing mode.

Difference between multicomputing mode and operation in a segmented rack

The segmented rack CR2 (physically segmented, can not be configured in the software) allows only one CPU per segment. This, however, is not a multicomputing system. The CPUs in the segmented rack form an independent unit and respond in the same way as single-processor systems. A shared logical address space does not exist.

Hence, multicomputing is not possible in segmented racks (see also the installation manual).

When do I use multicomputing?

In the following situations it is of advantage to use multicomputing:

- The size of your user program exceeds the capacity of a single CPU and you run out of storage space:
  distribute program execution to several CPUs.
- A certain part of your system requires high-speed processing:
  cut the relevant program section from the program and process it on a separate “high-speed” CPU.
- Your system consists of several units which can be easily partitioned and controlled independently:
  Execute system partition 1 on CPU 1 , system partition 2 on CPU 2, etc.

Example

The figure below shows a PLC operating in multicomputing mode. Each CPUs can access its assigned modules (FM, CP, SM).

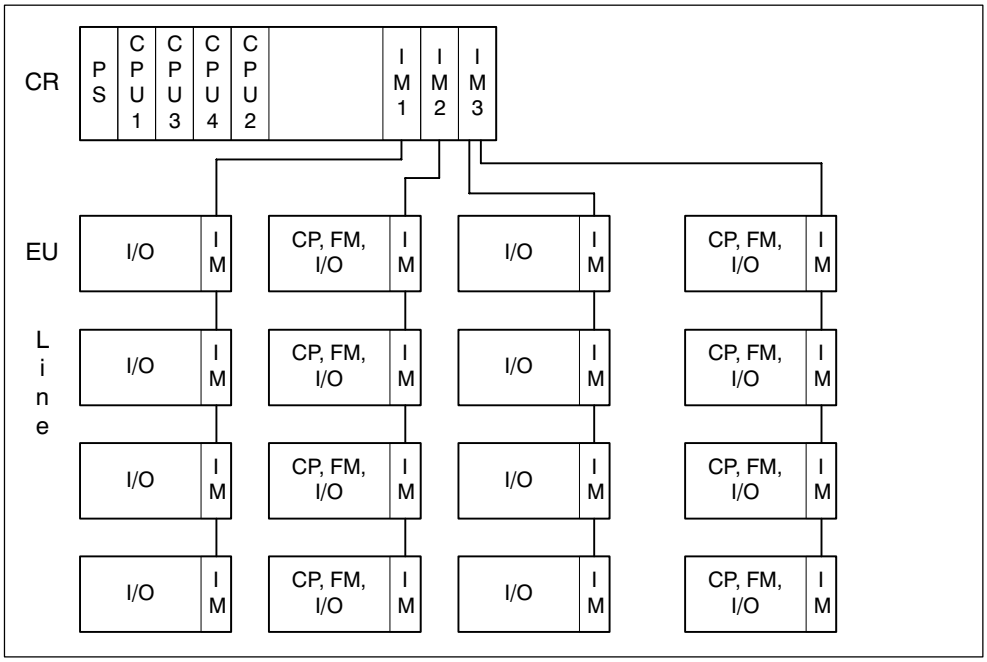


Figure 2-1 Multicomputing Example

2.2.1 Peculiarities

Slot Rules

In multicomputing operation, up to four CPUs can be inserted at the same time and in any order in a central controller (CC).

Bus Connection

The CPUs are interconnected via the communication bus (K bus). That is, if configured accordingly, all CPUs can be accessed by the PG via MPI interface.

Behavior at Startup and During Operation

During startup, all multicomputing CPUs automatically verify that they can operate in synchronism with each other. Synchronization is only possible if the requirements are satisfied:

- All configured CPUs (but only those) are inserted and fully functional.
- A proper configuration was created in STEP 7 and loaded to all CPUs in the rack.

If one of these conditions is not satisfied, an event with the ID 0x49A4 is output to the diagnostic buffer. For information on event IDs, refer to the reference help for standard and system functions.

When the CPU exits STOP mode, it compares the startup modes (COLD RESTART/RESTART (WARM RESTART) / HOT RESTART). With different startup modes, the CPUs do **not** switch to RUN mode.

Assignment of Addresses and Interrupts

In multicomputing mode, each CPU can access the modules it was assigned in the STEP 7 configuration. The address area of a module is always assigned exclusively to one CPU.

Each interrupt-capable module is therefore assigned to a CPU. Interrupts originating from such a module can not be received by the other CPUs.

Interrupt Processing

The following applies to interrupt processing:

- Process interrupts and diagnostic interrupts are only sent to one CPU.
- When a module fails or is removed or inserted, the interrupt is processed by the CPU that was assigned to the module in the STEP 7 configuration.
  Exception: A module insertion/removal interrupt output by a CP reaches all the CPUs, irrespective of the CP having been assigned to a CPU in the STEP 7 configuration.
- In the event of a rack failure, OB 86 is called on each CPU, including the CPUs which were not assigned a module in the faulty rack.

For further information on OB86, refer to the reference help on organization blocks.

I/O application specification

The typical I/O application specification of a PLC corresponds in multicomputing operation to the typical application specification of the CPU with the most resources. The relevant CPU-specific or DP master-specific typical application specifications cannot be exceeded in the individual CPUs.

2.2.2 Multicomputing Interrupt

Using the multicomputing interrupt (OB 60), you can respond synchronously to an event in multicomputing on the corresponding CPUs. In contrast to the process interrupts triggered by signal modules, the multicomputing interrupt can be output only by CPUs. The multicomputing interrupt is triggered by calling SFC 35 “MP_ALM“.

You will find more information in the *System Software for S7-300/400, System and Standard Functions* manual.

2.2.3 Configuring and programming multicomputing operation

Please refer to the manual *Configuring Hardware and Communication Connections with STEP 7* to find out how to configure and program the CPUs and the modules.

2.3 Modifications to the System During Operation

Certain changes can be made in the system configuration by means of CiR (Configuration in RUN) while the system is in RUN. Processing is halted for a brief period in order to accomplish this. The upper limit of this time period is set to one second by default but can be changed. During this time, the process inputs retain their most recent value (see the manual, *" Modifications to the System During Operation Using CiR"*

You can download a free copy of this manual from the Internet address:`http://www.siemens.com/automation/service&support`

You can modify the system during operation using CiR in system segments with distributed I/O. This requires a configuration as shown in the following illustration. To simplify the example, only one DP master system and one PA master system are shown. These restrictions do not apply in actual practice.

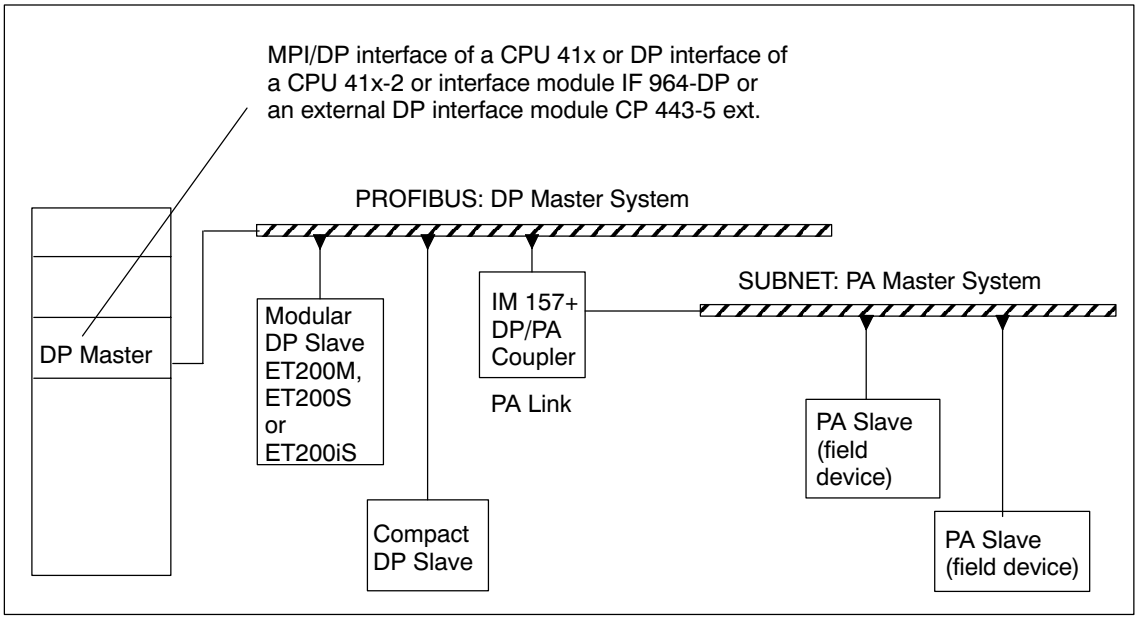


Figure 2-2 Overview: Architecture enabling modification of a system during operation

Hardware Requirements for Modification of a System During Operation

The following hardware requirements must have been fulfilled earlier in the commissioning phase in order to be able to subsequently modify the system during operation:

- An S7-400 standard CPU (CPU 412, CPU 414, CPU 416 or CPU 417), firmware V3.1 or later, or an S7-400-H-CPU (CPU 414-4H or CPU 417-4H) in single mode firmware V3.1 or later.
- If you wish to modify the system during operation on a DP master system with remote DP master (CP 443-5 extended), it must have firmware V5.0 or later.
- If you want to add modules for the ET 200M: Use the IM153-2 version MLFB 6ES7153-2AA03-0XB0 or later or the IM 153-2FO version MLFB 6ES7153-2BB00-0XB0 or later. You will also need to install the ET 200M with active bus elements and with enough free space for the planned expansion. You may not install the ET 200M as DPV0 slave (using a GSD file).
- If you wish to add entire stations: be sure to include the required bus connectors, repeaters, etc.
- If you wish to add PA slaves (field devices): use the IM157 version 6ES7157-0AA82-0XA00 or later in the corresponding DP/PA Link.
- The CR2 rack cannot be used.
- CP 444 and IM 467 modules can not be used within a station of which you want to modify the system configuation data in RUN by means of CiR.
- No multicomputing.
- No clocked operation on the same DP master system.

Note

You can freely mix components that are capable of system modification during operation and those that are not (except for the excluded modules, see above). However, you can modify the system configuration of components which are compatible with CiR.

Software Requirements for System Modifications During Operation

To be able to change a configuration in RUN mode, the user program must fulfill the following requirements: it must be written in such a way that station failures, module faults or exceeding cycle times do lead to a CPU STOP.

The following OBs are installed on the CPU:

- Process interrupt OBs (OB 40 to OB 47)
- Time-out error OB (OB 80)
- Diagnostic interrupt OB (OB 82)
- Insertion/removal OB (OB 83)
- CPU hardware error OB (OB 84)
- Runtime error OB (OB 85)
- Rack failure OB (OB 86)
- I/O access error OB (OB 122)

Permitted system modifications during operation: overview

The following modifications can be made to the system during operation:

- Add modules to the modular DP slave ET 200M, provided it has not been implemented as DPV0 slave (by means of GSD file)
- Reconfigure ET 200M modules, for example, modifying interrupt limits, or using the free channels.
- Use of the free channels of a module, or of a module of the ET 200M, ET 200S, ET 200iS modular slaves.
- Add DP slaves to an existing DP master system.
- Add PA slaves (field devices) to a PA master system
- Install DP/PA couplers downstream of an IM157
- Add PA Links (including PA master systems) to an existing DP master system
- Assign modules o a process image partition
- Reconfigure the modules of ET 200M stations (standard modules and fail-safe signal modules in standard mode).
- Undo modifications: for example, added modules, submodules, DP slaves and PA slaves (field devices) can be removed again.

Note

You can not add or remove slaves or modules, or make changes to a process image partition, on systems containing more than four DP masters.

Changes in RUN other than those specified earlier are not permitted and are excluded from this documentation.

S7-400 in PROFIBUS DP mode

3

Chapter overview

In section	You find	On Page
3.1	CPU 41x as DP Master/DP Slave	3-2
3.2	Direct Communication	3-31
3.3	Consistent Data	3-34

3.1 CPU 41x as DP Master/DP Slave

Introduction

This section contains the properties and technical specifications you require for using a 41x CPU as DP master or DP slave and to configure these for direct data exchange.

Agreed is: Because of the fact that DP master / DP slave behavior is the same for all CPUs, we refer to the CPUs described below as 41x CPU.

Further reference material

For information on the HW and SW configuration of a PROFIBUS subnet and on diagnostics functions within the PROFIBUS subnet, refer to the *STEP 7* Online Help.

3.1.1 DP address areas of 41x CPUs

Address areas of 41x CPUs

Table 3-1 CPUs 41x (MPI/DP Interface as PROFIBUS DP)

Address area	412-1	412-2	414-2	416-2
MPI interface as PROFIBUS DP, of inputs and of outputs [bytes]	2048	2048	2048	2048
DP interface as PROFIBUS DP, of inputs and of outputs [bytes]	–	4096	6144	8192
Of those in the process image, of inputs and of outputs Setting with up to x bytes	4096	4096	8192	16384

Table 3-2 CPUs 41x (MPI/DP Interface and DP Module as PROFIBUS DP)

Address area	414-3	416-3	417-4
MPI interface as PROFIBUS DP, of inputs and of outputs [bytes]	2048	2048	2048
DP interface as PROFIBUS DP, of inputs and of outputs [bytes]	6144	8192	8192
DP module as PROFIBUS DP, of inputs and of outputs [bytes]	6144	8192	8192
In the process image, of inputs and of outputs Setting with up to x bytes	8192	16384	16384

In the input address area, the **DP diagnostic addresses** occupy at least one byte for the DP master and each DP slave. The DP standard diagnosis for each node can be called at these addresses, for example (LADDR parameter of SFC 13). You define the DP diagnostic addresses in the configuration data, otherwise *STEP 7* assigns these automatically as DP diagnostic addresses in ascending order, starting at the highest byte address.

For DPV1 master mode, the slaves are usually assigned two diagnostic addresses.

3.1.2 41x CPU as PROFIBUS DP master

Introduction

This section provides information on the properties and technical data of a CPU operating in DP master mode.

Starting with section 6.1, you can find this information for 41x CPUs.

Requirements

You must configure the relevant CPU interface for operation in DP master mode. That is, in *STEP 7* you

- Configure the CPU as DP master
- Assign a PROFIBUS address
- Select an operating mode (S7-compatible or DPV1)
- Assign a diagnostic address
- Connect DP slaves to the DP master system

Note

Is one of the PROFIBUS DP slaves a 31x or 41x CPU?

If yes, you will find it in the PROFIBUS DP catalog as a “preconfigured station”. Assign this DP slave CPU a slave diagnostic address in the DP master. Interconnect the DP master with the DP slave, and define the address areas for data exchange with the DP slave.

From EN 50170 to DPV1 standard

The enhancements of the EN 50170 standard for distributed I/O were incorporated in IEC 61158 / IEC 61784-1:2002 Ed1 CP 3/1. The SIMATIC documentation refers to these as DPV1. The new version features a few additions and simplifications.

This DPV1 functionality is already implemented on certain SIEMENS automation components. Some slight modifications are required in order to enable this new functionality for your system. Information on the migration from EN 50170 to DPV1 is available on the Internet, on the FAQ pages “Changing from EN 50170 to DPV1”, FAQ ID 7027576, of the Customer Support.

Components supporting PROFIBUS DPV1 functionality

DPV1 masters

- S7-400 CPUs with integrated DP interface, with firmware V3.0 or higher.
- CP 443-5, order number 6GK7443-5DX03-0XE0, if used with one of these S7-400 CPUs.

DPV1 slaves

- DP slaves listed under their family name in the STEP 7 hardware catalog can be identified as DPV1 slave based on the included comment.
- DP slaves integrated in STEP 7 by means of GSD files, GSD Rev. 3 or higher.

STEP 7

STEP 7 V5.1 with Service Pack 2, or a higher version.

What are the operating modes for DPV1 components?

- S7-compatible

  In this mode, the components are compatible to EN 50170. Note that you can not utilize the full DPV1 functionality in this mode.

- DPV1 mode

  In this mode, you can utilize the full DPV1 functionality. Incompatible automation components in the station can be used as before.

DPV1 and EN 50170 compatibility

You can continue to use all existing slaves after the system conversion to DPV1. These are, however, do not support the enhanced function of DPV1.

DPV1 slaves can be implemented in system which are not converted to DPV1. In this case, their behavior corresponds with that of conventional slaves. SIEMENS DPV1 slaves can be operated in S7-compatible mode. For the DPV1 slaves of external manufacturers, you need a GSD file < Rev. 3 file to EN50170.

Migrating to DPV1

The migration to DPV1 applies to the entire station. You can set this DP mode in HW Config in STEP 7.

Further Information

Descriptions and information relating to the migration from PROFIBUS DP to PROFIBUS DPV1 is found on the Internet URL:

`http://www.siemens.com/automation/service&support`

Refer to ID 7027576

Monitor / modify, programming via PROFIBUS

The PROFIBUS DP interface is an alternative to the MPI interface you can use to program the CPU or execute the PG functions Monitor and Modify.

Note

The execution of programming and monitor/modify functions via PROFIBUS DP interface prolongs the DP cycle.

Constant bus cycle time

This is a property of PROFIBUS DP. The “Constant bus cycle time” function ensures that the DP master always starts the DP bus cycle within a constant interval. From the view of the slaves, this means that they receive their data from the master at constant time intervals.

In STEP 7 V 5.2 or higher, you can configure constant bus cycle times for PROFIBUS subnets.

Clocked update of process image partitions

SFC 126 “SYNC_PI“ is used for the clocked update of the process image partition of inputs. An application program which is interconnected to a DP cycle can use the SFC for consistent updates of the data recorded in the process image partition of inputs in synchronism with this cycle. SFC126 accepts interrupt control and can only be called in the OBs 61, 62, 63 and 64.

SFC 127 “SYNC_PO“ s used for the clocked update of the process image partition of ouptuts. An application program which is interconnected to a DP cycle can use the SFC for the consistent transfer of the computed output data of a process image partition of outputs to the I/O in synchonism with this cycle. SFC127 accepts interrupt control and can only be called in the OBs 61, 62, 63 and 64.

To allow clocked updates of process image partitions, all input or output addresses of a slave must be assigned to the same process image partition.

To ensure consistency of data in a process image partition, the following conditions must be satisfied on the various CPUs:

- CPU 412: number of slaves + number of bytes / 100 < 16
- CPU 414: number of slaves + number of bytes / 100 < 26
- CPU 416: number of slaves + number of bytes / 100 < 40
- CPU 417: number of slaves + number of bytes / 100 < 44

The SFCs 126 and 127 are descibed in the corresponding Online Help and in the “System and Standard Functions” manual.

Consistent user data

These are data which are associated in context and describe a process status at a given time. To ensure consistency, these data should not be modified or updated while being processed or transferred.

For details, refer to chapter 3.3.

SYNC/FREEZE

The SYNC control command is used to set sync mode at the DP slaves of selected groups. That is, the DP master transfers current output data and instructs the relevant DP slaves to freeze their outputs. The DP slaves writes the output data of the next output datagrams to an internal buffer; the state of the outputs remains unchanged.

Following each SYNC control command, the DP slaves of the selected groups transfer the output data stored in the internal buffer to the process outputs.

The outputs are only updated cyclically again after you transfer the UNSYNC control command using SFC 11 “DPSYC_FR”.

The FREEZE control command is used to set the relavant DP slaves to Freeze mode, that is, the DP master instructs the DP slaves to freeze the current state of the inputs. It then transfers the frozen data to the input area of the CPU.

Following each FREEZE control command, the DP slaves freeze the state of their inputs again.

The DP master receives the current state of the inputs cyclically again not until you have sent the UNFREEZE control command with SFC 11 “DPSYC_FR”.

For information on SFC 11, refer to the corresponding Online Help or to the “System and Standard Functions” manual.

Power-up of the DP master system

Use the following parameters to set power-up monitoring of the DP master:

- Transfer of the parameters to modules
- “Ready” message from the module

In other words, the DP slaves must power up and be configured by the CPU (as DP master) within the set time.

PROFIBUS Address of the DP Master

All PROFIBUS addresses are allowed.

3.1.3 Diagnostics of the CPU 41x as DP Master

Diagnostics Using LEDs

Table 3-3 explains the meaning of the BUSF LED.
The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 3-3 Meaning of the BUSF LED of the CPU 41x as DP Master

BUSF	Meaning	What to Do
Off	Configuration correct All configured slaves can be addressed	–
Lit	• Bus fault (hardware fault) • DP interface fault • Different transmission rates in multi-DP master mode	• Check for short-circuit or interruption of the bus cable. • Analyze the diagnosistic data. Reconfigure or correct the configuration.
Flashing	• Station failure • At least one of the assigned slaves can not be addressed	• Check whether the bus cable is connected to the CPU 41x or whether the bus is interrupted. • Wait until the CPU 41x has powered up. If the LED does not stop flashing, check the DP slaves or analyze the diagnosistic data of the DP slaves.
Flashes briefly INTF lights up briefly	CiR synchronization running	–

Initiating the detection of the Bus Topology in a DP Master System using SFC 103 “DP_TOPOL”

The diagnostics repeater is provided to enhance the options of locating faulty modules or DP cable interruptions when runtime errors have occurred. This module operates as a slave and can determine the topology of a DP slave and record any errors based on this information.

SFC 103 “DP_TOPOL” is used to initiate the detection of the bus topology of a DP master systems by means of the diagnostics repeater. SFC 103 is described in the corresponding Online Help and in the “System and Standard Functions” manual. For information on the diagnostics repeater, refer to the “Diagnostics Repeater for PROFIBUS DP” manual, order number 6ES7972-0AB00-8BA0.

Reading diagnosistic data in STEP 7

Table 3-4 Reading Out the Diagnosis with *STEP 7*

DP Master	Block or Tab in *STEP 7*	Application	Refer To...
CPU 41x	DP slave diagnostics tab	To display the slave diagnosis as plain text at the *STEP 7* user interface	See the section on hardware diagnostics in the *STEP 7* online help system and the *STEP 7* user guide
	SFC 13 “DPNRM_DG”	To read out the slave diagnosis (store in the data area of the user program)	For info on the structure of CPU 41x, see Section 3.1.5; SFC see the reference manual *System and Standard Functions* For info on the structure for other slaves, refer to the relevant sections
	SFC 59 “RD_REC”	To read out data records of the S7 diagnosis (store the data in the data area of the user program)	Reference Manual *System and Standard Functions*
	SFC 51 “RDSYSST”	To read out SSL sublists. Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	
	SFB 52 “RDREC”	For DPV1 slaves: To read out data records of the S7 diagnosis (store in the data area of the user program)	
	SFB 54 “RALRM”	For DPV1 slaves: To read out interrupt information within the associated interrupt OB	
	SFC 103 ”DP_TOPOL”	Triggers detection of the bus topology of a DP master system with diagnostic repeaters installed there.	

Analysis of diagnosistic data in the user program

The following figure shows you how to evaluate the diagnosis in the user program.

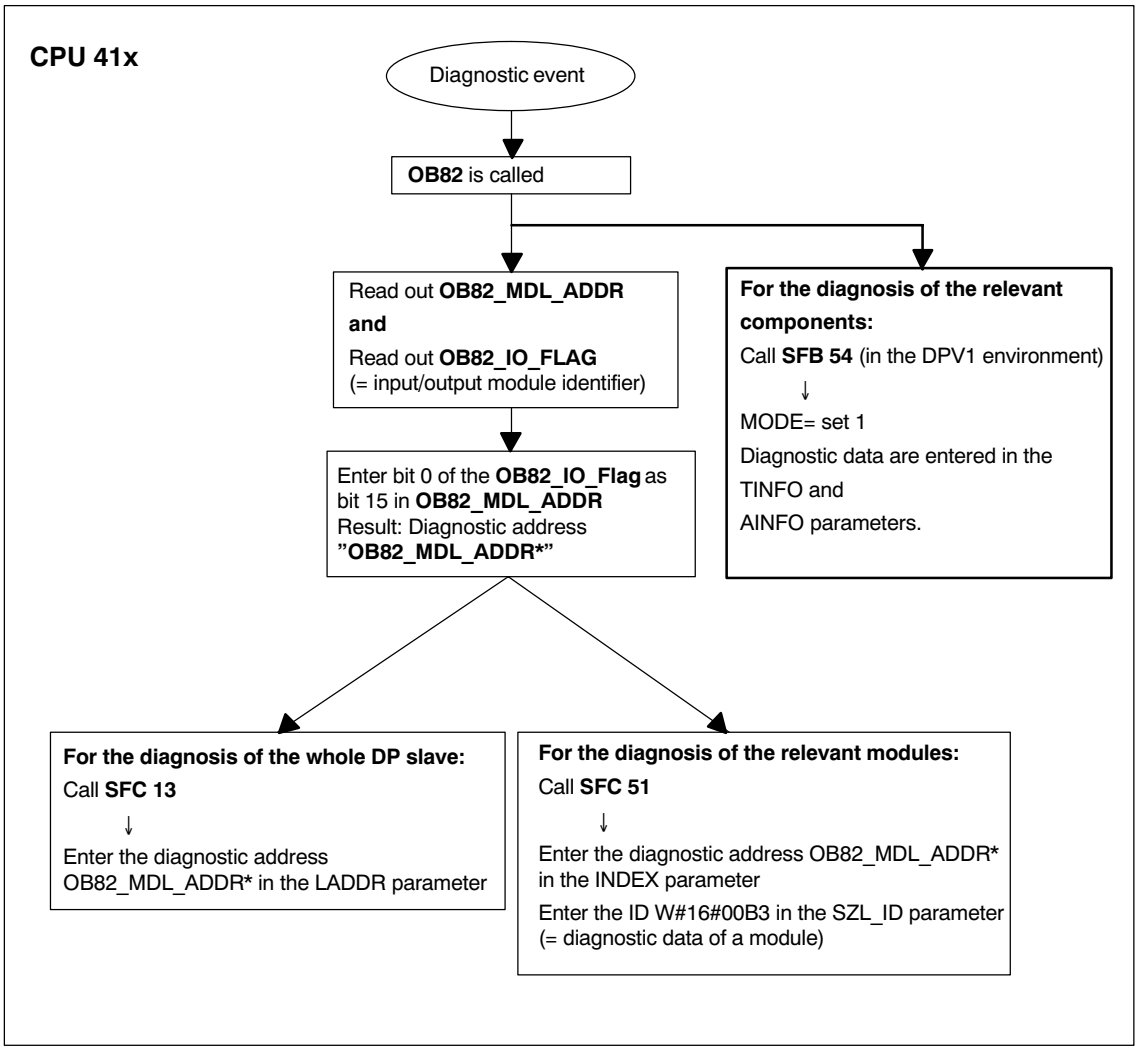


Figure 3-1 Diagnostics with CPU 41x

Diagnostic Addresses in Connection with DP Slave Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Ensure during configuration that DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

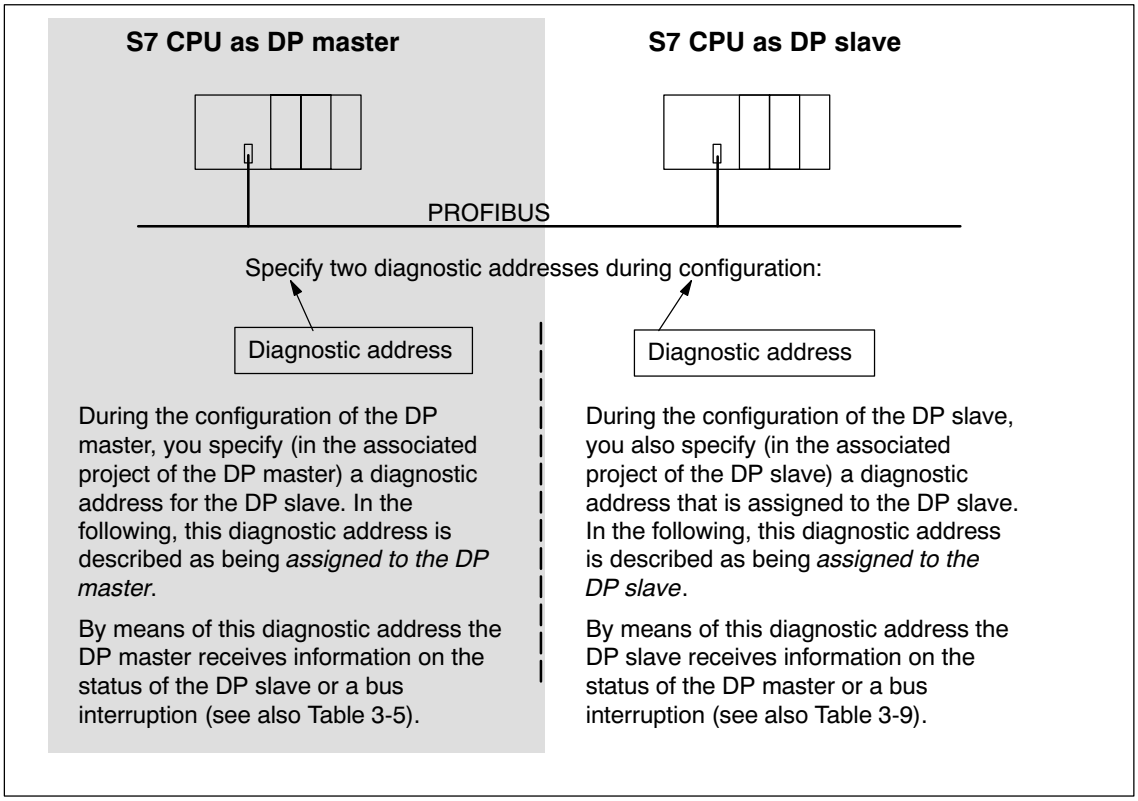


Figure 3-2 Diagnostic Addresses for the DP Master and DP Slave

Event Detection

Table 3-5 shows you how the CPU 41x as DP master detects any changes in the operating mode of a CPU as DP slave or interruptions in data transfer.

Table 3-5 Event Detection of the CPUs 41x as DP Master

Event	What Happens in the DP Master
Bus interruption (short circuit, connector removed)	• OB 86 called with the message *Station failure* (incoming event; diagnostic address of the DP slave that is assigned to the DP master) • In the case of I/O access: OB 122 called (I/O access error)
DP slave: RUN → STOP	• OB 82 is called with the message *Faulty module* (incoming event; diagnostic address of the DP slave that is assigned to the DP master; Variable OB82_MDL_STOP=1)
DP slave: STOP → RUN	• OB 82 is called with the message *Module OK.* (outgoing event; diagnostic address of the DP slave that is assigned to the DP master; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table shows you how, for example, you can evaluate RUN-STOP transitions of the DP slave in the DP master (see also Table 3-5).

In the DP Master		In the DP Slave (CPU 41x)
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**		Diagnostic addresses: (example) Slave diagnostic address=**422** Master diagnostic address=not relevant
The CPU calls OB 82 with the following information, amongst other things: • OB 82_MDL_ADDR:=**1022** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=module malfunction Tip: This information is also in the diagnostic buffer of the CPU You should also program the SFC 13 “DPNRM_DG” in the user program to read out the DP slave diagnostic data. We recommend you use SFB 54 in the DPV1 environment. It outputs the interrupt information in its entirety.	←	CPU: RUN → STOP CPU generates a DP slave diagnostic frame .

3.1.4 CPU 41x as DP Slave

Introduction

In this section we describe the features and technical specifications of the CPU if you operate it as a DP slave.

You can find the features and technical specifications of the CPUs 41x as of Section 6.1.

Requirements

1. Only one DP interface of a CPU can be configured as a DP slave.
2. Is the MPI/DP interface to be a DP interface? If so, you must configure the interface as a DP interface.

   Before commissioning you must configure the CPU as a DP slave. In other words, you must do the following in *STEP 7*

   – Activate the CPU as a DP slave

   – Assign a PROFIBUS address

   – Assign a slave diagnostic address

   – Define the address areas for data transfer to the DP master

GSD Files

You need a DDB file to configure the CPU as a DP slave in a third-party system.

You can download the GSD file free of charge from the Internet at http://www.ad.siemens.de/csi_e/gsd.

You can also download the GSD file from the mailbox of the Interface Center in Fürth on +49 (911) 737972.

Configuration and Parameter Assignment Frame

When you configure and assign parameters to CPU 41x, you are supported by *STEP 7*. If you require a description of the configuration and parameter assignment frame to carry out a check with a bus monitor, for example, you will find it on the Internet at http://www.ad.siemens.de/simatic-cs under the ID 1452338

Monitor/Modify, Programming via PROFIBUS

As an alternative to the MPI interface, you can use the PROFIBUS DP interface to program the CPU or execute the programming device functions Monitor and Modify. To do this, you must enable these functions when you configure the CPU as DP slave in *STEP 7*.

Note

The use of Programming or Monitor and Modify via the PROFIBUS DP interface extends the DP cycle.

Data Transfer Via an Intermediate Memory

As a DP slave the CPU 41x makes an intermediate memory available to PROFIBUS DP. Data transfer between the CPU as DP slave and the DP master always takes place via this intermediate memory. You can configure up to 32 address areas for this.

In other words, the DP master writes its data in these address areas of the intermediate memory and the CPU reads the data in the user program and vice versa.

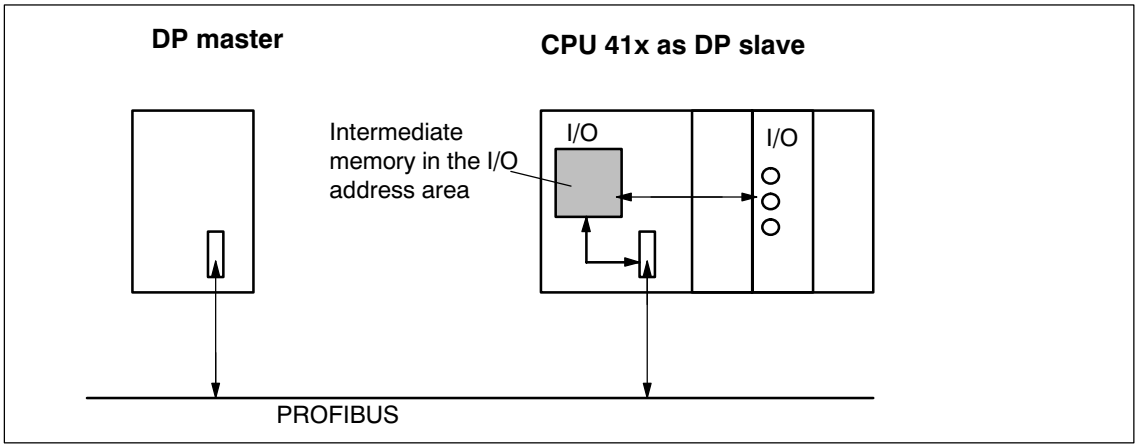


Figure 3-3 Intermediate Memory in the CPU 41x as DP Slave

Address Areas of the Intermediate Memory

Configure in *STEP 7* the input and output address areas:

- You can configure up to 32 input and output address areas.
- Each of these address areas can be up to 32 bytes in size
- You can configure a maximum of 244 bytes of inputs and 244 bytes of outputs in total

An example for the configuration of the address assignments of the intermediate memory is provided in the table below. You will also find this in the online help for STEP 7 configuration.

Table 3-6 Configuration Example for the Address Areas of the Intermediate Memory

	Type	Master Address	Type	Slave Address	Length	Unit	Consistency
1	e	222	A	310	2	Byte	Unit
2	A	0	e	13	10	Word	Total length
:							
32							
	Address areas in the DP master CPU		Address areas in the DP slave CPU		These parameters of the address areas must be the same for the DP master and DP slave		

Rules

You must adhere to the following rules when working with the intermediate memory:

- Assignment of the address areas:
  - Input data of the DP slave are **always** output data of the DP master
  - Output data of the DP slave are **always** input data of the DP master
- You can assign the addresses as you choose. You access the data in the user program with load/transfer commands or with SFCs 14 and 15. You can also specify addresses from the process image input and output table (see also section 3.1.1).

Note

You assign addresses for the intermediate memory from the DP address area of the CPU 41x.

You must not reassign the addresses you have already assigned to the intermediate memory to the I/O modules on the CPU 41x.

- The lowest address in each address area is the start address of that address area.
- The length, unit and consistency of address areas for the DP master and DP slave that belong together must be the same.

S5 DP Master

If you use an IM 308 C as a DP master and the CPU 41x as a DP slave, the following applies to the exchange of consistent data:

You must program FB 192 in the IM 308-C so that consistent data can be transferred between the DP master and DP slave. The data of the CPU 41x are only output or displayed contiguously in a block with FB 192.

S5-95 as DP Master

If you use an AG S5-95 as a DP master, you must also set its bus parameters for the CPU 41x as DP slave.

Sample Program

The small sample program below illustrates data transfer between the DP master and DP slave. This example contains the addresses from Table 3-6.

In the DP Slave CPU				In the DP Master CPU			
L	2		Preprocess data				
T	MB	6	in the DP slave				
L	EB	0					
T	MB	7					
L	MW	6	Transfer data to				
T	PQW	310	the DP master				
				L	PIB	222	Continue to
				T	MB	50	process received
				L	PIB	223	data in the DP
				L	B#16#3		master
				+	I		
				T	MB	51	
				L	10		Preprocess data
				+	3		in the DP master
				T	MB	60	
				CALL	SFC	15	Send data to the
				LADDR:= W#16#0			DP slave
				RECORD:= P#M60.0 Byte20			
				RET_VAL:= MW 22			
CALL	SFC	14	Receive data				
LADDR:=W#16#D			from the DP				
RET_VAL:=MW 20			master				
RECORD:=P#M30.0 Byte20							
L	MB	30	Continue to				
L	MB	7	process received				
+	I		data				
T	MW	100					

Data Transfer in STOP Mode

The DP slave CPU goes into STOP mode: The data in the intermediate memory of the CPU are overwritten with “0”. In other words, the DP master reads “0”.

The DP master goes into STOP mode: The current data in the intermediate memory of the CPU are retained and can continue to be read by the CPU.

PROFIBUS Address

You cannot set 126 as PROFIBUS address for the CPU 41x as DP slave.

3.1.5 Diagnostics of the CPU 41x as DP Slave

Diagnostics using LEDs – CPU 41x

Table 3-7 explains the meaning of the BUSF LEDs.
The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 3-7 Meaning of the BUSF LEDs of the CPU 41x as DP Slave

BUSF	Meaning	What to Do
Off	Configuration correct	–
Flashing	The CPU 41x is incorrectly configured. There is no data interchange between the DP master and the CPU 41x. Causes: • The response monitoring time has expired. • Bus communication via PROFIBUS DP has been interrupted. • The PROFIBUS address is incorrect.	• Check the CPU 41x. • Check to make sure that the bus connector is properly inserted. • Check whether the bus cable to the DP master has been interrupted. • Check the configuration and parameter assignment.
On	• Bus short circuit	• Check the bus setup.

Triggering Detection of the Bus Topology in a DP Master System with the SFC 103 “DP_TOPOL”

The diagnostics repeater is provided to improve the ability to locate disrupted modules or an interruption on the DP cables when failures occur in ongoing operation. This module operates as a slave and can determine the topology of a DP strand and record any faults originating from it.

You can use SFC 103 “DP_TOPOL” to trigger the analysis of the bus topology of a DP master systems by the diagnostics repeater. SFC 103 is documented in the corresponding online help and in the manual “System and Standard Functions”. The diagnostics repeater is documented in the manual “Diagnostics Repeater for PROFIBUS DP”, order number 6ES7972-0AB00-8BA0.

Diagnostics with *STEP 5* or *STEP 7* Slave Diagnostics

The slave diagnosis complies with the EN 50170, Volume 2, PROFIBUS standard. Depending on the DP master, it can be read out with *STEP 5* or *STEP 7* for all DP slaves that comply with the standard.

The display and structure of the slave diagnosis is described in the following sections.

S7 Diagnosis

An S7 diagnosis can be requested for all diagnostics-capable modules in the SIMATIC S7/M7 range of modules in the user program. You can find out which modules have diagnostic capability in the module information or in the catalog. The structure of the S7 diagnostic data is the same for both central and distributed modules.

The diagnostic data of a module is in data records 0 and 1 of the system data area of the module. Data record 0 contains 4 bytes of diagnostic data describing the current status of a module. Data record 1 also contains module-specific diagnostic data.

You will find the structure of the diagnostic data described in the *Standard and System Functions* Reference Manual.

Reading Out the Diagnosis

Table 3-8 Reading Out the Diagnostic Data with *STEP 5* and *STEP 7* in the Master System

Automation System with DP Master	Block or Tab in *STEP 7*	Application	Refer To...
SIMATIC S7/M7	DP slave diagnostics tab	To display the slave diagnosis as plain text at the *STEP 7* user interface	See the section on hardware diagnostics in the *STEP 7* online help system and in the *STEP 7* user guide
	SFC 13 “DP NRM_DG”	To read out the slave diagnosis (store in the data area of the user program)	SFC see Reference Manual *System and Standard Functions*
	SFC 51 “RDSYSST”	To read out SSL sublists Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	See the *System and Standard Functions* Reference Manual
	SFB 54 “RDREC”	Applies to the DPV1 environment: To read out interrupt information within the associated interrupt OB	
	FB 125/FC 125	To evaluate slave diagnosis	The Internet page http://www.ad.siemens.de/simatic-cs ID 387 257
SIMATIC S5 with IM 308-C as DP master	FB 192 “IM308C”	To read out the slave diagnosis (store in the data area of the user program)	FBs see the *ET 200 Distributed I/O System manual*
SIMATIC S5 with S5-95U programmable controller as DP master	SFB 230 “S_DIAG”		

Example of Reading Out the Slave Diagnosis with FB 192 “IM 308C”

Here you will find an example of how to use FB 192 to read out the slave diagnosis for a DP slave in the *STEP 5* user program.

Assumptions

The following assumptions apply to this *STEP 5* user program:

- The IM 308-C is assigned pages 0 to 15 (number 0 of the IM 308-C) as the DP master.
- The DP slave has the PROFIBUS address 3.
- The slave diagnosis is to be stored in DB 20. However, you can also use any other data block for this.
- The slave diagnosis consists of 26 bytes.

STEP 5 User Program

```
STL                                 Explanation
       :A     DB 30
       :JU    FB 192
Name   :IM308C
DPAD   :      KH F800              Default address area of the IM 308-C
IMST   :      KY 0, 3              IM no. = 0, PROFIBUS address of DP slave = 3
FCT    :      KC SD                Function: Read slave diagnosis
GCGR   :      KM 0                 Not evaluated
TYP    :      KY 0, 20             S5 data area: DB 20
STAD   :      KF +1                Diagnostic data from data word 1
LENG   :      KF 26                Length of diagnosis = 26 bytes
ERR    :      DW 0                 Error code stored in DW 0 of DB 30
```

Diagnostic Addresses in Connection with DP Master Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Ensure during configuration that DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

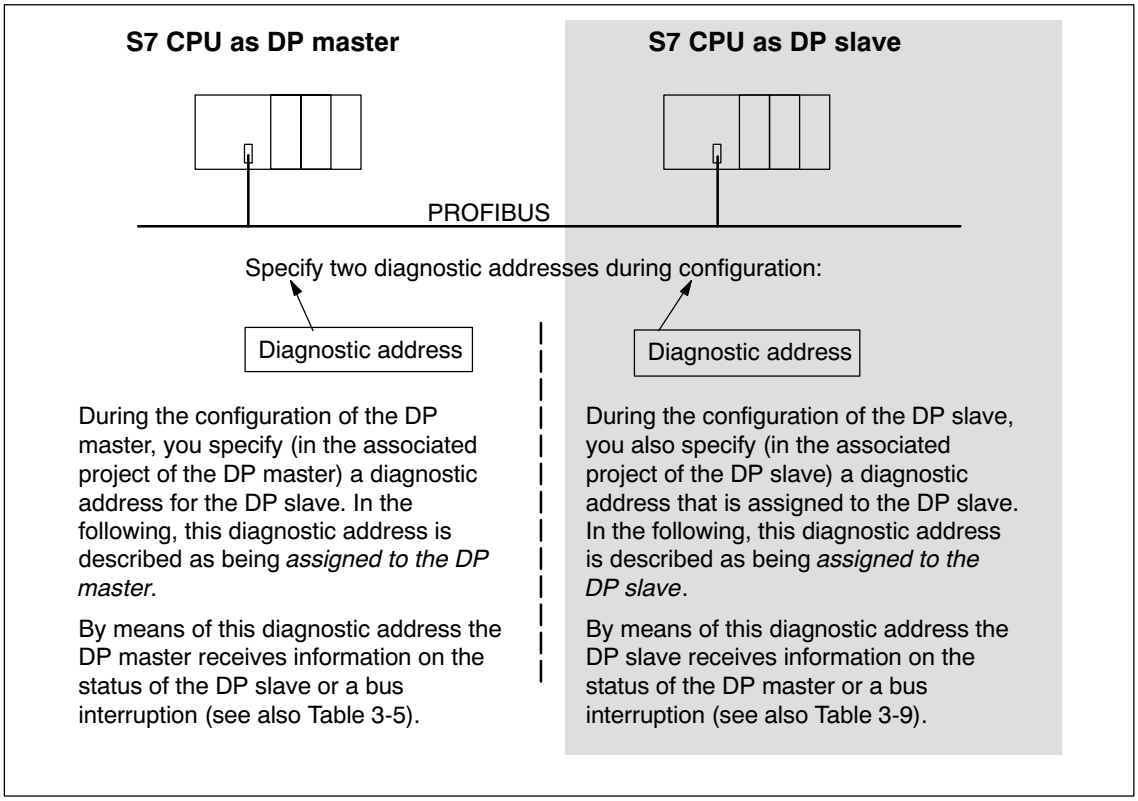


Figure 3-4 Diagnostic Addresses for the DP Master and DP Slave

Event Detection

Table 3-9 shows you how the CPU 41x as DP slave detects any operating mode changes or interruptions in data transfer.

Table 3-9 Event Detection of the CPUs 41x as DP Slave

Event	What Happens in the DP Slave
Bus interruption (short circuit, connector removed)	• OB 86 is called with the message *Station failure* (incoming event; diagnostic address of the DP slave that is assigned to the DP slave) • In the case of I/O access: OB 122 called (I/O access error)
DP master: RUN → STOP	• OB 82 is called with the message *Faulty module* (incoming event; diagnostic address of the DP slave that is assigned to the DP slave; Variable OB82_MDL_STOP=1)
DP master: STOP → RUN	• OB 82 is called with the message *Module OK.* (outgoing event; diagnostic address of the DP slave that is assigned to the DP slave; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table 3-10 shows you, for example, how you can evaluate RUN-STOP transitions of the DP master in the DP slave (see also Table 3-9).

Table 3-10 Evaluation of RUN-STOP Transitions in the DP Master/DP Slave

In the DP Master	In the DP Slave
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic addresses: (example) Slave diagnostic address=**422** Master diagnostic address=not relevant
CPU: RUN → STOP →	The CPU calls OB 82 with the following information, amongst other things: • OB 82_MDL_ADDR:=**422** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=module malfunction Tip: This information is also in the diagnostic buffer of the CPU

Structure of the Slave Diagnosis

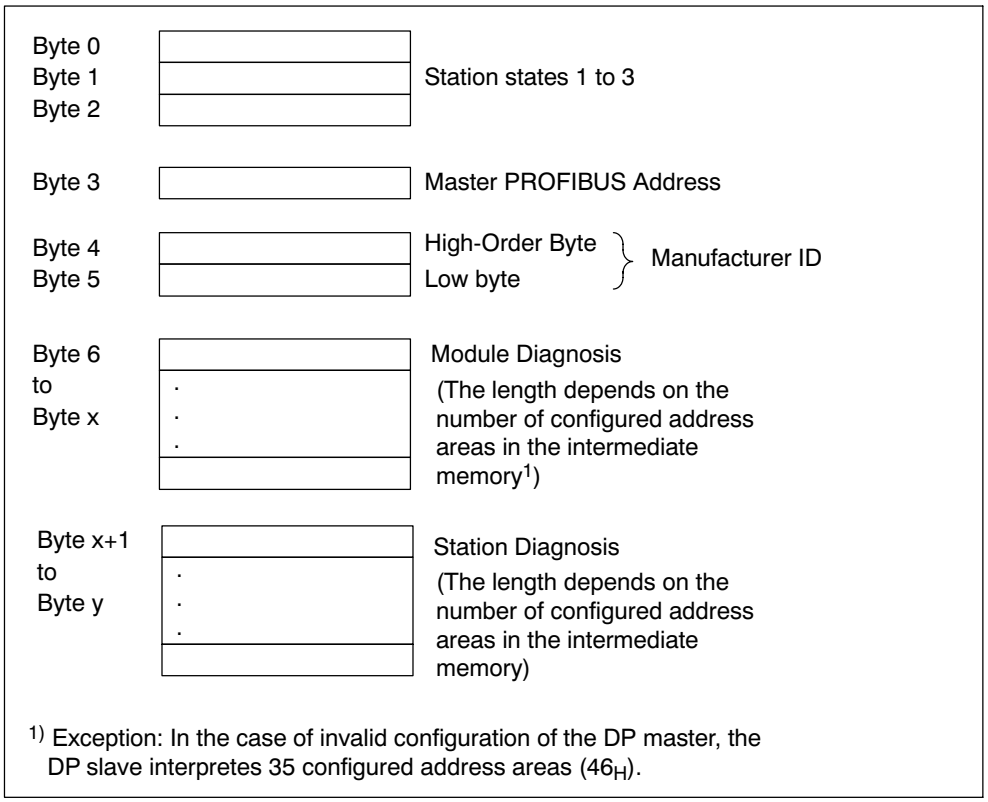


Figure 3-5 Structure of the Slave Diagnosis

3.1.6 CPU 41x as DP slave: Station States 1 to 3

Station states 1 to 3

Station status 1 to 3 provides an overview of the status of a DP slave.

Table 3-11 Structure of the Station Status 1 (Byte 0)

Bit	Meaning	What to Do
0	1: The DP slave **cannot** be addressed by the DP master.	• Correct DP address set on the DP slave? • Bus connector connected? • Voltage on DP slave? • RS 485 repeater set correctly? • Execute reset on the DP slave
1	1: The DP slave is not yet ready for data transfer.	• Wait while the DP slave powers up.
2	1: The configuration data sent by the DP master to the DP slave does not correspond to the actual configuration of the DP slave.	• Correct station type or correct configuration of the DP slave entered in the software?
3	1: Diagnostic interrupt, triggered by RUN-STOP transition of the CPU 0: Diagnostic interrupt, triggered by STOP-RUN transition of the CPU	• You can read out the diagnosis.
4	1:Function is not supported, e.g. changing the DP address via software	• Check the configuration.
5	0: The bit is always “0”.	–
6	1: The DP slave type does not correspond to the software configuration.	• Correct station type entered in the software? (Parameter assignment error)
7	1: Parameters have been assigned to the DP slave by a different DP master to the one that currently has access to the DP slave.	• Bit is always at 1, when you are accessing the DP slave using the programming device or another DP master, for example. The DP address of the parameter assignment master is in the “master PROFIBUS address” diagnostic byte.

Table 3-12 Structure of Station Status 2 (Byte 1)

Bit	Meaning
0	1: The DP slave must be assigned new parameters and reconfigured.
1	1: A diagnostic message has been issued. The DP slave cannot continue until the problem has been corrected (static diagnostic message).
2	1: The bit is always set to “1” if the DP slave with this DP address is present.
3	1: Response monitoring is enabled for this DP slave.
4	0: The bit is always at “0”.
5	0: The bit is always at “0”.
6	0: The bit is always at “0”.
7	1: The DP slave is disabled – that is, it has been removed from cyclic processing.

Table 3-13 Structure of Station Status 3 (Byte 2)

Bit	Meaning
0 to 6	0: The bits are always at “0”.
7	1: • There are more diagnostic messages than the DP slave can store. • The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.

Master PROFIBUS Address

The master PROFIBUS address diagnostic byte contains the DP address of the DP master that:

- assigns parameters for the DP slave and
- has read and write access to the DP slave

Table 3-14 Structure of the Master PROFIBUS Address (Byte 3)

Bit	Meaning
0 to 7	DP address of the DP master which configured the DP slave and which has read and write access to the DP slave.
	FF_H: DP slave has not been configured by any DP master.

Manufacturer ID

The manufacturer ID contains a code that describes the type of DP slave.

Table 3-15 Structure of the Manufacturer ID (Bytes 4, 5)

Byte 4	Byte 5	Manufacturer ID for CPU
80_H	$C5_H$	412-1
80_H	$C6_H$	412-2
80_H	$C7_H$	414-2
80_H	$C8_H$	414-3
80_H	CA_H	416-2
80_H	CB_H	416-3
80_H	CC_H	417-4

Module Diagnosis

The module diagnosis tells you for which of the configured address areas of the intermediate memory an entry has been made.

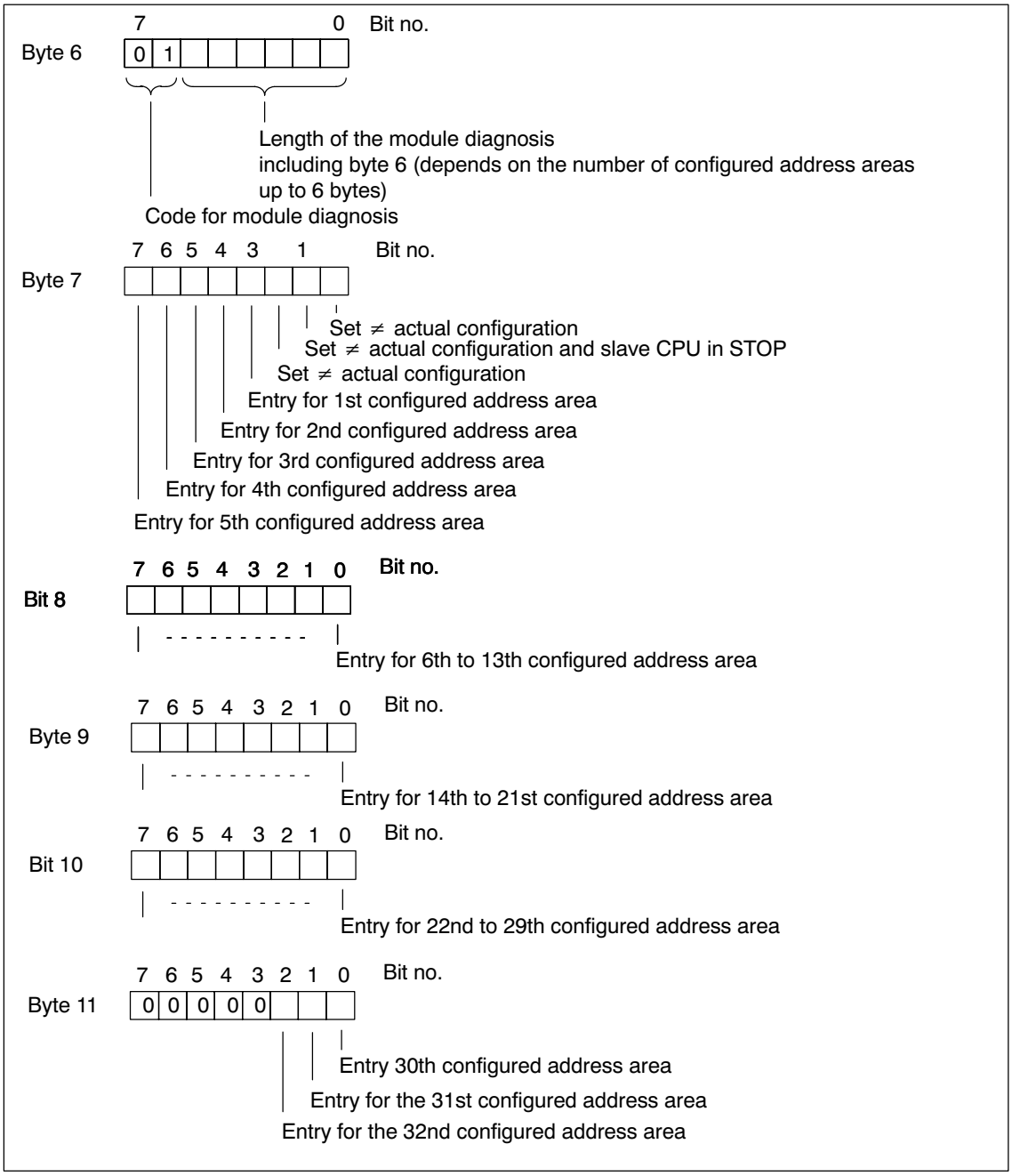


Figure 3-6 Structure of the Module Diagnosis of the CPU 41x

Station Diagnosis

The station diagnosis provides detailed information on a DP slave. The station diagnosis starts as of byte x and can include up to 20 bytes.

The figure below illustrates the structure and contents of the bytes for a configured address area of the intermediate memory.

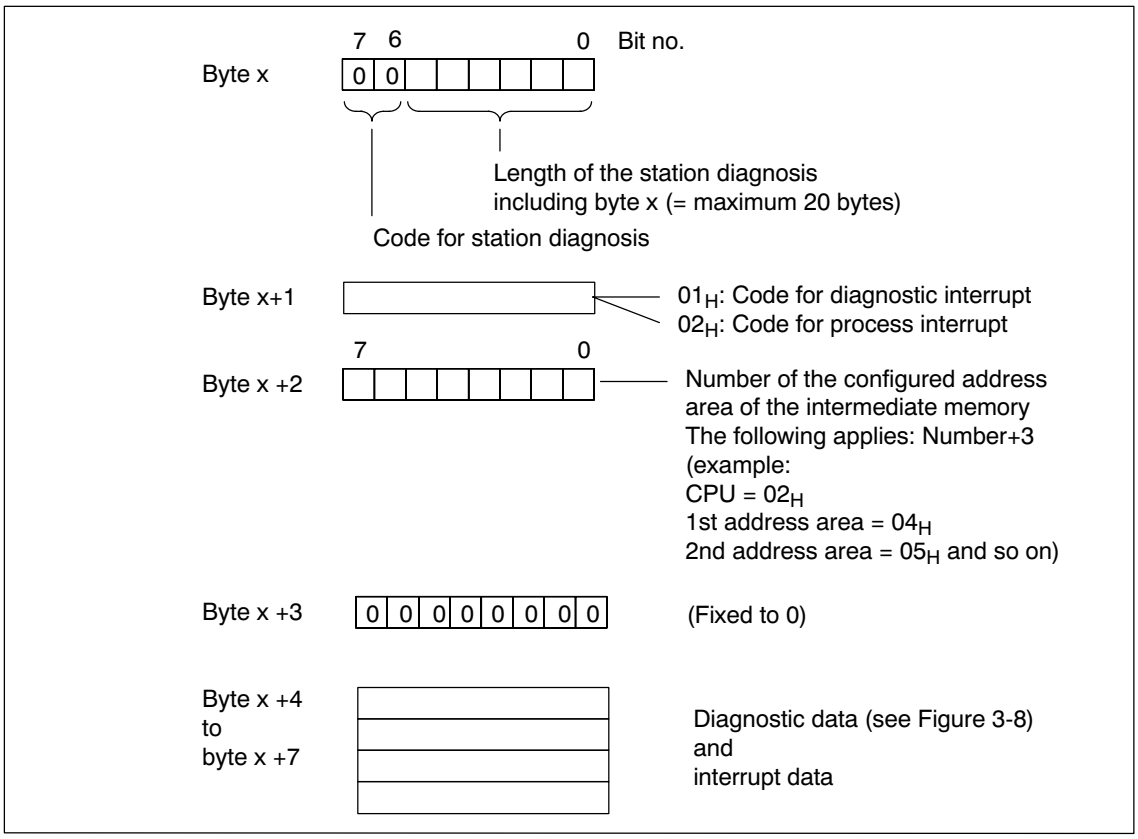


Figure 3-7 Structure of the Station Diagnosis

As of byte x +4

The meaning of the bytes as of byte x+4 depends on byte x +1 (see Figure 3-7).

In Byte x +1, the Code Stands for:	
Diagnostic Interrupt (01_H)	**Process Interrupt (02_H)**
The diagnostic data contain the 16 byte status information of the CPU. Figure 3-8 shows you the assignment of the first 4 bytes of the diagnostic data. The following 12 bytes are always 0.	You can program 4 bytes of interrupt information any way you wish for the process interrupt. You transfer these 4 bytes to the DP master in *STEP 7* using SFC 7 “DP_PRAL”.

Bytes x+4 to x+7 for Diagnostic Interrupts

Figure 3-8 illustrates the structure and contents of bytes x +4 to x +7 for the diagnostic interrupt. The contents of these bytes correspond to the contents of data record 0 of the diagnosis in *STEP 7* (in this case not all the bits are assigned).

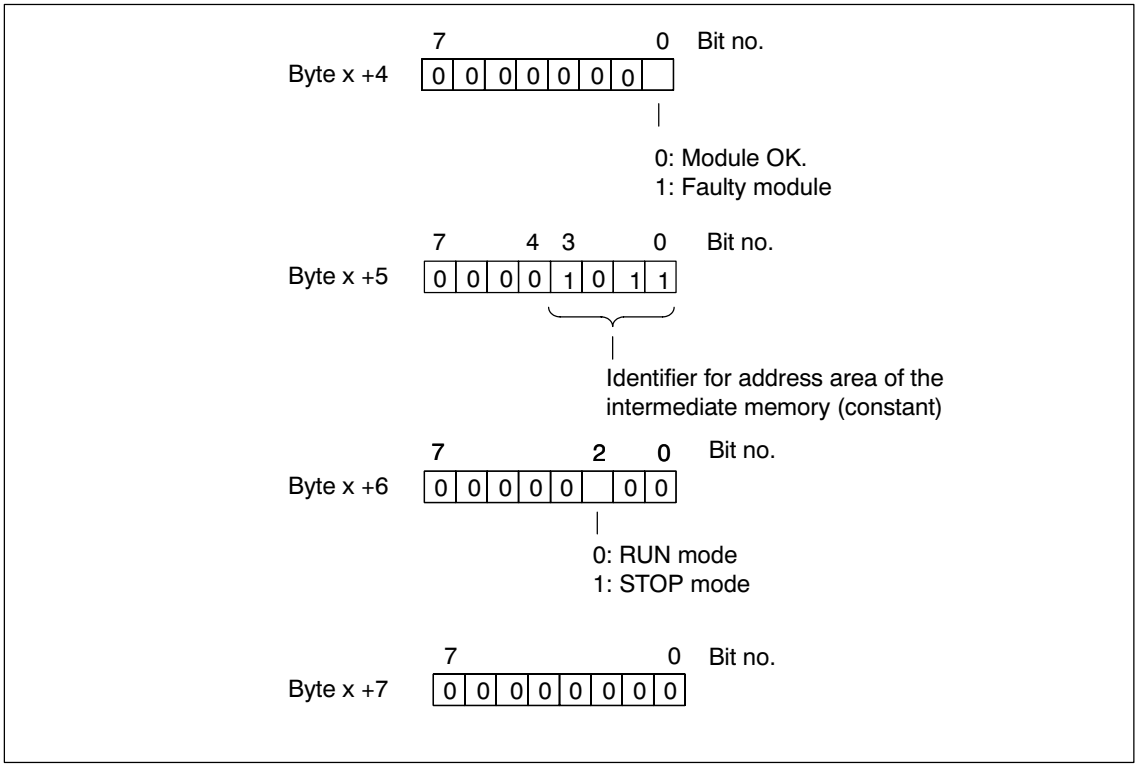


Figure 3-8 Bytes +4 to +7 for Diagnostic and Process Interrupts

Interrupts with the S7/M7 DP Master

In the CPU 41x as a DP slave you can trigger a process interrupt in the DP master from the user program. You can trigger an OB 40 in the user program of the DP master by calling SFC 7 “DP_PRAL”. Using SFC 7 you can forward interrupt information in a double word to the DP master, which you can evaluate in OB 40 in the OB40_POINT_ADDR variable. You can program the interrupt information as you choose. You will find a detailed description of SFC 7 “DP_PRAL” in the *System Software for S7-300/400, System and Standard Functions* Reference Manual.

Interrupts with another DP Master

If you are running the CPU 41x with another DP master, these interrupts are reflected in the station diagnosis of the CPU 41x. You have to process the relevant diagnostic events in the DP master’s user program.

Note

Note the following in order to be able to evaluate diagnostic interrupts and process interrupts by means of the station diagnosis when using a different DP master:

- The DP master should be able to store the diagnostic messages; in other words, the diagnostic messages should be stored in a ring buffer in the DP master. There are more diagnostic messages than the DP master can store, only the last diagnostic message received would be available for evaluation, for example.
- You must query the relevant bits in the station diagnosis at regular intervals in your user program. You must also take the PROFIBUS DP bus cycle time into consideration so that you can query the bits at least once synchronously with the bus cycle time, for example.
- You cannot use process interrupts in the station diagnosis with an IM 308-C as the DP master, because only incoming – and not outgoing – interrupts are reported.

3.2 Direct Communication

You can configure direct communication for PROFIBUS nodes as of *STEP 7* V 5.0. The CPU 41x can participate in direct communication as the sender or recipient.

"Direct Communication" represents a special type of communication relationship between PROFIBUS DP nodes.

3.2.1 Principle of Direct Data

Direct communication is characterized by the fact that PROFIBUS DP nodes "listen in" to find out which data a DP slave is sending back to its DP master. By means of this mechanism the "eavesdropper" (recipient) can access changes to the input data of remote DP slaves directly.

During configuration in *STEP 7*, you specify by means of the relevant I/O input addresses the address area of the recipient to which the required data of the sender are to be read.

A CPU 41x can be:

Sender	as a DP slave
Recipient	as a DP slave or a DP master or as a CPU that is not integrated in a master system (see Figure 3-9).

Example

Figure 3-9 uses an example to illustrate which direct communication "relationships" you can configure. All the DP masters and DP slaves in the figure are CPUs 41x. Note that other DP slaves (ET 200M, ET 200X, ET 200S) can only be senders.

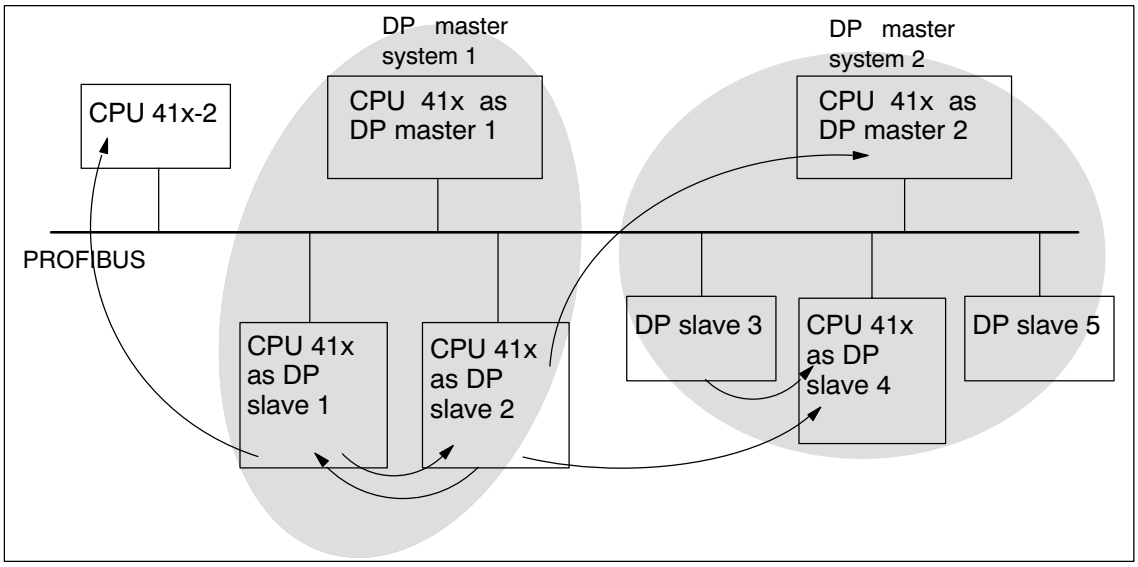


Figure 3-9 Direct Communication with CPUs 41x

3.2.2 Diagnostics in Direct Communication

Diagnostic Addresses

In direct communication you assign a diagnostic address in the recipient:

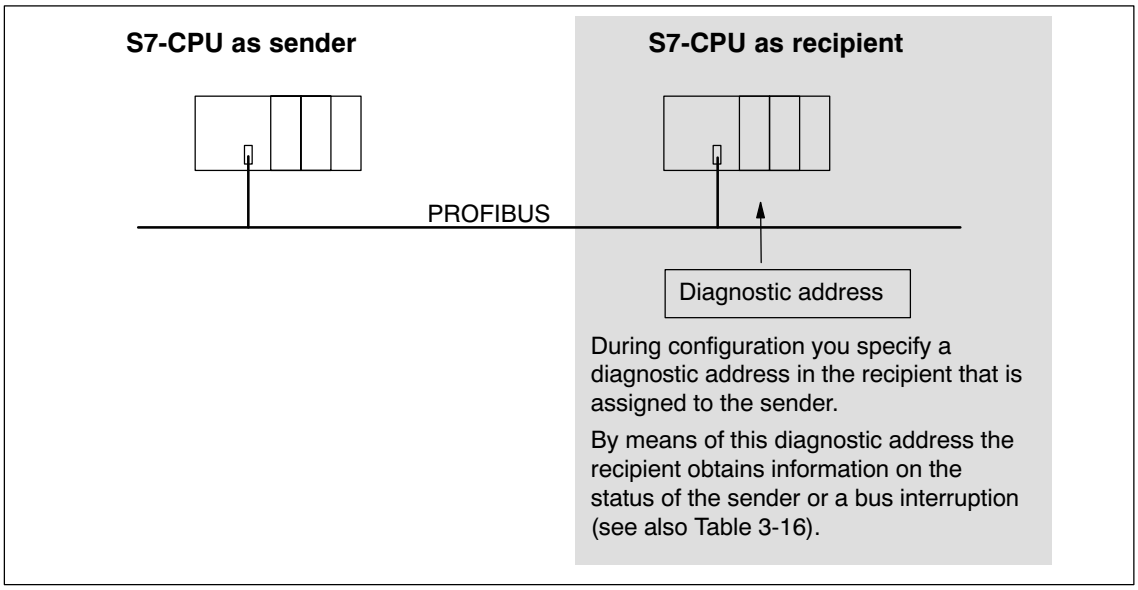


Figure 3-10 Diagnostic Address for the Recipient During Direct Communication

Event Detection

Table 3-16 shows you how the CPU 41x as recipient detects interruptions in data transfer.

Table 3-16 Event Detection of the CPUs 41x as Recipient During Direct Communication

Event	What Happens in the Recipient
Bus interruption (short circuit, connector removed)	• OB 86 is called with the message *Station failure* (incoming event; diagnostic address of the recipient assigned to the sender) • In the case of I/O access: OB 122 called (I/O access error)

Evaluation in the User Program

The following table 3-17 shows you, for example, how you can evaluate a sender station failure in the recipient (see also Table 3-16).

Table 3-17 Evaluation of the Station Failure in the Sender During Direct Communication

In the Sender	In the Recipient
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic address: (example) Diagnostic address=**444**
Station failure →	The CPU calls OB 86 with the following information, amongst other things: • OB 86_MDL_ADDR:=**444** • OB86_EV_CLASS:=B#16#38 (incoming event) • OB86_FLT_ID:=B#16#C4 (failure of a DP station) Tip: This information is also in the diagnostic buffer of the CPU

3.3 Consistent Data

Data that belongs together in terms of its content and a process state written at a specific point in time is known as consistent data. To maintain consistency, the data should not be changed or updated during processing or transmission.

Example

To ensure that the CPU has a consistent image of the process signals for the duration of cyclic program scanning, the process signals are read from the process image inputs prior to program scanning and written to the process image outputs after the program scanning. Subsequently, during program scanning when the address area “inputs” (I) and “outputs” (O) are addressed, the user program addresses the internal memory area of the CPU on which the image of the inputs and outputs is located instead of directly accessing the signal modules.

SFC 81 “UBLKMOV”

With SFC 81 “UBLKMOV” (uninterruptible block move), you can copy the contents of a memory area (= source area) consistently to a different memory area (= destination area). The copy operation cannot be interrupted by other operating system activities.

SFC 81 “UBLKMOV” enables you to copy the following memory areas:

- Memory markers
- DB contents
- Process image of the inputs
- Process image of outputs

The maximum amount of data you can copy is 512 bytes. Take into consideration the restrictions for the specific CPU, which are documented in the operations list, for example.

Since copying cannot be interrupted, the interrupt reaction times of your CPU may increase when using SFC 81 “UBLKMOV”.

The source and destination areas must not overlap. If the specified destination area is larger than the source area, the function only copies as much data to the destination area as that contained in the source area. If the specified destination area is smaller than the source area, the function only copies as much data as can be written to the destination area.

For information on SFC 81, refer to the corresponding Online Help and to the “*System and Standard Functions*” manual.

3.3.1 Consistency for Communication Blocks and Functions

Using S7-400 the communication data is not processed in the scan cycle checkpoint; instead, this data is processed in fixed time slices during the program cycle.

In the system the byte, word and double word data formats can always be processed consistently, in other words, the transfer or processing of 1 byte, 1 word (= 2 bytes) or 1 double word (= 4 bytes) cannot be interrupted.

If communication blocks (such as SFB 12 “BSEND”) are called in the user program, which are only used in pairs (such as SFB 12 “BSEND” und SFB 13 “BRCV”) and which share access to data, the access to this data area can be coordinated between themselves, using the “DONE” parameter, for example. Data consistency of the communication areas transmitted locally with a communication block can thus be ensured in the user program.

S7 communication functions such as SFB 14 “GET”, SFB 15 “PUT” react differently because no block is needed in the user program of the destination device. In this case the size of data consistency has to be taken into account beforehand during the programming phase.

3.3.2 Access to the Working Memory of the CPU

The communication functions of the operating system access the working memory of the CPU in fixed block lengths. The block size is a variable length up to a maximum of 462 bytes.

3.3.3 Reading from and Writing to a DP Standard Slave Consistently

Writing Data Consistently to a DP Standard Slave Using SFC 14 “DPRD_DAT”

Using SFC 14 “DPRD_DAT” (read consistent data of a DP standard slave) you can consistently read the data of a DP standard slave.

The data read is entered into the destination range defined by RECORD if no error occurs during the data transmission.

The destination range must have the same length as the one you have configured for the selected module with STEP 7.

By invoking SFC 14 you can only access the data of one module / DP ID at the configured start address.

For information on SFC 14, refer to the corresponding Online Help and to the “*System and Standard Functions*” manual

3.3.4 Writing Data Consistently to a DP Standard Slave Using SFC 15 “DPWR_DAT”

Using SFC 15 “DPWR_DAT” (write consistent data to a DP standard slave) you can consistently write data to the DP standard slave addressed in the RECORD.

The source range must have the same length as the one you have configured for the selected module with STEP 7.

Note

The Profibus DP standard defines the upper limit for the transmission of consistent user data (see following section). Typical DP standard slaves adhere to this upper limit. In older CPUs (<1999) there are restrictions in the transmission of consistent user data depending on the CPU. For these CPUs you can determine the maximum length of the data which the CPU can consistently read and write to and from the DP standard in the respective technical specifications under the index entry “DP Master – User data per DP slave”. Newer CPUs are capable of exceeding the value for the amount of data that a DP standard slave can send and receive.

Upper Limit for the Transmission of Consistent User Data to a DP Slave

The Profibus DP standard defines the upper limit for the transmission of consistent user data to a DP slave. For this reason a maximum of 64 words = 128 bytes of user data can be consistently transferred in a block to the DP slave.

During the configuration you can determine the size of the consistent area. You can set a maximum length of consistent data at 64 words = 128 bytes in the special identification format (SKF) (128 bytes for inputs and 128 bytes for outputs); the data block size cannot exceed this.

This upper limit only applies to pure user data. Diagnostics and parameter data are regrouped into full records and therefore always transferred consistently.

In the general identification format (AKF) the maximum length of consistent data can be set at 16 words = 32 bytes (32 bytes for inputs and 32 bytes for outputs); the data block size cannot exceed this.

Note in this context that a CPU 41x in a general environment acting as a DP slave on a third-party master (connection defined by GSD) has to be configured with the general identification format. The transfer memory of a CPU 41x acting as a DP slave to the PROFIBUS DP can therefore be a maximum of 16 words = 32 bytes.

For information on SFC 15, refer to the corresponding Online Help and to the “*System and Standard Functions*” manual

3.3.5 Consistent Data Access without the Use of SFC 14 or SFC 15

Consistent data access of > 4 bytes without using SFC 14 or SFC 15 is possible for the CPUs describedin this manual. The data area of a DP slave that should transfer consistently is transferred to a process image partition. The information in this area is therefore always consistent. You can subsequently use load/transfer commands (such as L EW 1) to access the process image. This is an especially convenient and efficient (low runtime load) way to access consistent data. This allows efficient integration and configuration of drives or other DP slaves, for example.

An I/O access error does **not** occur with direct access (e.g. L PEW or T PAW).

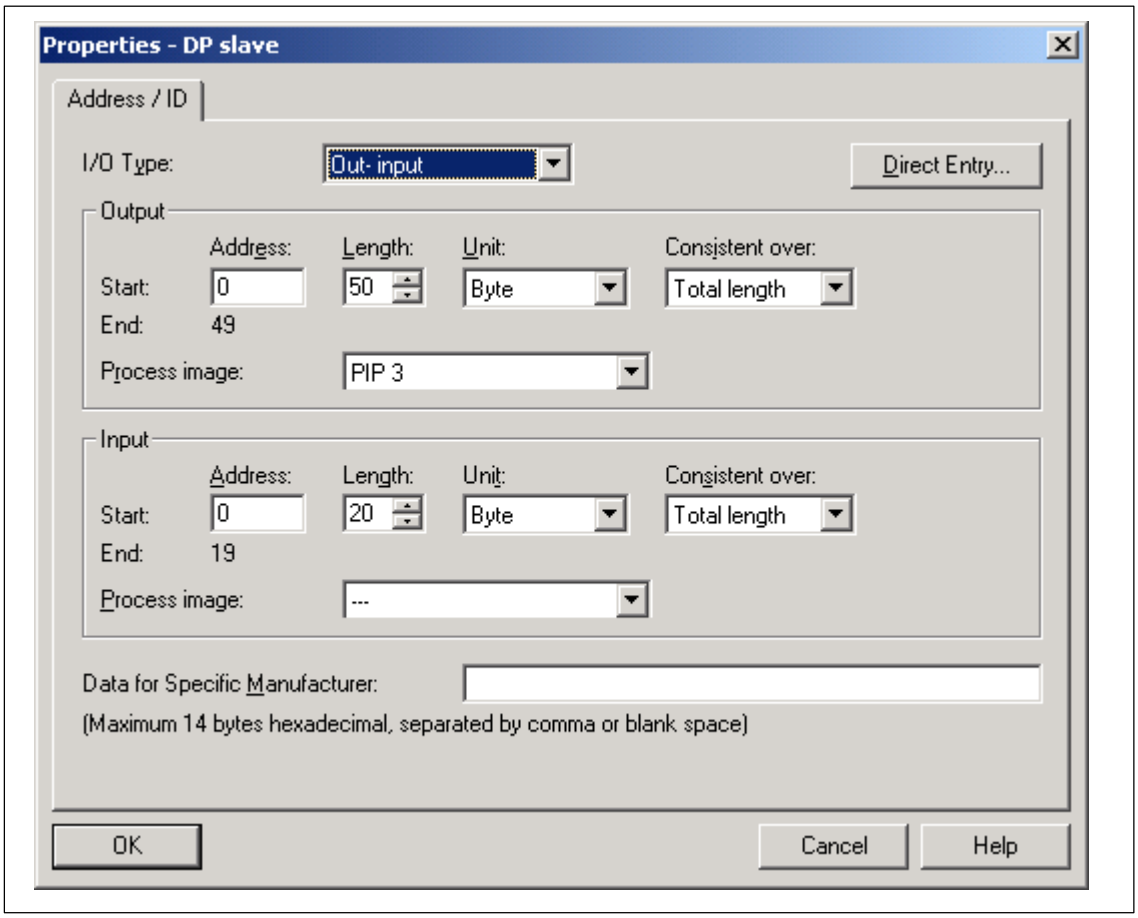
The following is important for converting from the SFC14/15 method to the process image method:

- When converting from the SFC14/15 method to the process image method, it is not recommended to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, the consistency between the process image values and the values of the system function SFC14 is not ensured.
- SFC 50 “RD_LGADR” outputs another address area with the SFC 14/15 method as with the process image method.
- If you are using a CP 443-5 ext the simultaneous use of SFC 14/15 and the process image results in the following errors, you cannot read/write into the process image and/or you can no longer read/write with SFC 14/15.

Example:

The following example (of the process image partition 3 “TPA 3”) shows such a configuration in HW Config:

- TPA 3 at output: These 50 bytes are stored consistent in the process image partition 3 (pull-down list “Consistent over –> entire length”) and can therefore be read through the normal “load input xy” commands.
- Selecting “Process Image Partition –> ––” under input in the pull-down menu means: do not store in a process image. Then the handling can only be performed using the system functions SFC14/15.



Memory Concept and Startup Scenarios

4

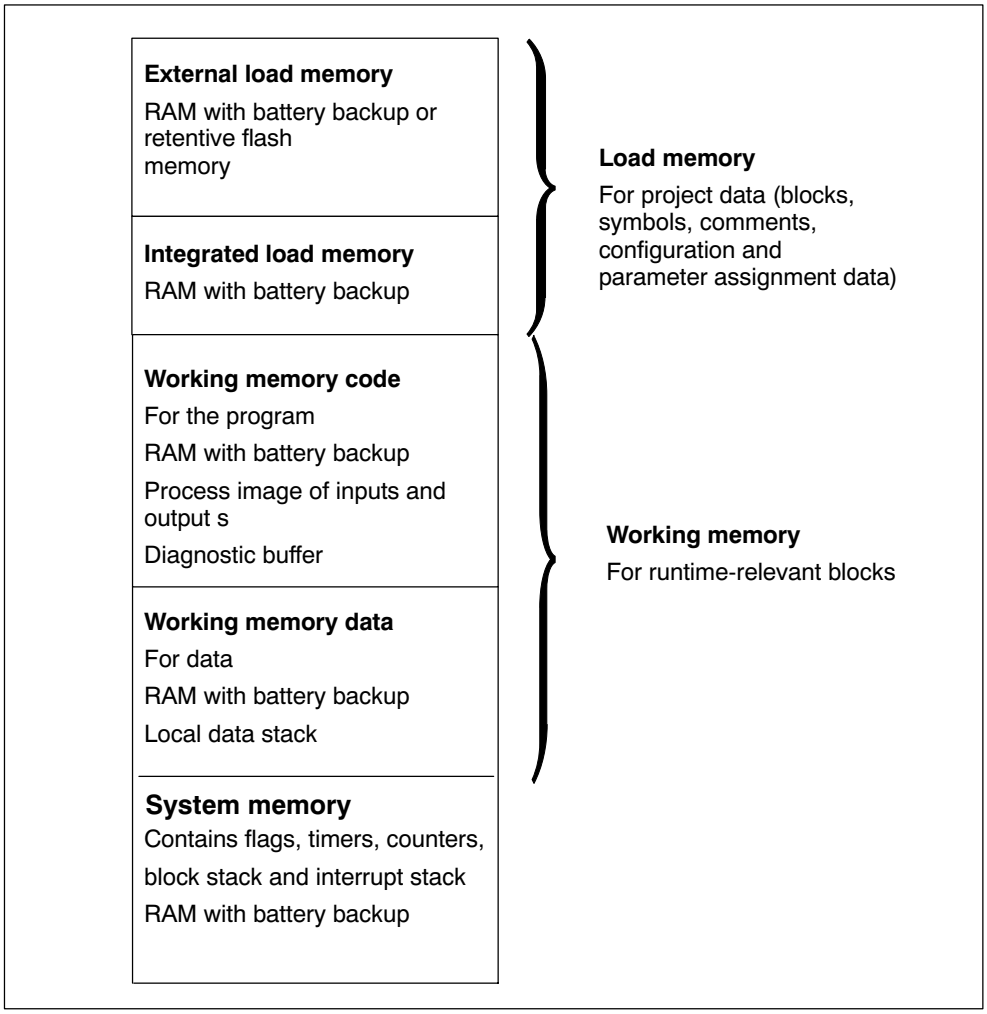
Chapter Overview

In Section	You will find	On Page
4.1	Overview of the Memory Concept of S7-400 CPUs	4-2
4.2	Overview of the Startup Scenarios for S7-400-CPUs	4-5

4.1 Overview of the Memory Concept of S7-400 CPUs

Organization of Memory Areas

You can divide the memory of the S7 CPUs into the following areas:



Important Note for CPUs with Configurable Division of the Working Memory

If you use parameter assignment to change the division of the working memory, the working memory is reorganized when the system data are downloaded to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

The usable size of the working memory for code or data blocks is changed if you change the following parameters for loading the system data:

- Size of the process image (byte by byte; “Cycle/Clock Memory” tab)
- Communication resources (S7-400 only; “Memory” tab)
- Size of the diagnostic buffer (“Diagnostics/Clock” tab)
- Number of local data for all priority classes (“Memory” tab)

Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory in the CPU, you must take into consideration the following memory requirements when assigning parameters:

Table 4-1 Memory Requirements

Parameter	Required Working Memory	In Code/Data Memory
Size of the process image (inputs)	12 bytes per byte in the process input image	Code memory
Size of the process image (outputs)	12 bytes per byte in the process output image	Code memory
Communication resources (communication jobs)	72 bytes per communication job	Code memory
Size of diagnostic buffer	32 bytes per entry in the diagnostic buffer	Code memory
Volume of local data	1 byte per byte of local data	Data memory

Memory Types in S7-400 CPUs

- Load memory for project data, such as blocks, configuration and parameter assignment data, including symbols and comments as of version 5.1.
- Working memory for the runtime-relevant blocks (code blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as memory markers, timers, and counters. The system memory also receives the block stack and the interrupt stack.
- System memory of the CPU also makes temporary memory available (local data stack, diagnostic buffer and communication resources) that is assigned to the program when a block is called for its temporary data. These data are only valid as long as the block is active.

  By changing the default values for the process image, local data, diagnostic buffer and communication resources (see the object properties of the CPU in HWConfig), you can control the working memory available to the runtime-relevant blocks.

Notice

Please note the following if you enlarge the process image of a CPU. Make sure that you configure the modules that can only be operated above the process image in such a way that they are also positioned above the enlarged process image. This particularly applies to IP and WF modules that you operate in the S5 adapter casing in a S7-400.

Flexible Memory Capacity

- Working memory:

  The capacity of the working memory is determined by selecting the appropriate CPU from the graded range of CPUs.
- Load memory:

  The integrated load memory is sufficient for small and medium-sized programs.

  The load memory can be increased for larger programs by inserting the RAM memory card.

  Flash memory cards are also available to ensure that programs are retained in the event of a power failure even if there isn't a backup battery. Flash memory cards can also be used (as of 4 MB) to send and execute operating system updates.

Backup

- The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.

4.2 Overview of the Startup Scenarios for S7-400 CPUs

Cold Restart

- At the restart, all data (process image, memory markers, timers, counters and data blocks) are reset to the start values stored in the program (load memory), irrespective of whether they were configured as retentive or non-retentive.

  Retentive flags, timers and counters retain their last valid value.

  All All DBs assigned the “Non Retain” attribute are reset to the load values. The remaining blocks retain their last valid value.
- Program processing is started from the beginning again (startup OB or OB 1).

Warm Restart

- At a warm restart, the process image and the non-retentive memory markers, timers and counters are reset.

  Retentive flags, timers and counters retain their last valid value.
- Program execution is started from the beginning again (startup OB or OB 1).
- When the power supply is interrupted, a warm restart is only possible in backup mode.

Hot Restart

- At a hot restart, all the data, including the process image, retain their last valid value.
- Program processing is resumed at the breakpoint.
- The outputs are not changed until the end of the current cycle.
- When the power supply is interrupted, a restart is only possible in backed-up mode.

Cycle and Reaction Times of the S7-400

5

This chapter explains the composition of the cycle and reaction times of the S7-400.

You can display the cycle time of your user program on the relevant CPU using the programming device (see manual *Configuring Hardware and Communication Connections with STEP 7 Version 5.0* or higher).

Examples will illustrate how you calculate the cycle time.

The reaction time is important for monitoring a process. This chapter provides a detailed description of how to calculate this. If you use a CPU 41x-2 DP as a master in the PROFIBUS DP network, you also have to take into account DP cycle times (see Section 5.5).

Chapter Overview

Further Information

You will find further information on the following processing times in the S7-400 Instruction List. It lists all the *STEP 7* instructions that can be processed by the relevant CPUs, together with their execution times and all the SFCs/SFBs integrated in the CPUs and the IEC functions that can be called in *STEP 7*, together with their processing times.

5.1 Cycle Time

In this chapter you will learn about the composition of the cycle time and how you can calculate the cycle time.

Definition of the Cycle Time

The cycle time is the time which the operating system needs to process a program run – in other words, an OB 1 run – and all the program segments and system activities that interrupt that run.

This time is monitored.

Time-Sharing Model

Cyclic program scanning, and thus also processing of the user program, is performed in time slices. So that you can better appreciate these processes, we will assume in the following that each time slice is exactly 1 ms long.

Process Image

The process signals are read or written prior to program scanning so that a consistent image of the process signals is available to the CPU for the duration of cyclic program scanning. Then the CPU does not directly access the signal modules during program scanning when the address area “inputs” (I) and “outputs” (O) are addressed, but addresses instead the internal memory area of the CPU on which the image of the inputs and outputs is located.

The Cyclic Program Scanning Process

The following table and figure illustrate the phases of cyclic program scanning.

Table 5-1 Cyclic Program Scanning

Step	Process
1	The operating system starts the scan cycle monitoring time.
2	The CPU writes the values from the process-image output table in the output modules.
3	The CPU reads out the status of the inputs at the input modules and updates the process-image input table.
4	The CPU processes the user program in time slices and performs the operations specified in the program.
5	At the end of a cycle, the operating system executes pending tasks, such asthe loading and clearing of blocks.
6	The CPU then goes back to the beginning of the cycle after the configured minimum cycle time, as necessary, and starts cycle time monitoring again.

Parts of the Cycle Time

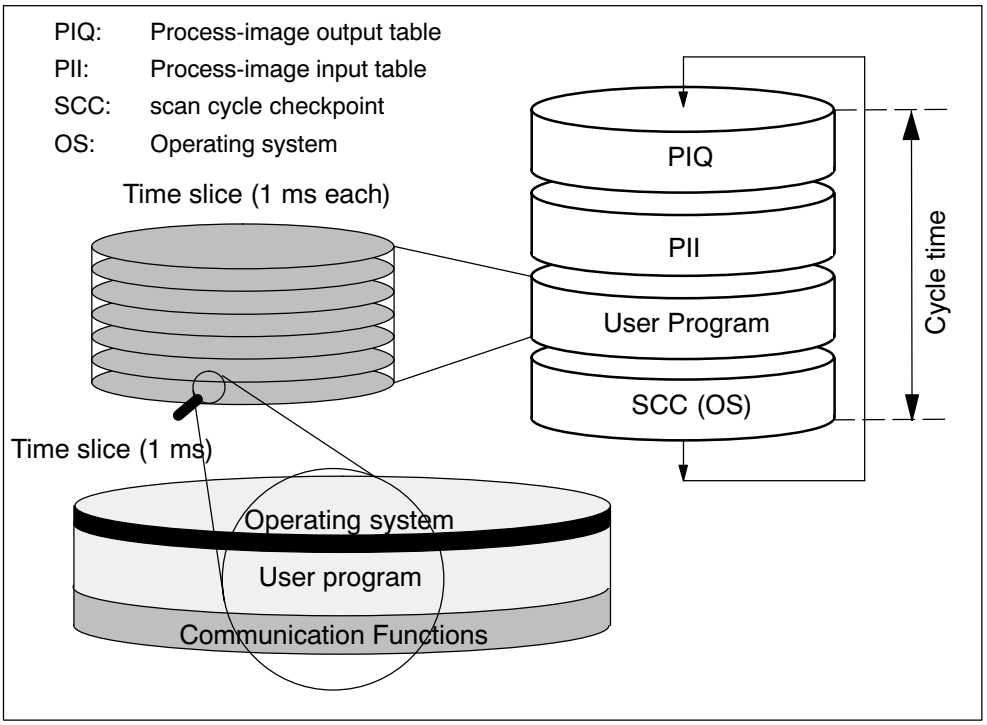


Figure 5-1 Parts and Composition of the Cycle Time

5.2 Cycle Time Calculation

Increasing the Cycle Time

Basically, you should note that the cycle time of a user program is increased by the following:

- Time-driven interrupt processing
- Hardware interrupt processing (see also Section 5.8)
- Diagnostics and error handling (see also Section 5.9)
- Communications via the MPI and CPs connected via the communication bus (for example, Ethernet, Profibus, DP); contained in the communication load
- Special functions such as control and monitoring of variables or block status
- Transfer and clearance of blocks, compression of the user program memory

Factors that Influence the Cycle Time

The following table indicates the factors that influence the cycle time.

Table 5-2 Factors that Influence the Cycle Time

Factors	Remark
Transfer time for the process-image output table (PIQ) and the process-image input table (PII)	... see Table 5-3
User program processing time	... is calculated from the execution times of the different instructions (see *S7-400 Instruction List*).
Operating system scan time at scan cycle checkpoint	... see Table 5-4
Increase in the cycle time from communications	You set the maximum permissible cycle load expected for communication in % in *STEP 7* (manual *Programming with STEP 7*). See Section 5.4.
Impact of interrupts on the cycle time	Interrupt can interrupt the user program at any time. ... see Table 5-5

Note
With CPUs produced prior to October 1998, updating of the process image of the outputs takes place before the scan cycle checkpoint.

Process Image Updating

The table below shows the CPU times for process image updating (process image transfer time). The times listed in the table are “ideal values” that may be increased by the occurrence of interrupts and by CPU communications.

The transfer time for process image updating is calculated as follows

C	+ portion in central rack (from line A of the following table)
	+ portion in expansion rack with local connection (from line B)
	+ portion in expansion rack with remote connection (from line C)
	+ portion via integrated DP interface (from line D)
	+ portion of consistent data via integrated DP interface (from line E1)
	+ portion of consistent data via external DP interface (from line E2)
	= transfer time for process image updating

The following tables list the individual portions of the transfer times for updating the process image (process image transfer time), once for standard CPUs and once for redundant CPUs. The times listed in the table are “ideal values” that may be increased by the occurrence of interrupts and by CPU communications.

Table 5-3 Portions of the process image transfer time

	Portions n = number of bytes in the process image c= number of consistency areas ****) in the process image	**CPU 412**	**CPU 414**	**CPU 416**	**CPU 417**
K	Base load	22 µs	18 µs	10 µs	7 µs
A	In the central rackI *)	n * 1,9 µs	n * 1,9 µs	n * 1,9 µs	n * 1,9 µs
B	In the expansion rack with local connectionI *)	n * 5 µs	n * 5 µs	n * 5 µs	n * 5 µs
C	In the expansion rack with remote connection *) **)				
	Read	n * 12 µs	n * 12 µs	n * 12 µs	n * 12 µs
	Write	n * 11 µs	n * 11 µs	n * 11 µs	n * 11 µs
D	In the DP area for the integrated DP interface	13 µs + n * 0,4 µs	4,0 µs + n * 0,25 µs	2,0 µs + n * 0,1 µs	1,5 µs + n * 0,1 µs
E	In the DP area for the external DP interface (CP 443-5 extended)	2,3 µs + n * 2,3 µs	1,3 µs + n * 2,0 µs	1,0 µs + n * 2,0 µs	1,0 µs + n * 2,0 µs
F 1	Consistent data in the process image for the integrated DP interface	k * 45 µs + n*0,25 µs	k * 4,0 µs + n*0,25 µs	k * 2,0 µs + n*0,15 µs	k * 1,5 µs + n*0,21 µs
F 2	Consistent data in the process image for the external DP interface (CP 443-5 extended)	k * 33 µs + n *2,0 µs	k * 2,1 µs + n *0,5 µs	k * 2,0 µs +n * 0,5 µs	k * 2,0 µs + n *1,9 µs

*) In the case of I/O modules that are plugged into the central rack or an expansion rack, the specified value contains the runtime of the I/O module

**) Measured with the IM 460-3 and IM 461-3 with a connection length of 100 m

***) The areas set in HW Config that are written to or read from the I/O at once and are therefore consistent.

Operating System Scan Time at the Scan Cycle Checkpoint

The table below lists the operating system scan times at the scan cycle checkpoint of the CPUs.

Table 5-4 Operating system scan time at scan cycle checkpoint

Process	CPU 412-1	CPU 412-2	CPU 414-2	CPU 414-3	CPU 416-2	CPU 416-3	CPU 417-4
Scan cycle control at the SCC	331 µs to 545 µs ∅ 339 µs	381 µs to 560 µs ∅ 391 µs	222 µs to 348 µs ∅ 228 µs	270 µs to 391 µs ∅ 276 µs	140 µs to 220 µs ∅ 144 µs	179 µs to 260 µs ∅ 184 µs	164 µs to 233 µs ∅ 168 µs

Increase in Cycle Time by Nesting Interrupts

Table 5-5 Increase in Cycle Time by Nesting Interrupts

CPU	Hardware Interrupt	Diagnostic Interrupt	Day Interrupt	Time-Delay Interrupt	Watchdog Interrupt	Programming/ Periphery Access Error
CPU 412-1/-2	696 µs	752 µs	584 µs	504 µs	504 µs	224 µs / 232 µs
CPU 414-2/-3	420 µs	450 µs	350 µs	300 µs	300 µs	135 µs / 140 µs
CPU 416-2/-3	280 µs	305 µs	230 µs	200 µs	200 µs	90 µs / 90 µs
CPU 417-4	260 µs	280 µs	210 µs	185 µs	185 µs	80 µs / 90 µs

You have to add the program execution time at the interrupt level to this increase.

If several interrupts are nested, their times must be added together.

5.3 Different Cycle Times

The length of the cycle time (T_{cyc}) is not identical in each cycle. The following figure shows different cycle times, T_{cyc1} and T_{cyc2}. T_{cyc2} is longer than T_{cyc1} , because the cyclically scanned OB 1 is interrupted by a time-of-day interrupt OB (in this instance, OB 10).

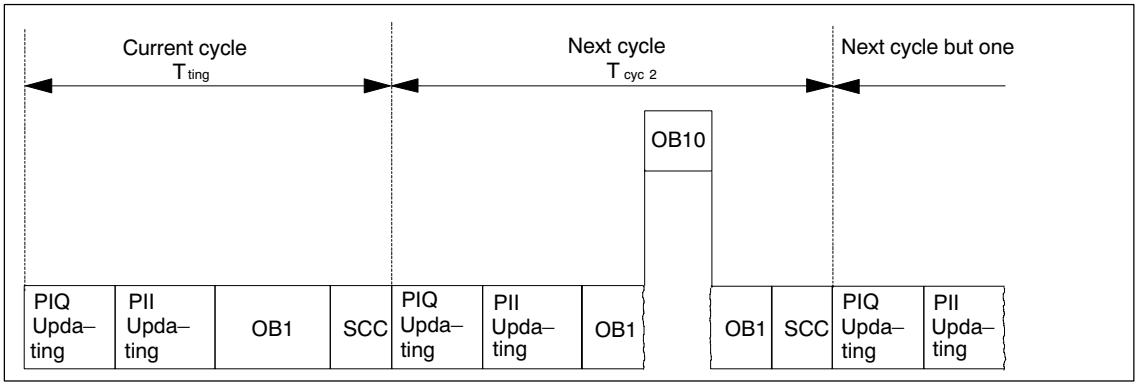


Figure 5-2 Different Cycle Times

A further reason for cycle times of different length is the fact that the execution time of blocks (for example, OB 1) can vary on account of:

- Conditional instructions
- Conditional block calls
- Different program paths
- Loops, etc.

Maximum Cycle Time

You can modify the default maximum cycle time in STEP 7 (cycle monitoring time). If this time has expired, OB 80 is called, and in it you can define how you want the CPU to respond to the time error. If you do not retrigger the cycle time with SFC 43, OB 80 doubles the cycle time at the first call. In this case, the CPU goes to STOP at the second call of OB 80.

If there is no OB 80 in the CPU memory, the CPU goes to STOP.

Minimum Cycle Time

You can set a minimum cycle time for a CPU in STEP 7. This is practical if

- you want the intervals of time between the start of program scanning of OB1 (free cycle) to be roughly of the same length, or
- updating of the process images would be performed unnecessarily often with too short a cycle time, or
- you want to process a program with the OB 90 in the background (not CPU 41x-4H).

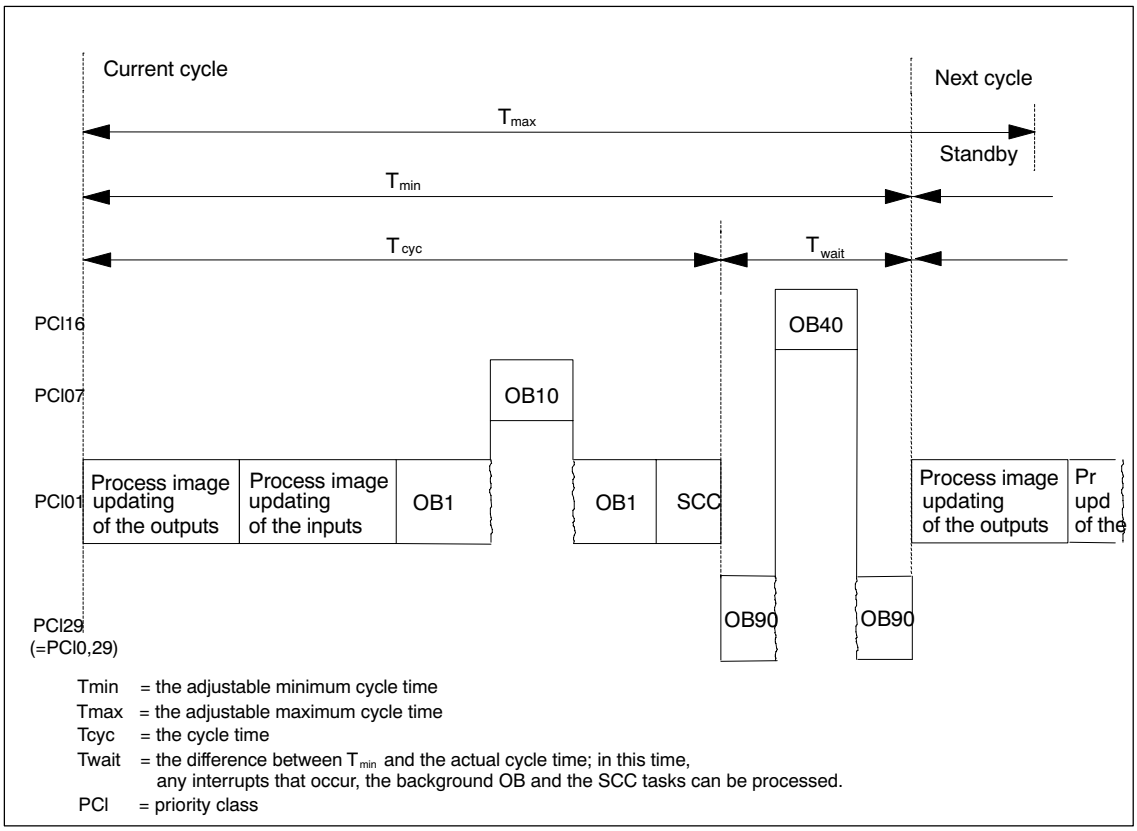


Figure 5-3 Minimum Cycle Time

The actual cycle time is the sum of T_{cyc} and T_{wait}. It is always greater than or equal to T_{min}.

5.4 Communication Load

The CPU operating system continually makes available to communications the percentage you configured for the overall CPU processing performance (time sharing). If this processing performance is not required for communications, it remains available for other processing tasks.

In the hardware configuration, you can set the load due to communications between 5% and 50%. By default, the value is set to 20%.

This percentage should be regarded as an average value, in other words, the communications component can be considerably greater than 20% in a time slice. On the other hand, the communications component in the next time slice is only a few or zero percent. This fact is also expressed by the following formula:

$$\text{Actual cycle time} = \text{cycle time} \cdot \frac{100}{100 - \text{“configured communication load in \%”}}$$

Round up the result to the next whole number !

Figure 5-4 Formula: Influence of Communication Load

Data consistency

The user program is interrupted for communications processing. The interrupt can be executed after any instruction. These communication jobs can modify the program data.
This means that the data consistency cannot be guaranteed for the duration of several accesses.
The manner in which you can guarantee consistency enduring for more than just one instruction is explained in the manual *System Software for S7-300/400 System and Standard Functions*, in the chapter on *Overview of S7 Communications and S7 Basic Communications*.

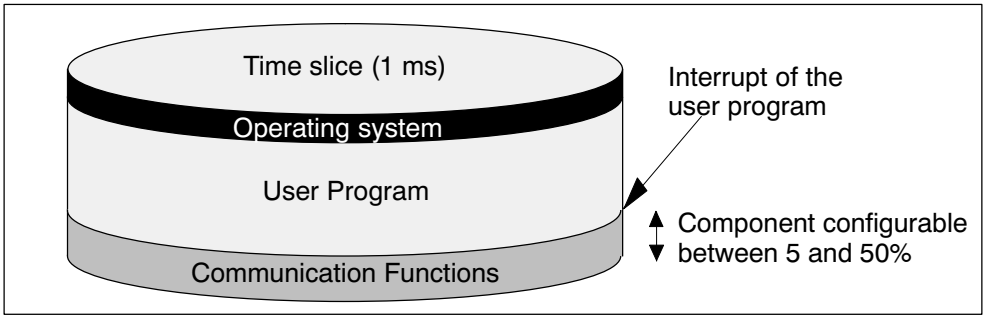


Figure 5-5 Breakdown of a Time Slice

Of the part remaining, the operating system of the S7-400 requires only a negligibly small amount for internal tasks.

Example: 20 % Communication Load

You have configured a communication load of 20% in the hardware configuration.

The calculated cycle time is 10 ms.

A 20% communication load means that, on average, 200 µs and 800 µs of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 800 µs = 13 time slices to process one cycle. This means that the actual cycle time is 13 times a 1 ms time slice = 13 ms, if the CPU fully utilizes the configured communication load.

This means that 20% communications do not increase the cycle linearly by 2 ms but by 3 ms.

Example: 50 % Communication Load

You have configured a communication load of 50% in the hardware configuration.

The calculated cycle time is 10 ms.

This means that 500 µs of each time slice remain for the cycle. The CPU therefore requires 10 ms / 500 µs = 20 time slices to process one cycle. This means that the actual cycle time is 20 ms if the CPU fully utilizes the configured communication load.

A 50 % communication load means that, on average, 500 µs and 500 µs of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 500 µs = 20 time slices to process one cycle. This means that the actual cycle time is 20 times a 1 ms time slice = 20 ms, if the CPU fully utilizes the configured communication load.

This means that 50% communications do not increase the cycle linearly by 5 ms but by 10 ms.

Dependency of the Actual Cycle Time on the Communication Load

The following figure describes the non-linear dependency of the actual cycle time on the communication load. As an example, we have chosen a cycle time of 10 ms.

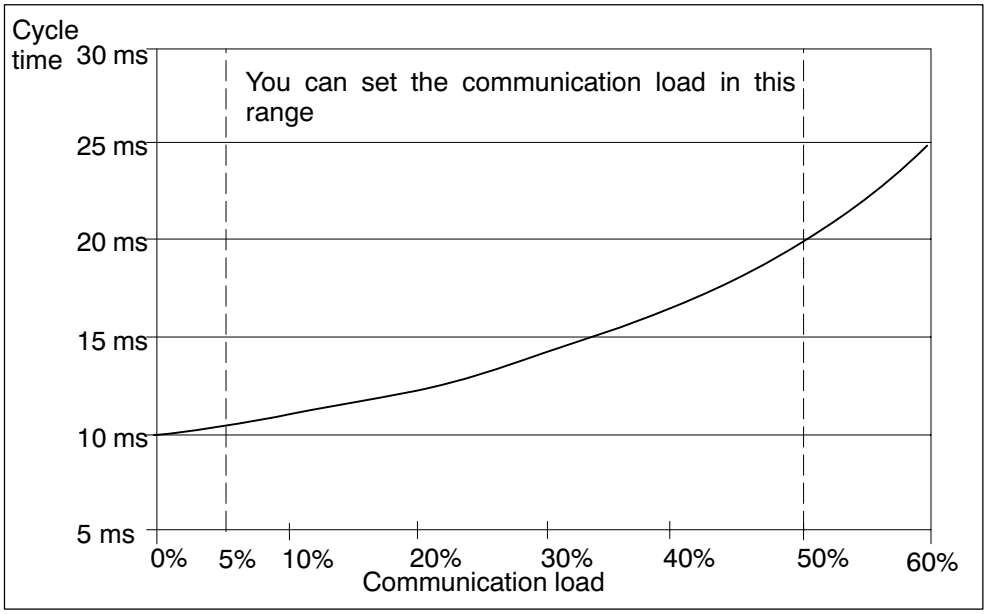


Figure 5-6 Dependency of the Cycle Time on the Communication Load

Further Effect on the Actual Cycle Time

Due to the increase in the cycle time as a result of the communications component, even more asynchronous events occur, from a statistical point of view, within an OB 1 cycle than, say, interrupts. This also increases the OB 1 cycle. This increase depends on how many events occur per OB 1 cycle and how long event processing lasts.

Notes

- Check the effects of a change of the value for the parameter “Cycle load due to communications” in system operation.
- The communication load must be taken into account when you set the maximum cycle time, since time errors will occur if it is not.

Recommendations

- If possible, apply the default value.
- Use a larger value only if the CPU is being used primarily for communication purposes and the user program is non-time-critical. In all other cases select a smaller value.

5.5 Reaction Time

Definition of the Reaction Time

The reaction time is the time from an input signal being detected to changing an output signal linked to it.

Variation

The actual reaction time is somewhere between a shortest and a longest reaction time. For configuring your system, you must always reckon with the longest reaction time.

The shortest and longest reaction times are analyzed below so that you can gain an impression of the variation of the reaction time.

Factors

The reaction time depends on the cycle time and on the following factors:

- Delay in the inputs and outputs
- Additional DP cycle times on the PROFIBUS-DP network
- Execution of the user program

Delay in the Inputs and Outputs

Depending on the module, you must heed the following time delays:

- For digital inputs: the input delay
- For interrupt-capable digital inputs: the input delay + the module-internal preparation time
- For digital outputs: negligible time delays
- For relay outputs: typical time delays from 10 to 20 ms. The delay of the relay outputs depends, among other things, on the temperature and voltage.
- For analog inputs: cycle time of analog input module
- For analog outputs: response time of the analog output module

The time delays can be found in the technical specifications of the signal modules.

DP Cycle Times on the PROFIBUS-DP Network

If you have configured your PROFIBUS-DP network with *STEP 7*, then *STEP 7* will calculate the typical DP cycle time that must be expected. You can then have the DP cycle time of your configuration displayed for the bus parameters on the programming device.

The following figure will provide you with an overview of the DP cycle time. We assume in this example that each DP slave has 4 byte of data on average.

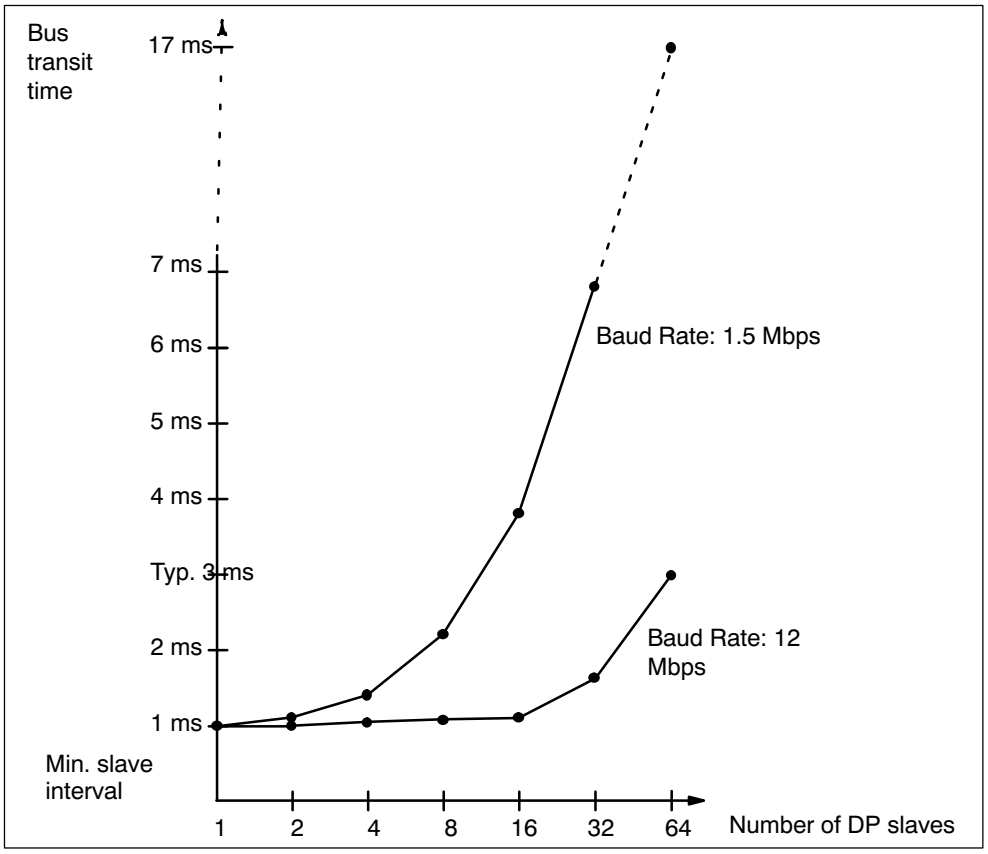


Figure 5-7 DP Cycle Times on the PROFIBUS-DP Network

If you are operating a PROFIBUS-DP network with more than one master, you must take the DP cycle time into account for each master. In other words, perform a separate calculation for each master and add the results together.

Shortest Reaction Time

The following figure illustrates the conditions under which the shortest reaction time is achieved.

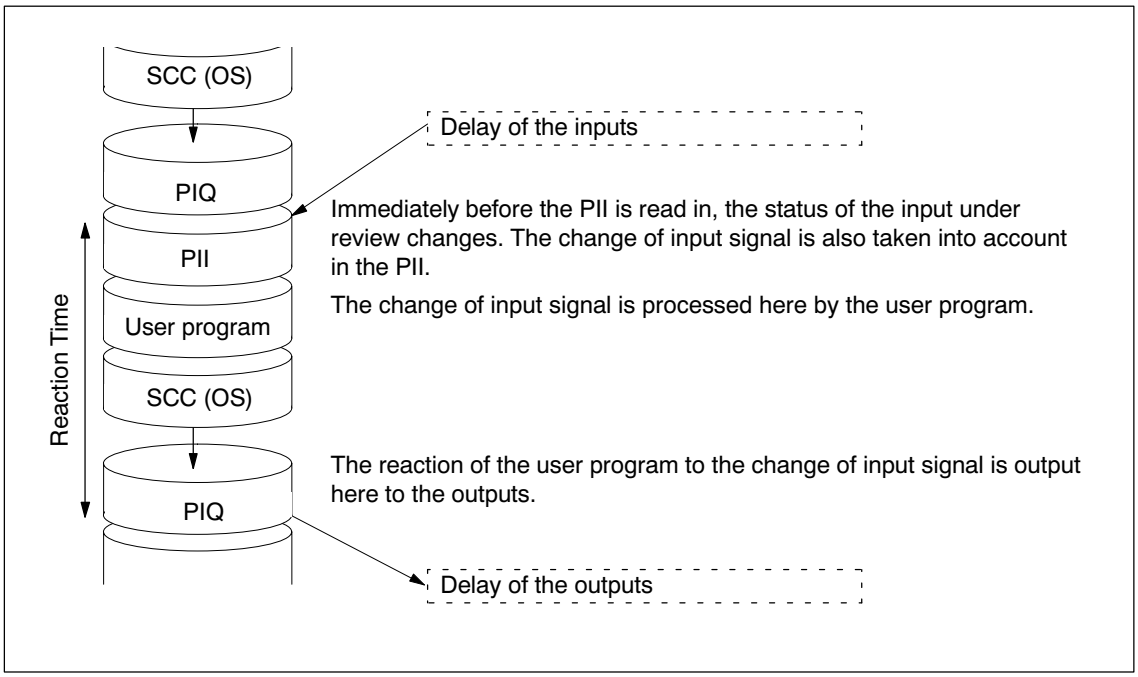


Figure 5-8 Shortest Reaction Time

Calculation

The (shortest) reaction time is made up as follows:

- 1 × process image transfer time of the inputs +
- 1 × process image transfer time of the outputs +
- 1 × program processing time +
- 1 × operating system processing time at SCC +
- Delay in the inputs and outputs

This is equivalent to the sum of the cycle time and the delay in the inputs and outputs.

Note

If the CPU and signal module are not in the central rack, you have to add double the runtime of the DP slave frame (including processing in the DP master).

Longest Reaction Time

The following figure shows you how the longest reaction time results.

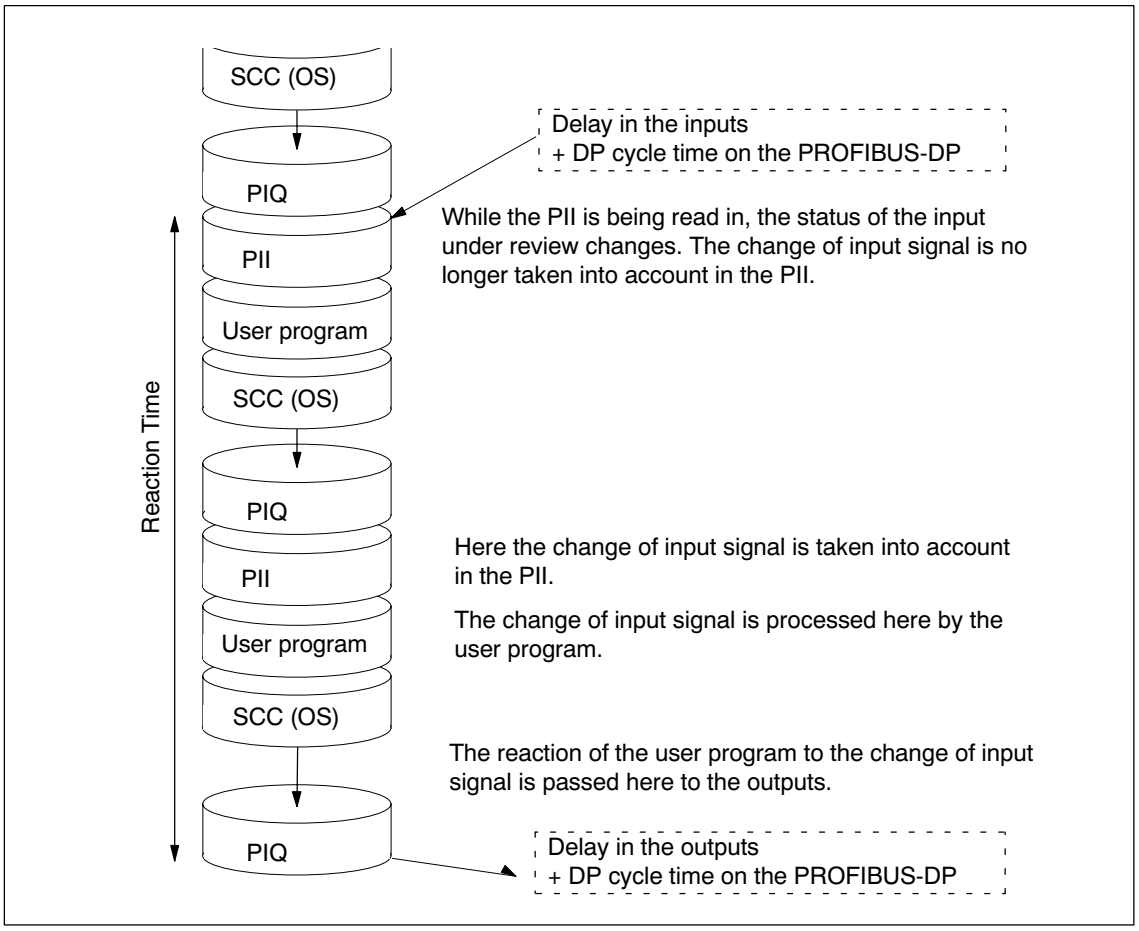


Figure 5-9 Longest Reaction Time

Calculation

The (longest) reaction time is made up as follows:

- 2 × process image transfer time of the inputs +
- 2 × process image transfer time of the outputs +
- 2 × operating system processing time +
- 2 × program processing time +
- 2 × runtime of the DP slave frame (including processing in the DP master) +
- Delay in the inputs and outputs

This is equivalent to the sum of twice the cycle time and the delay in the inputs and outputs plus twice the DP cycle time.

I/O Direct Accesses

You can achieve faster reaction times by direct access to the I/O in the user program, for example with

- L PIB or
- T PQW

you can avoid the reaction times in part, as described above.

Reducing the Reaction Time

In this way the maximum reaction time is reduced to

- Delay in the inputs and outputs
- Runtime of the user program (can be interrupted by high-priority interrupt handling)
- Runtime of direct accesses
- Twice the bus transit time of DP

The following table lists the execution times of direct accesses by the CPU to I/O modules. The times shown are “ideal values”.

Table 5-6 Reducing the Reaction Time

Type of Access	CPU 412-1 412-2	CPU 414-2 414-3	CPU 416-2 416-3	CPU 417-4
I/O Module				
Read byte	3.0 µs	2.7 µs	2.4 µs	2.3 µs
Read word	4.7 µs	4.4 µs	3.9 µs	3.8 µs
Read double word	7.6 µs	7.2 µs	6.9 µs	6.7 µs
Write byte	3.2 µs	2.8 µs	2.4 µs	2.3 µs
Write word	4.7 µs	4.5 µs	4.1 µs	4.0 µs
Write double word	8.1 µs	7.7 µs	7.3 µs	7.2 µs
Expansion device with close coupling				
Read byte	6.4 µs	6.2 µs	5.8 µs	5.7 µs
Read word	11.8 µs	11.3 µs	10.9 µs	10.8 µs
Read double word	21.7 µs	21.3 µs	20.9 µs	20.8 µs
Write byte	7.9 µs	5.8 µs	5.6 µs	5.5 µs
Write word	11.2 µs	11.0 µs	10.6 µs	10.5 µs
Write double word	21.1 µs	20.7 µs	20.4 µs	20.2 µs

Type of Access	CPU 412-1 412-2	CPU 414-2 414-3	CPU 416-2 416-3	CPU 417-4
Reading bytes in the expansion device with remote coupling				
Read byte	11.4 µs	11.4 µs	11.3 µs	11.3 µs
Read word	22.9 µs	22.9 µs	22.8 µs	22.8 µs
Read double word	45.9 µs	45.9 µs	45.9 µs	45.9 µs
Write byte	11.0 µs	10.9 µs	10.8 µs	10.8 µs
Write word	22.0 µs	22.0 µs	21.9 µs	21.9 µs
Write double word	44.0 µs	44.0 µs	44.0 µs	44.0 µs

The specified times are merely CPU processing times and apply, unless otherwise stated, to signal modules in the central rack.

Note

You can similarly achieve fast reaction times by using hardware interrupts; refer to Section 5.8.

5.6 How Cycle and Reaction Times Are Calculated

Cycle time

1. Using the Instruction List, determine the runtime of the user program.
2. Calculate and add the transfer time for the process image. You will find guide values for this in Table 5-3.
3. Add to it the processing time at the scan cycle checkpoint. You will find guide values for this in Table 5-4.

The result you achieve is the cycle time.

Increasing the Cycle Time with Communication and Interrupts

4. Multiply the result by the following factor:

$$\frac{100}{100 - \text{“configured communication load in \%”}}$$

5. Using the Instruction List, calculate the runtime of the program sections that hardware interrupts. Add to it the relevant value in Table 5-5.
   Multiply this value by the factor from step 4.
   Add this value to the theoretical cycle time as often as the interrupt is triggered or is expected to be triggered during the cycle time.

The result you obtain is approximately the actual cycle time. Make a note of the result.

Table 5-7 Example of Calculating the Reaction Time

Shortest Reaction Time	Longest Reaction Time
6. Then, calculate the delays in the inputs and outputs and, if applicable, the DP cycle times on the PROFIBUS DP network.	6. Multiply the actual cycle time by a factor of 2.
	7. Then, calculate the delays in the inputs and outputs and the DP cycle times on the PROFIBUS DP network.
7. The result you obtain is the shortest reaction time.	8. The result you obtain is the longest reaction time.

5.7 Examples of Calculating the Cycle Time and Reaction Time

Example I

You have installed an S7-400 with the following modules in the central rack:

- One CPU 414-2
- Two digital input modules SM 421; DI 32 x DC 24 V (4 byte each in PA)
- Two digital output modules SM 422; DO 32 x DC 24 V/0.5A (4 byte each in PA)

User Program

According to the Instruction List, your user program has a runtime of 15 ms.

Cycle Time Calculation

The cycle time for the example results from the following times:

- Process image transfer time

  Process image: 13 µs + 16 byte x 1.5 µs = approx. **0.037 ms**

- Operating system runtime at scan cycle checkpoint:
  approx. **0.23 ms**

The cycle time for the example results from the sum of the times listed:

Cycle time = 12.0 ms + 0.037 ms + 0.23 ms **= 12.27 ms.**

Calculation of the Actual Cycle Time

- Allowance of the communication load (default value: 20%):
  12.27 ms * 100 / (100-20) **= 15.24 ms.**
- There is no interrupt handling.

The rounded actual cycle time is thus **15.3 ms.**

Calculation of the Longest Reaction Time

- Longest reaction time
  15.3 ms * 2 = **30.6 ms.**
- The delay in the inputs and outputs is negligible.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- There is no interrupt handling.

Rounded off, the longest reaction time is thus = **31 ms.**

Example II

You have installed an S7-400 with the following modules:

- One CPU 414-2
- Four digital input modules SM 421; DI 32 x DC 24 V (4 byte each in PA)
- Three digital output modules SM 422; DO 16 x DC 24 V/2A (2 byte each in PA)
- Two analog input modules SM 431; AI 8 x 13 bit (not in PA)
- Two analog output modules SM 432; AO 8 x 13 bit (not in PA)

CPU Parameters

The CPU has been assigned parameters as follows:

- Cycle load due to communications: 40%

User Program

According to the Instruction List, the user program has a runtime of 10.0 ms.

Cycle Time Calculation

The theoretical cycle time for the example results from the following times:

- Process image transfer time
  Process image: 13 µs + 22 byte x 1.5 µs = approx. **0.049 ms**
- Operating system runtime at scan cycle checkpoint:
  approx. **0.23 ms**

The cycle time for the example results from the sum of the times listed:

Cycle time = 10.0 ms + 0.049 ms + 0.23 ms = **10.28 ms.**

Calculation of the Actual Cycle Time

- Allowance of communication load:
  10.28 ms * 100 / (100-40) = **37 ms.**
- A time-of-day interrupt having a runtime of 0.5 ms is triggered every 100 ms. The interrupt cannot be triggered more than once during a cycle:
  0.5 ms + 0.35 ms (in Table 5-5) = **0.85 ms.**
  Allowance for communication load:
  0.85 ms * 100 / (100-40) = **1.42 ms.**
- 17.1 ms + 1.42 ms = **18.52 ms.**

The actual cycle time is therefore **18.5 ms** taking into account the time slices**.**

Calculation of the Longest Reaction Time

- Longest reaction time
  8.5 ms * 2 = **37 ms.**
- Delays in the inputs and outputs
  - The digital input module SM 421; DI 32 x DC 24 V has an input delay of not more than **4,8 ms** per channel
  - The digital output module SM 422; DO 16 x DC 24 V/2A has a negligible output delay.
  - The analog input module SM 431; AI 8 x 13 bit was assigned parameters for 50 Hz interference frequency suppression. This results in a conversion time of 25 ms per channel. Since 8 channels are active, a cycle time of **200 ms** results for the analog input module.
  - Analog output module SM 432; AO 8 x 13 bit was assigned parameters for the measuring range from 0 to 10V. This results in a conversion time of **0.3 ms** per channel. Since 8 channels are active, a cycle time of 2.4 ms results. To this must be added the settling time for the resistive load, which is 0.1 ms. A response time of **2.5 ms** therefore results for an analog output.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- **Case 1:** When a digital signal is read in, an output channel of the digital output module is set. This produces a reaction time of:

  Reaction time= 37 ms + 4.8 ms **= 41.8 ms**.
- **Case 2:** An analog value is read in and an analog value output. This produces a reaction time of:

  Reaction time = 37 ms + 200 ms + 2.5 ms **= 239.5 ms**.

5.8 Interrupt Reaction Time

Definition of the Interrupt Reaction Time

The interrupt reaction time is the time from when an interrupt signal first occurs to calling the first instruction in the interrupt OB.

The following general rule applies: Interrupts having a higher priority take precedence. This means that the interrupt reaction time is increased by the program processing time of the higher priority interrupt OBs and interrupt OBs with the same priority that have not yet been processed (queue).

Note
The interrupt reaction times can be delayed by read and write jobs with a high data volume (approx. 460 byte).
When interrupts are transferred between a CPU and DP master, only a diagnostic **or** hardware interrupt can be currently reported at any time from a DP line.

Calculation

	Min. interrupt reaction time of the CPU		Max. interrupt reaction time of the CPU
+	min. interrupt reaction time of the signal modules	+	max. interrupt reaction time of the signal modules
+	DP cycle time on PROFIBUS-DP	+	2 * DP cycle time on PROFIBUS-DP
=	Shortest Reaction Time	=	Longest Reaction Time

Figure 5-10 Calculating the Interrupt Reaction Time

Hardware Interrupt and Diagnostic Interrupt Reaction Times of CPUs

Table 5-8 Hardware Interrupt and Diagnostic Interrupt Reaction Times; Maximum Interrupt Reaction Time Without Communication

CPU	Process interrupt reaction times		Diagnostic interrupt reaction times		Asynchronous error (OB 85, at process image update)
	min.	max.	min.	max.	
412-1/-2	544 µs	560 µs	608 µs	624 µs	392 µs
414-2/-3	325 µs	335 µs	365 µs	375 µs	300 µs
416-2/-3	220 µs	230 µs	245 µs	255 µs	200 µs
417-4	200 µs	210 µs	225 µs	235 µs	180 µs

Increasing the Maximum Interrupt Reaction Time with Communication

The maximum interrupt reaction time increases when communication functions are active. The increase is calculated with the following formula:

CPU 412: tv = 200 µs + 1000 µs x n%

CPU 414-417: tv = 100 µs + 1000 µs x n%

where n = cycle load from communication

Signal Modules

The hardware interrupt reaction time of the signal modules is made up as follows:

- Digital input modules

  Hardware interrupt reaction time = internal interrupt processing time + input delay

  You will find the times in the data sheet of the digital input module concerned.

- Analog input modules

  Hardware interrupt reaction time = internal interrupt processing time + conversion time

  The internal interrupt processing time of the analog input modules is negligible. The conversion times can be taken from the data sheet of the analog input module concerned.

The diagnostic interrupt reaction time of the signal modules is the time which elapses between a diagnostics event being detected by the signal module and the diagnostic interrupt being triggered by the signal module. This time is so small that it can be ignored.

Hardware Interrupt Processing

When the hardware interrupt OB 40 is called, the hardware interrupt is processed. Interrupts with higher priority interrupt hardware interrupt processing, and direct access to the I/O is made when the instruction is executed. When hardware interrupt processing is completed, either cyclic program processing is continued or other interrupt OBs with the same or a lower priority are called and processed.

5.9 Example of Calculating the Interrupt Reaction Time

Parts of the Interrupt Reaction Time

As a reminder, the hardware interrupt reaction time is made up of the following:

- Hardware interrupt reaction time of the CPU
- Hardware interrupt reaction time of the signal module.
- 2 × DP cycle time on the PROFIBUS-DP

Example: You have an S7-400 consisting of a CPU 416-2 and 4 digital modules in the central rack. One digital input module is the SM 421; DI 16×UC 24/60 V; with hardware and diagnostic interrupts. In the parameter assignment of the CPU and the SM, you have only enabled the hardware interrupt. You do not require time-driven processing, diagnostics and error handling. You have assigned an input delay of 0.5 ms for the digital input module. No activities at the scan cycle checkpoint are required. You have set a cycle load from communication of 20%.

Calculation

The hardware interrupt reaction time for the example results from the following times:

- Hardware interrupt reaction time of the CPU 416-2: approx. 0.35 ms
- Increase from communication in accordance with the formula shown in Table 5-8 :

  100 µs + 1000 µs x 20% = 300 µs = 0.3 ms
- Hardware interrupt reaction time of the SM 421; DI 16 x UC 24/60 V:
  - Internal interrupt processing time: 0.5 ms
  - Input delay: 0.5 ms
- Since the signal modules are plugged into the central rack, the DP cycle time on the PROFIBUS-DP is not relevant.

The hardware interrupt reaction time results from the sum of the listed times:

Hardware interrupt reaction time = 0.23 ms +0.3 ms + 0.5 ms + 0.5 ms = approx. **1.53 ms**.

This calculated hardware interrupt reaction time is the time from a signal being applied across the digital input to the first instruction in OB 40.

5.10 Reproducibility of Time-Delay and Watchdog Interrupts

Definition of “Reproducibility”

Time-delay interrupt:

The deviation with time from the first instruction of the interrupt OB being called to the programmed interrupt time.

Watchdog interrupt

The variation in the time interval between two successive calls, measures between the first instruction of the interrupt OB in each case.

Reproducibility

Table 5-9 contains the reproducibility of time-delay and watchdog interrupts of the CPUs.

Table 5-9 Reproducibility of Time-Delay and Watchdog Interrupts of the CPUs.

Module	Reproducibility	
	Time-Delay Interrupt:	Watchdog Interrupt
CPU 412-1/-2	–220 µs / +220 µs	–35 µs / +35 µs
CPU 414-2/-3	–235 µs / +205 µs	–35 µs / +35 µs
CPU 416-2/-3	–210 µs / +210 µs	–20 µs / +20 µs
CPU 417-4	–220 µs / +200 µs	–20 µs / +20 µs

These times apply only if the interrupt can be executed at this time and not, for example, delayed by interrupts with higher priority or interrupts of identical priority that have not yet been executed.

Technical Specifications

6

Chapter overview

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6.1 Technical Specifications of the CPU 412-1; (6ES7412-1XF04-0AB0)

CPU and Firmware Version	
MLFB	6ES7412-1XF04-0AB0
• Firmware version	4.0.0
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW update
Memory	
Working memory	
• Integrated	72 Kbytes for code 72 Kbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup with battery	Yes, all data
Processing Times	
Processing times for	
• Bit operations	0.1 µs
• Word instructions	0.1 µs
• Integer math instructions	0.1 µs
• Floating-point math instructions	0.3 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	4 Kbytes
• Retentivity can be set	From MB 0 to MB 4095
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 511 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 8 Kbytes
• Preset	4 Kbytes
Blocks	
OBs	See instruction list
• Size	Limited by working memory
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 256
• Size	Limited by working memory
FCs	Max. 256
• Size	Limited by working memory
Address Areas (Inputs/Outputs)	
Total I/O address area	4 Kbytes/4 Kbytes
• Of which distributed MPI/DP interface	2 Kbytes/2 Kbytes
Process Image	4 Kbytes/4 Kbytes (can be set)
• Preset	128 bytes/128 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 32768/Max. 32768
• Of which central	Max. 32768/Max. 32768
Analog channels	Max. 2048/Max. 2048
• Of which central	Max. 2048/Max. 2048

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	1
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 EX40	
IM 467 cannot be used with the CP 443-1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• PROFIBUS and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	None
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 256
• Number of additional values per message	1
– With 100 ms grid	None
– With 500, 1000 ms grid	1
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 70
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (can be set)	Max. 300
• Preset	150
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	4

Test and Commissioning Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 64
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	15 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	16, with each of them reserved for PG and OPrespectively
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	1 variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 16 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– virtual slots	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time for every strand	
• DPSYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes/100 + number of slaves <16
Constant bus cycle time	Yes
Shortest clock pulse	1.5 ms 0.5 ms without use of SFC 126, 127
see the manual *Clock Synchronism*	
CiR synchronization time	
Base load	100 ns
Time per I/O byte	200 µs

Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 0.6 A Max. 0.7 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 350 µA Max. 890 µA
maximum backup time	See manual *Module Specifications*, chapter 3.3
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 3.0 W

6.2 Technical Specifications of the CPU 412-2; (6ES7412-2XG04-0AB0)

CPU and Version	
MLFB	6ES7412-2XG04-0AB0
• Firmware version	V 4.0.0
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update
Memory	
Working memory	
• Integrated	128 KB for code
	128 KB for data
Load memory	
• Integrated	256 KB RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 MB
• Expandable RAM	With memory card (RAM) up to 64 MB
Backup	Yes
• With battery	All data
• Without battery	None
Typical processing times	
Processing times for	
• Bit operations	0.1 µs
• Word instructions	0.1 µs
• Integer math instructions	0.1 µs
• Floating-point math instructions	0.3 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Flags	4 Kbytes
• Retentivity can be set	From MB 0 to MB 4095
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 511 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 8 Kbytes
• Preset	4 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	1
FBs	Max. 256
• Size	Max. 64 Kbytes
FCs	Max. 256
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	4 Kbytes/4 Kbytes
• Of which distributed	incl. diagnostic addresses for I/O intrerfaces etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	4 Kbytes/4 Kbytes
Process Image	4 Kbytes/4 Kbytes (can be set)
• Preset	128 bytes/128 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 32768/Max. 32768
• Of which central	Max. 32768/Max. 32768
Analog channels	Max. 2048/Max. 2048
• Of which central	Max. 2048/Max. 2048

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
IM 467 cannot be used with the CP 443-1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	None
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 256
• Number of additional values per message	1
– With 100 ms grid	None
– With 500, 1000 ms grid	1
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 70
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (can be set)	Max. 300
• Default	150
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	4

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Quantity	Max. 64
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 400 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	15 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	16, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 16 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
• User data per DP slave **Note:** • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Virtual slots	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16
Functionality	
• PROFIBUS DP	DP master/DP slave
2nd Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cylce time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 64
• Address area	Max. 4 Kbytes inputs / 4 Kbytes outputsMax. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
• User data per DP slave	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
2nd Interface DP Slave Mode	
Technical specifications as for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time per segment	
• DP_SYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	200 µs
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Nnmber of bytes/100 + number of slaves <16
Constant bus cylce time	Yes
Shortest clock pulse	1.5 ms 0.5 ms without use of SFC 126, 127
see manual *Clock Synchronism*	
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0,72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.0 A Max. 1.2 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 350 µA Max. 890 µA
maximum backup time	See manual *Module Specifications*, chapter 3.3
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 4.5 W

6.3 Technical Specifications of the CPU 414-2; (6ES7414-2XG04-0AB0)

CPU and Version	
MLFB	6ES7414-2XG04-0AB0
• Firmware version	V 4.0.0
Associated programming package	As of STEP7 5.2 SP1 HF3 with HW-Update
Memory	
Working memory	
• Integrated	256 Kbytes for code 256 Kbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup with battery	Yes, all data
Typ. processing Times	
Processing times for	
• Bit operations	0.06 µs
• Word instructions	0.06 µs
• Integer math instructions	0.06 µs
• Floating-point math instructions	0.18 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	8 Kbytes
• Retentivity can be set	From MB 0 to MB 8191
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 16 Kbytes
• Preset	8 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	1
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	8 Kbytes/8 Kbytes
• Of which distributed	incl. diagnostic addresses for I/O interfaces, etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	6 Kbytes/6 Kbytes
Process Image	8 Kbytes/8 Kbytes (can be set)
• Preset	256 bytes/256 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 65536/Max. 65536
• Of which central	Max. 65536/Max. 65536
Analog channels	Max. 4096/Max. 4096
• Of which central	Max. 4096/Max. 4096

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
IM 467 cannot be used with the CP 443-1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs, LANs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	Max. 128
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 512
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500 – 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 100
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (can be set)	Max. 600
• Preset	300
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 256
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 400 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	31 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	32, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	1 variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 32 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
Utilities	
• Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/ 2 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
• User data per DP slave	
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16
Functionality	
• PROFIBUS DP	DP master/DP slave
2nd Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 96
• Address area	Max. 6 Kbytes inputs/6 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs,
• User data per DP slave	max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
2nd Interface DP Slave Mode	
As for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
System function blocks (SFB)	See instruction list
Number of SFCs active at the same time for every strand	
• DP_SYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	80 µs
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: number of bytes / 100 + number of slaves < 26
Constant bus cycle time	Yes
Shortest clock pulse	1 ms
See manual *Clock Synchronism*	0.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0,72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.0 A Max. 1.2 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 550 µA Max. 1530 µA
maximum backup time	See manual *Module Specifications*, chapter 3.3
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 1,5 W

6.4 Technical Specifications of the CPU 414-3; (6ES7414-3XJ04-0AB0)

CPU and Version	
MLFB	6ES7414-3XJ04-0AB0
• Firmware version	V 4.0.0
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update
Memory	
Working memory	
• Integrated	700 Kbytes for code 700 Kbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup with battery	Yes, all data
Typ. Processing Times	
Processing times for	
• Bit operations	0.06 µs
• Word instructions	0.06 µs
• Integer math instructions	0.06 µs
• Floating-point math instructions	0.18 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	8 Kbytes
• Retentivity can be set	From MB 0 to MB 8191
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 16 Kbytes
• Preset	8 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	1
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	8 Kbytes/8 Kbytes
• Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	6 Kbytes/6 Kbytes
Process Image	8 Kbytes/8 Kbytes (can be set)
• Preset	256 bytes/256 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 65536/Max. 65536
• Of which central	Max. 65536/Max. 65536
Analog channels	Max. 4096/Max. 4096
• Of which central	Max. 4096/Max. 4096

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
IM 467 cannot be used with the CP 443-1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964-DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	Max. 128
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 512
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500 to 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 100
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 600
• Preset	300
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 256
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	31 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	32, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	1 variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 32 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs,
• User data per DP slave	max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– virtual slots	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16
Functionality	
• PROFIBUS DP	DP master/DP slave
2nd Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 96
• Address area	Max. 6 Kbytes inputs/6 Kbytes outputs
• User data per DP slave • User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
2nd Interface DP Slave Mode	
As for the 1st interface	
3rd Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list

Number of SFCs active at the same time for every strand	
• DP_SYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	80 µs
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Numer of bytes/100 + number of slaves <16
Constant bus cycle time	Yes
Shortest clock pulse	1 ms 0.5 ms without use of SFC 126, 127
Longest clock pulse see *Clock Synchronism* manual	32 ms
Dimensions	
Mounting dimensions W×H×D (mm)	50×290×219
Slots required	2
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.0 A Max. 1.2 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ 550 µA Max. 1530 µA
maximum backup time	See manual *Module Specifications*, chapter 3.3
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 4.5 W

6.5 Technical Specifications of the CPU 416-2; (6ES7416-2XK04-0AB0, 6ES7416-2FK04-0AB0)

CPU and Version	
MLFB	6ES7416-2XK04-0AB0 6ES7416-2FK04-0AB0
• Firmware version	V 4.0.0
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update
Memory	
Working memory	
• Integrated	1.4 Mbytes for code 1.4 Mbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup with battery	Yes, all data
Typ. processing times	
Processing times for	
• Bit operations	0.04 µs
• Word instructions	0.04 µs
• Integer math instructions	0.04 µs
• Floating-point math instructions	0.12 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 32 Kbytes
• Preset	16 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	512 bytes/512 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 131072/ Max. 131072
• Of which central	Max. 131072/ Max. 131072
Analog channels	Max. 8192/ Max. 8192
• Of which central	Max. 8192/ Max. 8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
IM 467 cannot be used with the CP 443-1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Operating hours counters	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 12
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 200
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	63 without message processing, 12 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packages	
– Sender	Max. 16
– Receiver	Max. 32
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	1 variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 44 DP: 32, a diagnostic repeater in the segment reduces the number of connection resources by 1
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/ 2 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs,
• User data per DP slave	max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– virtual slots	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes
2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	32, a diagnostic repeater on the segment reduces the number of connection resources by 1

Functionality	
• PROFIBUS DP	DP Master/DP Slave
2nd Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 125
• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs / 244 bytes outputs distributed over 244 slots each with 128 bytes
2nd Interface DP Slave Mode	
As for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time for every strand	
• DP_SYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes

CiR synchronization time	
Base load	100 ms
Time per I/O byte	40 µs
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes/100 + number of slaves <40
Constant bus cycle time	Yes
Shortest clock pulse	1 ms
Longest pulse clock see manual *Clock Synchronism*	0.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.0 A Max. 1.2 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 550 µA Max. 1539 µA
maximum backup time	See manual *Module Specifications*, chapter 3.3
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 4.5 W

6.6 Technical Specifications of the CPU 416-3; (6ES7416-3XL04-0AB0)

CPU and Version	
MLFB	6ES7416-3XL04-0AB0
• Firmware version	V 1.0
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update
Memory	
Working memory	
• Integrated	2.8 Mbytes for code 2.8 Mbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup with battery	Yes, all data
Typ. Processing Times	
Processing times for	
• Bit operations	0.04 µs
• Word instructions	0.04 µs
• Integer math instructions	0.04 µs
• Floating-point math instructions	0.12 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data area (incl. memory markers, timers, counters)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 32 Kbytes
• Preset	16 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	512 bytes/512 bytes
• Number of process images partitions	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 131072/ Max. 131072
• Of which central	Max. 131072/ Max. 131072
Analog channels	Max. 8192/ Max. 8192
• Of which central	Max. 8192/ Max. 8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
IM 467 cannot be used with the CP 443-1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 12
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 200
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	63 without message processing, 12 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packages	
– Sender	Max. 16
– Receiver	Max. 32
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	1 variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 44 DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs,
• User data per DP slave	max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes inputs
– virtual slots	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	32, a diagnostic repeater in the strand reduces the number of connection resources by 1
Functionality	
• PROFIBUS DP	DP master/DP slave
2nd Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 125
• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs,
• User data per DP slave	max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
2nd Interface DP Slave Mode	
As for the 1st interface	
3rd Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time for every strand	
• DPSYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	40 µs
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: NUmber of bytes/50 + number of slaves
Constant bus cycle time	Yes
Shortest clock pulse	1 ms
Longest clock pulse	0.5 ms without use of SFC 126, 127
see manual *Clock Synchronism*	
Dimensions	
Mounting dimensions W×H×D (mm)	50×290×219
Slots required	2
Weight	approx. 1.07 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.2 A Max. 1.4 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 550 µA Max. 1530 µA
maximum backup time	See manual *Module Specifications*, chapter 3.3
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 5.0 W

6.7 Technical Specifications of the CPU 417-4; (6ES7417-4XL04-0AB0)

CPU and Version	
MLFB	6ES7417-4XL04-0AB0
• Firmware version	V 1.0
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update
Memory	
Working memory	
• Integrated	10 Mbytes for code
	10 Mbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup with battery	Yes, all data
Processing Times	
Processing times for	
• Bit operations	0.03 µs
• Word instructions	0.03 µs
• Integer math instructions	0.03 µs
• Floating-point math instructions	0.09 µs
Timers/Counters and Their Retentivity	
S7 counters	2048
• Retentivity can be set	From Z 0 to Z 2047
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	2048
• Retentivity can be set	From T 0 to T 2047
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 8191 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 64 Kbytes
• Preset	32 Kbytes

Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 6144
• Size	Max. 64 Kbytes
FCs	Max. 6144
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	1024 bytes/1024 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 131072/ Max. 131072
• Of which central	Max. 131072/ Max. 131072
Analog channels	Max. 8192/ Max. 8192
• Of which central	Max. 8192/ Max. 8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	2
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
IM 467 cannot be used with the CP 443–1 EX40 in PN IO mode	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	as master or slave

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 16
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 200
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks **and** blocks for S7 communication (can be set)	Max. 10000
• Preset	1200
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	64

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	63 without message processing, 16 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packages	
– Sender	Max. 16
– Receiver	Max. 32
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	via SFC I_GET and I_PUT
• User data per job	Max. 76 bytes
– Of which consistent	1 variable
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 44 DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st Interface MPI Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes via SFC X_SEND, X_RCV, X_GET and X_PUT
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps
1st Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	max. 244 bytes inputs,
• User data per DP slave	max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note:	
• The accumulated number of input bytes at the slots may not exceed 244	
• The accumulated number of output bytes at the slots may not exceed 244	
• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st Interface DP Slave Mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Utilities	
– Monitor/modify	Yes
– Programming	Yes
– Routing	Yes
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Virtual slots	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes
2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA

Number of connection resources	32, a diagnostic repeater in the strand reduces the number of connection resources by 1
Functionality	
• PROFIBUS DP	DP master/DP slave
2nd Interface DP Master Mode	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– S7 basic communication	Yes
– S7 communication	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 125
• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave • User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 8 KB inputs /8 KB outputs) accumulated by 125 slaves may not be exceeded	
2nd Interface DP Slave Mode	
As for the 1st interface	
3rd Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
4th Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time for every strand	
• DPSYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	40 µs
Clock synchronism	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes/50 + number of slaves
Constant bus cycle time	Yes
Shortest clock pulse see manual *Clock Synchronism*	1 ms 0.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	50×290×219
Slots required	2
Weight	approx. 1,07 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 A Max. 1.7 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typically 600 µA Maximum 1810 µA
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
maximum backup time	See manual *Module Specifications*, chapter 3.3
Power loss	Typ. 6.0 W

6.8 Technical Specifications of the Memory Cards

Name	Order Number	Current Consumption at 5 V	Backup Currents
MC 952 / 64 Kbytes / RAM	6ES7952-0AF00-0AA0	Typ. 20 mA Max. 50 mA	Typ. 0.5 µA Max. 20 µA
MC 952 / 256 Kbytes / RAM	6ES7952-1AH00-0AA0	Typ. 35 mA Max. 80 mA	typ. 1 µA Max. 40 µA
MC 952 / 1 Mbyte / RAM	6ES7952-1AK00-0AA0	Typ. 40 mA Max. 90 mA	Typ. 3 µA Max. 50 µA
MC 952 / 2 Mbytes / RAM	6ES7952-1AL00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA
MC 952 / 4 MB / RAM	6ES7952-1AM00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA
MC 952 / 8 MB / RAM	6ES7952-1AP00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA
MC 952 / 16 MB / RAM	6ES7952-1AS00-0AA0	Typ. 100 mA Max. 150 mA	Typ. 50 µA Max. 125 µA
MC 952 / 64 MB / RAM	6ES7952-1AY00-0AA0	Typ. 100 mA Max. 150 mA	Typ. 100 µA Max. 500 µA
MC 952 / 64 Kbytes / 5V Flash	6ES7952-0KF00-0AA0	Typ. 15 mA Max. 35 mA	–
MC 952 / 256 Kbytes / 5V Flash	6ES7952-0KH00-0AA0	Typ. 20 mA Max. 45 mA	–
MC 952 / 1 Mbyte / 5V Flash	6ES7952-1KK00-0AA0	Typ. 40 mA Max. 90 mA	–
MC 952 / 2 Mbytes / 5V Flash	6ES7952-1KL00-0AA0	Typ. 50 mA Max. 100 mA	–
MC 952 / 4 Mbytes / 5V Flash	6ES7952-1KM00-0AA0	Typ. 40 mA Max. 90 mA	–
MC 952 / 8 Mbytes / 5V Flash	6ES7952-1KP00-0AA0	Typ. 50 mA Max. 100 mA	–
MC 952 / 16 Mbytes / 5V Flash	6ES7952-1KS00-0AA0	Typ. 55 mA Max. 110 mA	–
MC 952 / 32 Mbytes / 5V Flash	6ES7952-1KT00-0AA0	Typ. 55 mA Max. 110 mA	–
MC 952 / 64 Mbytes / 5V Flash	6ES7952-1KY00-0AA0	Typ. 55 mA Max. 110 mA	–
Dimensions W x H x D W × H × D (in mm)		7,5 x 57 x 87	
Weight		Max. 35 g	
EMC protection		Provided by construction	

IF 964-DP Interface Submodule

7

Chapter Overview

Section	You will Find	Page
7.1	IF 964-DP Interface Submodule for S7-400	7-2

7.1 IF 964-DP Interface Submodule for S7-400

Order Numbers

You can use the IF 964-DP interface submodule with order number 6ES7964-2AA04-0AB0 in the S7-400 with firmware V4.0 or higher.

The interface is labeled on the front panel and can therefore be identified in mounted state.

Characteristics

The IF 964-DP interface submodule is used for connecting distributed I/O via “PROFIBUS DP”. The submodule has an isolated RS485 interface. The maximum transmission rate is 12 Mbps.

The permissible cable length depends on the transmission rate and the number of nodes. In the case of a point-to-point connection with a speed of 12 Mbps, a cable length of 100 m is possible, and with a speed of 9.6 Kbps a cable length of 1,200 m is possible.

The system can be expanded to 125 stations.

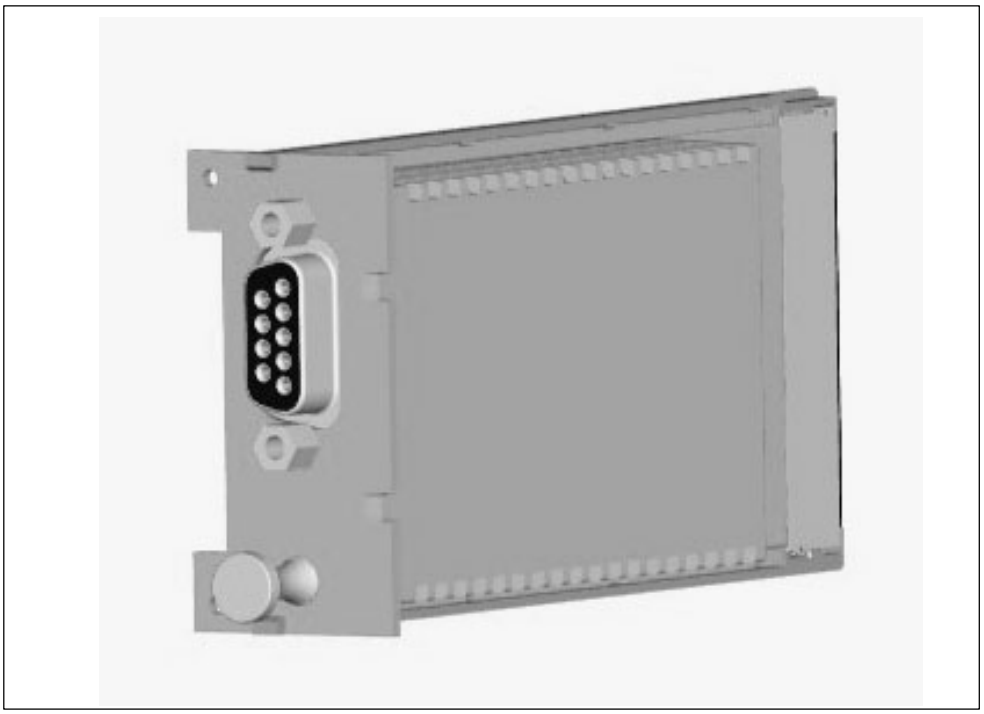

Figure 7-1 IF 964-DP Interface Submodule

Note

Even in an S7-400 CPU you may remove or insert the IF 964-DP interface submodule only if it is **off circuit**.

If you remove the interface submodule while the power supply is switched on, the CPU goes into DEFECTIVE mode.

Additional Information

You can find information on “PROFIBUS DP” in the following technical overviews or manuals:

- DP master manuals, for example, *S7-300 Programmable Controller* or *S7-400, Programmable Controllers* for the PROFIBUS-DP interface
- Manuals on the DP slaves, for example, *ET 200M Distributed I/O Device* or *ET 200C Distributed I/O Device*
- STEP 7 manuals

7.1.1 Pin Assignments

X1 Connector

There is a 9-pin sub D socket connector on the frontside of the submodule for plugging in the connecting cable. See Table 7-1 for the pin assignments.

Table 7-1 X1 Socket, IF 964-DP (9-Pin Sub D Connector)

Pin	Signal	Meaning	Direction
1	–		
2	M 24	24 V reference potential	Output
3	LTG_B	Line B	Input/Output
4	RTSAS	Request to send (AS)	Output
5	$M5_{ext}$	Operational ground (isolated)	Output
6	$P5_{ext}$	+ 5 V (isolated), max. 90 mA (for supplying the bus terminator)	Output
7	P 24 V	+24 V, max. 150 mA, non-isolated	Output
8	LTG_A	Line A	Input
9	–		

7.1.2 Technical Specifications

Technical Specifications

The IF 964-DP interface submodule receives its supply voltage from the CPU. The current consumption given in the technical specifications is the consumption required for dimensioning the power supply.

Dimensions and weights	
Dimensions W x H x D (mm)	26 x 54 x 130
Weight	0.065 kg
Performance	
Transmissoin rate	9.6 kbps to 12 Mbps
Cable length	
• at 9.6 kbps	max. 1200 m
• at 12 Mbps	max. 100 m
Number of stations	≤ 125 (depends on the CPU used)
Interface physics	RS485
Potential isolation	yes

Voltages, Currents	
Power supply	provided by the S7-400
Current sink on S7-400 bus The module does not draw current at 24 V, it merely supplies this voltage to the DP interface	accumulated current consumption of components connected to the DP interface, but max. 150 mA
Load capability on 5 V (floating) ($P5_{ext}$)	max. 90 mA
Load capability on 24 V	max.150 mA
Power loss	1 W

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